Data tiling for memory system design space exploration

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Context: High level synthesis of real-time systems with large amount of data
Problem: Reduce power consumption in memory access and bandwidth bottlenecks by reducing redundancy in data transfer and by using hierarchical memory organization
Idea: Tile separately input and output data spaces for a panel of possible tile’s volume. Link tilings to each other by supertiling algorithm

Supertiling

- Build input and output spaces
- Build supertiling space
- Explore supertiling space

Supertiling matrix

IoT

Functional model

Behavioral model writing

High Level Synthesis: Past and accurate design evaluation

Behavioral models with:
- Different buffers volumes between FUs
- Different number of FUs

Supertiling

Scheduling

Mapping

Designs optimized for data management

Hardware

Pre-calculated mapping and scheduling

- The management of dependencies between tiles held by designer
- Possible mappings
  - Sequentially on the same functional unit
  - In parallel on multiple units
- A controller used to manage data transfer and functional units synchronization

Application

Photoreceptors space variant sampling in Gipsa-lab retina model

Supertiling applied to space variant filter MIP-MAPPED

INNOVATIONS

- Tile data space instead of iteration space
- Applicable to treatments with non-affine memory access
- Data management-driven design space exploration
- Local and global optimizations of data management

PERSPECTIVES

- Automate manual operations
- Study the sensitivity of Supertiling to IO tiles shape
- Treat automatically internal dependencies
- Test supertiling on different targets (multiprocessors, NOC, etc.)
- Test other applications