

ART 2018 - Final Program

Thursday, November 1st

4:00 - 4:15 **OPENING** – Yervant Zorian (Synopsys – US), Paolo Bernardi (Politecnico di Torino – IT)

4:15 - 5:00 KEYNOTE: Burkhard Huhnke, *Vice President for Automotive Strategy, Synopsys US*

5:00 - 7:00 SESSION 1: Design for Automotive Testing

Moderator: Daniel Tille (Infineon - DE)

SRAM and ECC Logic Testing Using On-line MBIST

Alan Becker (ARM - UK)

Tester-On-Chip: An in-field system-test interface for heterogeneous IPs

Devanathan Varadarajan, Srinivas Vooka and Prasad Jondhale (Texas Instruments - US, IND)

In-System-Test (IST) Architecture for NVIDIA Drive-AGX Platforms

Pavan Kumar Datla Jagannadha, Mahmut Yilmaz, Milind Sonawane, Shantanu Sarangi, Sailendra Chadalavada, Bonita Bhaskaran, Narendra Devta Prasanna, Jae Wu, Anitha Kalva, Sunil Bhavsar, Kaushik Narayanun, Hari Krishnan and Patrick Shen (NVIDIA Corporation - US)

A Divide and Conquer Scalable Test Infrastructure to Save Test Time and Resources!

Christophe Eychenne, Gurgun Harutyunyan, Yervant Zorian (Bosch - FR, Synopsys - US)

A Scalable Design for Test Architecture for In-System and Manufacturing Test for Large Automotive ICs

Karthik Subramanian, Praveen Jaini, Adrian Arozqueta and Mohammed Abdelwahid (Ambarella Corp. - US and Mentor, A Siemens Business - US)

Unified and Physically-Aware Compression and LBIST

Christos Papameletis and Vivek Chickermane (Cadence Design Systems - US)

7:00 - 9:00 **Welcome reception**

Friday, November 2nd

8:00 - 10:00 SESSION 2: Functional Safety techniques and tools

Moderator: Michele Portolan (TIMA - FR)

A comprehensive approach to a "Reliability aware" safety Analysis

Shivakumar Chonnad and Radu Iacob (Synopsys - US)

Security and Functional Safety Validation for a Connected Automotive

Ritu Sethi and Riccardo Mariani (INTEL - IND, IT)

FMEDA Configuration tool

Marco Restifo, Oscar Ballan and Federico Venini (Politecnico di Torino - IT and Xilinx - US)

Automotive Functional Safety strategies for an effective use of LBIST and other detection mechanisms

Alessandra Nardi, Francesco Lertora and Antonino Armato (Cadence Design Systems, Inc - US, IT)

Estimating Residual Error Probability of Data Communication In Safety Critical Systems

Srikanth Srinivasan Kaniyanoor, Sivasubramanian Srinivasan, Laura Spinella, Elisa Spano, Gabriele Boschi and Nabajit Deka (INTEL - IT, IND)

FIT Rate Calculation and Mitigation Techniques for Advanced Technologies and Automotive Applications

Gurgun Harutyunyan, Issam Nofal, Michael Nicolaidis, Yervant Zorian (Synopsys - US, IROc - FR and TIMA Lab - FR)

10:00 - 10:30 POSTER SESSION during COFFEE BREAK

On-Chip Delay Measurement for In-field Periodic Test of FPGAs

Yousuke Miyake, Yasuo Sato and Seiji Kajihara (Kyushu Institute of Technology - JP)

TRACE - Enabling Smart Mobility and Smart Infrastructure by Development of a Technology ReAdiness Process for Consumer Electronics

Rebecca Busch, Michael Wahl and Rainer Brück (Universität Siegen - DE)

RETE, embedding reliability for zero defects

Nigel Kissaun and Alessandro Levy Bacchielli (ELES SEMICONDUCTOR EQUIPMENT - IT)

Analysis of Fault Simulations Result during development of a Software Test Library

Andrea Floridia, Davide Piumatti, Annachiara Ruospo and Ernesto Sanchez (Politecnico di Torino - IT)

Test cost and test quality: Key factors for Automotive monster-chips

Davide Appello, Marco Restifo, Matteo Sonza Reorda, David Vondran and Karthik Ranganathan (Politecnico di Torino - IT, STMicroelectronics - IT and Astronics Test Systems - US)

Modelling of cost data in the TRACE project

Rebecca Busch, Michael Wahl and Rainer Brück (Universität Siegen - DE)

SER Qualification and Radiation Effects Implications for Functional Safety in Automotive Electronics

Jyotika Athavale (INTEL - US)

10:30 - 12:00 PANEL: Smarter test for Automotive

Organizer: Teresa McLaurin, ARM

Moderator: Davide Appello, STMicroelectronics - IT

Panelists:

Alan Becker, ARM - UK

Christophe Eychenne, Bosch - FR

Sandeep Goel, TSMC - US

Xiankun (Robert) Jin, NXP - US

Jyotika A Athavale, Intel - US

Abstract: Currently we are so fearful of missing something that we may be planning to overtest in the field. For example, ECC vs online MBIST. If ECC is checking the contents of the memories constantly for correctness, do we need to be periodically doing online MBIST or is MBIST at POST enough? On the other side, how do we ensure the tests we are running are high quality (testing the most critical logic). For instance, if the goal is 90% test coverage and we achieve that on the whole module, we stop looking. But, perhaps if we dig down we might find that some blocks are achieving much less coverage. How do we determine if these contain critical logic? Instead of throwing every test at the problem or not testing to a high enough quality (they may both look the same from a high enough level), can we get smarter about the testing we are doing?

The panelists will address solutions to these important issues, discussing also Functional Safety (FuSa) methodologies to reach the levels of safety demanded by ISO 26262.

12:00 - 1:00 **LUNCH**

1:00 - 1:40 EMBEDDED TUTORIAL: ASPICE and ISO 26262 Compliant Software Development Methodologies

Organizer and Moderator: Rubin Parekhji, Texas Instruments.

Presenters: Zoran Mladenovic and Bharat Rajaram, Texas Instruments.

Abstract: The advent of the several disruptive trends in the automotive industry (vehicle electrification, connectivity and autonomous cars) is expected to increase the semiconductor content in automobiles by 3-5x (vs. conventional cars). As a result the cost of developing quality, reliable SW has easily become a significant portion of the NRE (non-recurring engineering) costs. Several international standards (ASPICE and ISO 26262) recommend the state-of-the-art in developing, testing and productizing quality software. These standards are very broad in their scope as they have to address the needs of all types of electronic systems in cars (from TPMS – tire pressure monitoring systems to completely driverless cars). Car OEMs and Tier 1s are demanding that semiconductor manufacturers follow these standards while developing even the most basic software components like low-level device drivers and SDKs (software development kits). It is important for semiconductor companies to study and interpret the recommendations of these standards and select methods and techniques that are congruent to the complexity of the software being developed. Otherwise it is very easy to be overwhelmed and err on the side of caution by adding on significant overhead for software development teams. In fact, most software developed by semiconductor companies are ‘out-of-context’ as there is limited knowledge regarding the final end-application that the software will be deployed in.

In this tutorial Zoran Mladenovic and Bharat Rajaram will outline a case study in how an ASPICE, ISO 26262 and IEC 61508 compliant software development process was conceptualized and installed at Texas Instruments. This is ~2 year journey, and there are several lessons learned that have now led to a benchmark methodology for reliable, quality software development.

1:40 - 2:40 SESSION 3: Artificial Intelligence for Automotive Test and Reliability

Moderator: Marco Restifo (Politecnico di Torino - IT)

Deep Neural Networks Reliability: A Case Study

Alberto Bosio and Ernesto Sanchez (Lyon U. - FR and Politecnico di Torino - IT)

Kayotee: A Fault Injection-based System to Assess the Safety and Reliability of Autonomous Vehicles to Faults and Errors
Saurabh Jha, Timothy Tsai, Siva Kumar Sastry Hari, Michael Sullivan, Zbigniew Kalbarczyk, Stephen W. Keckler and Ravishankar Iyer (University of Illinois at Urbana - Champaign- US, Nvidia Corporation - US and Coordinated Science Laboratory - US)

Increasing Dependability of Stereo Reconstruction through Deep Learning

Vlad Miclea, Liviu-Cristian Miclea and Sergiu Nedevschi (Technical University of Cluj-Napoca - RO)

2:40 - 2:50 **BREAK**

2:50 - 3:50 SESSION 4: Automotive Reliability

Moderator: Gurgen Harutyunyan (Synopsys - US)

Functional Degradation Analysis of Complete 14nm FinFET SRAM

Daniel Kraak, Innocent Agbo, Mottaqiallah Taouil, Said Hamdioui, Pieter Weckx, Stefan Cosemans and Francky Catthoor (Delft University of Technology - NL and IMEC vzw - BE)

Hybrid Verification Methodology for Automotive RADAR

Sainath Karlapalem, Shashank Venugopal, Shiva Nagendar Pokala and Paulraj M K (NXP Semiconductors - IND)

Scratch Algorithm

Dan Sebban, Leonid Gurov and Gal Peled (Optimal Plus - IL)

3:50 – 4:00 **CLOSING REMARKS**

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