Institute of Microelectronic Systems

Leibniz Universität Hannover

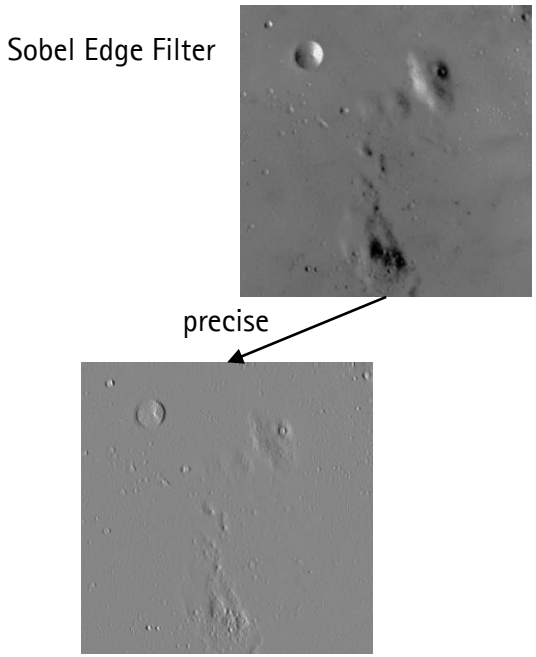
ATE-Accuracy Trade-Offs for Approximate Adders and Multipliers in Pipelined Processor Datapaths

M. Weißbrich[1], A. Najafi[2], A. García-Ortiz[2] and G. Payá-Vayá[1]

1) Institute of Microelectronic Systems, Leibniz Universität Hannover
2) Institute of Electrodynamics and Microelectronics, Universität Bremen

Introduction: Approximate Computing

- Precise computation results not necessary in many applications
  - (Noisy) image processing, edge & feature detection etc.
- Imprecise results in hardware by…



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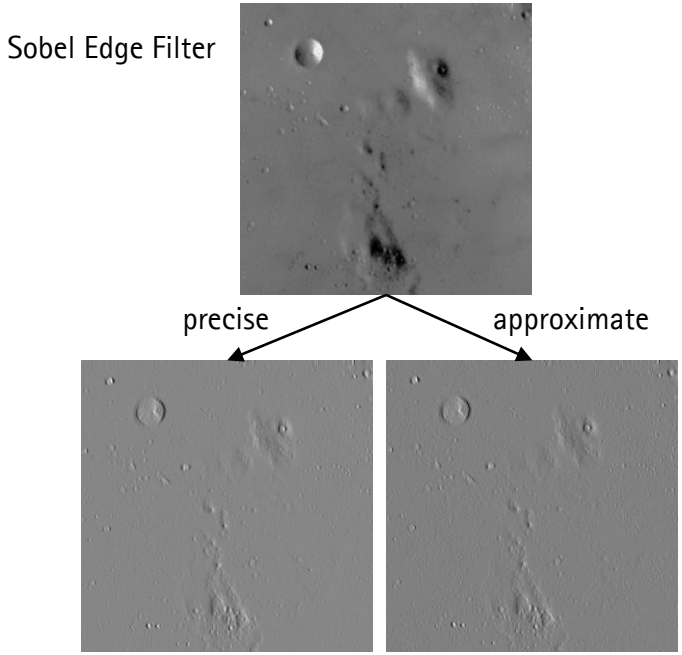

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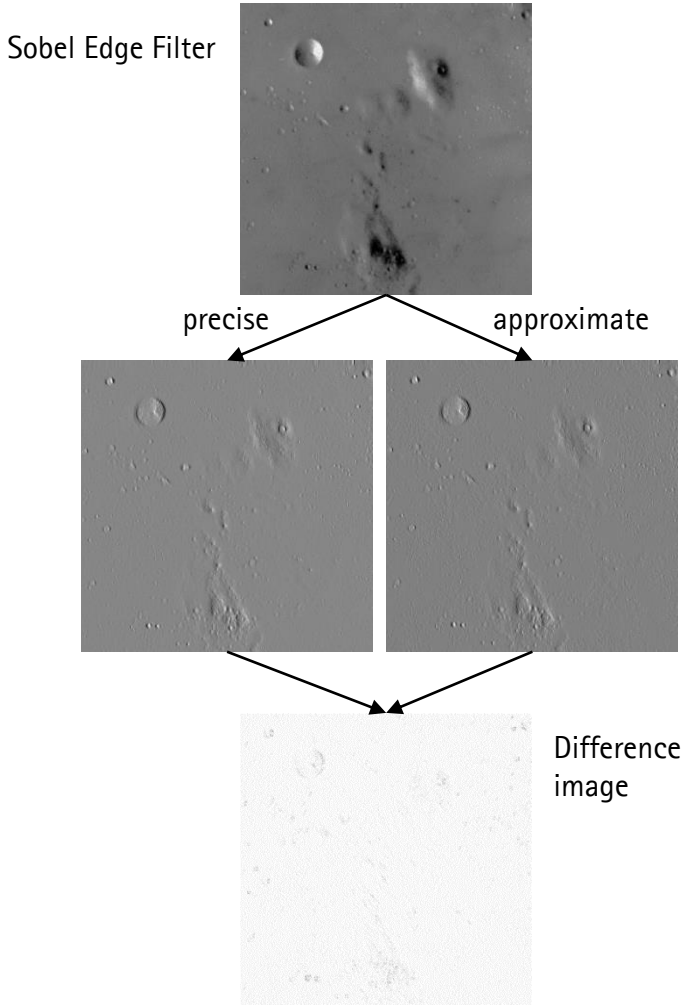

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  - *Stochastic Computing*:
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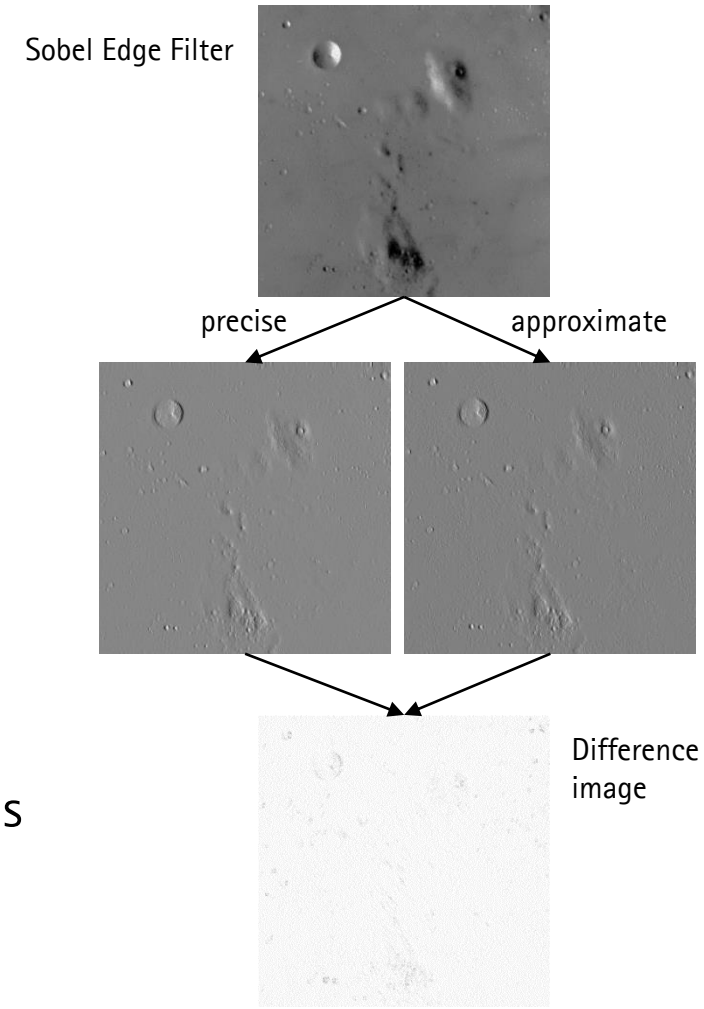
    - Not considered here



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- Pipelining of processor architectures for image processing:
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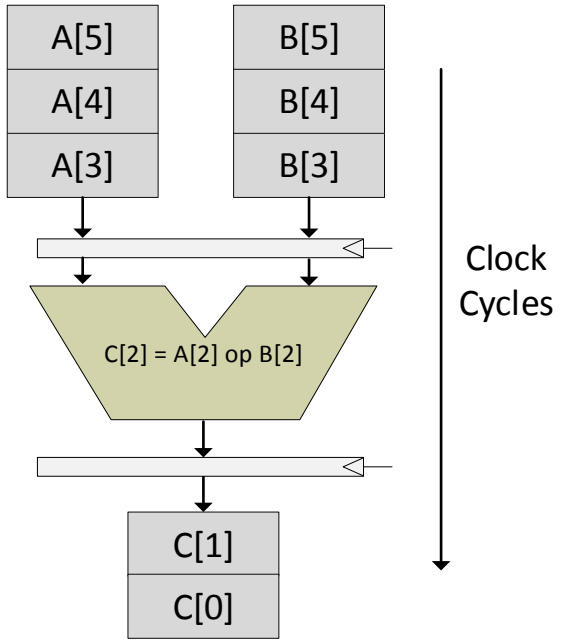

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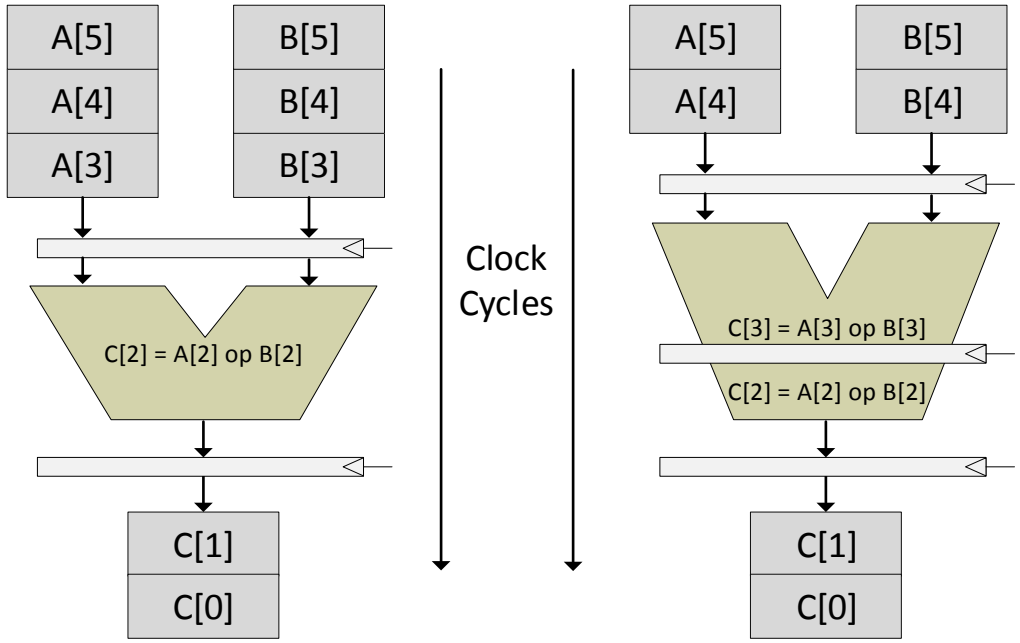

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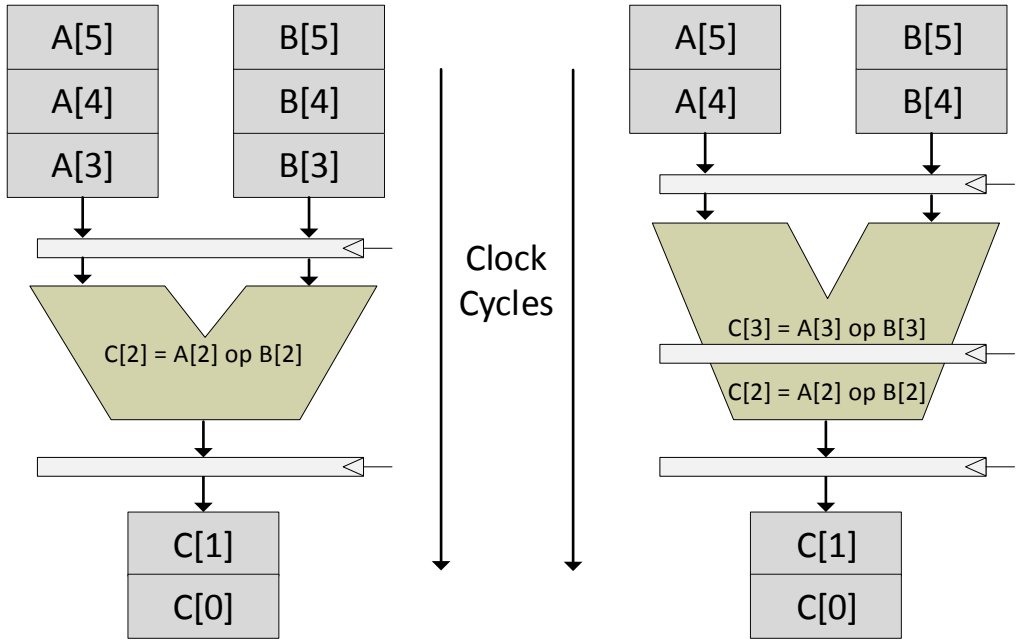

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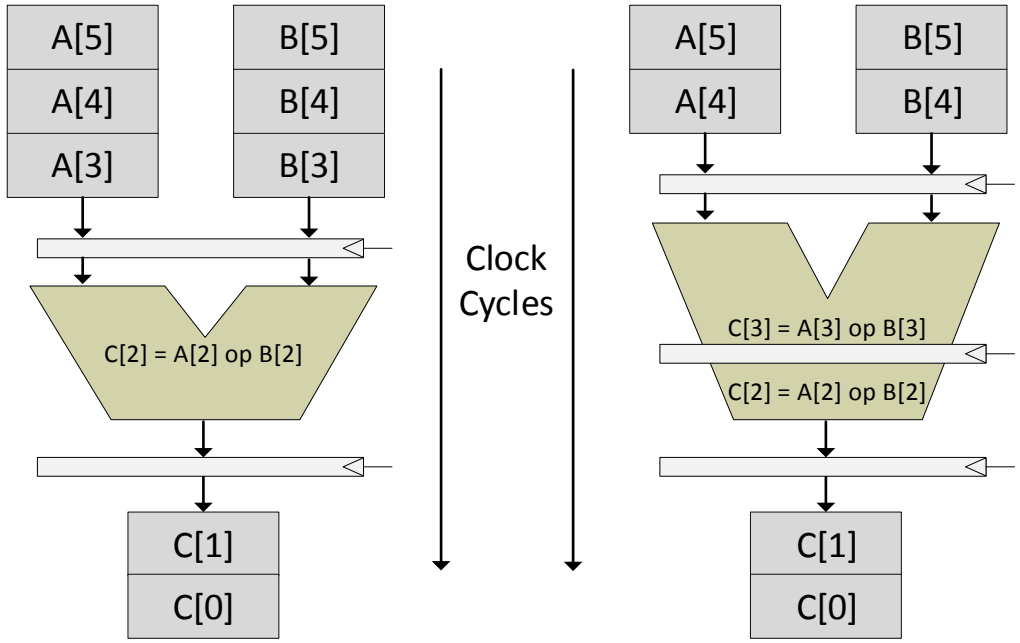
- Influence on:
  - Area Efficiency
  - Energy Efficiency
  - Needs to be explored for architectural decisions



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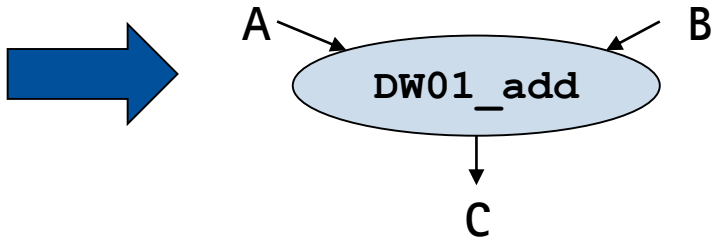

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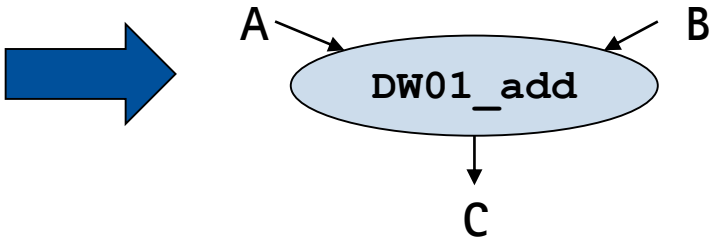

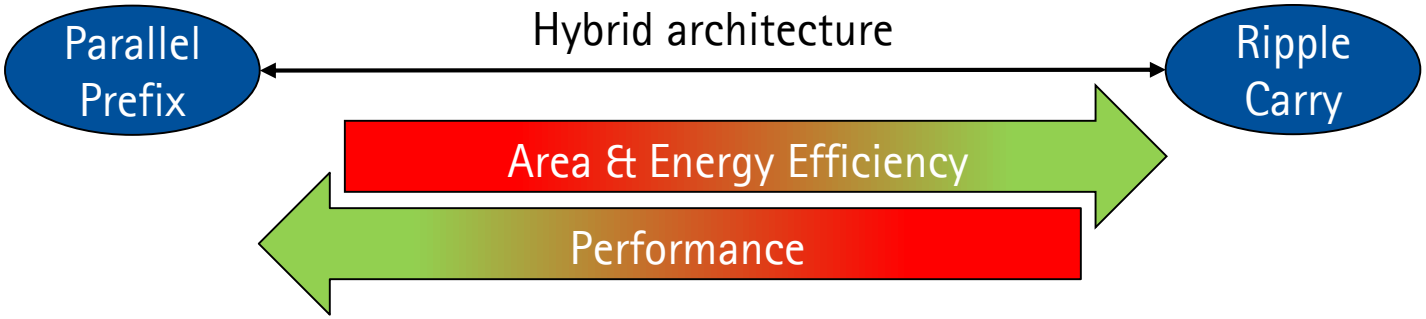

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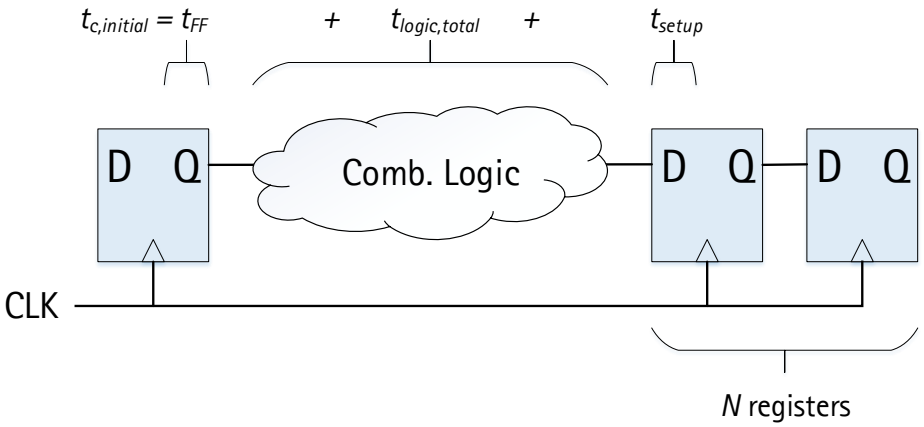

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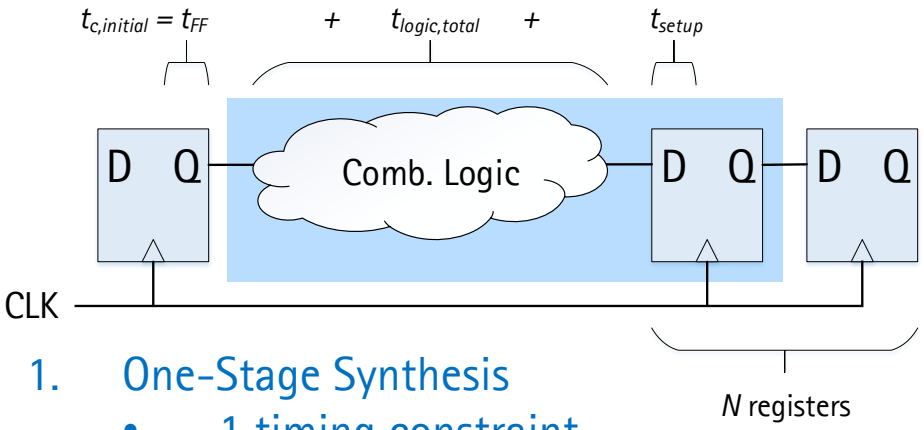

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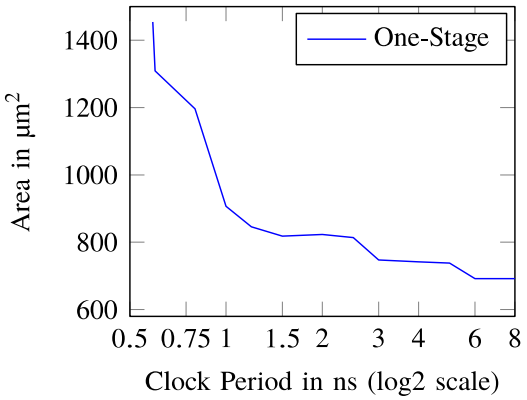

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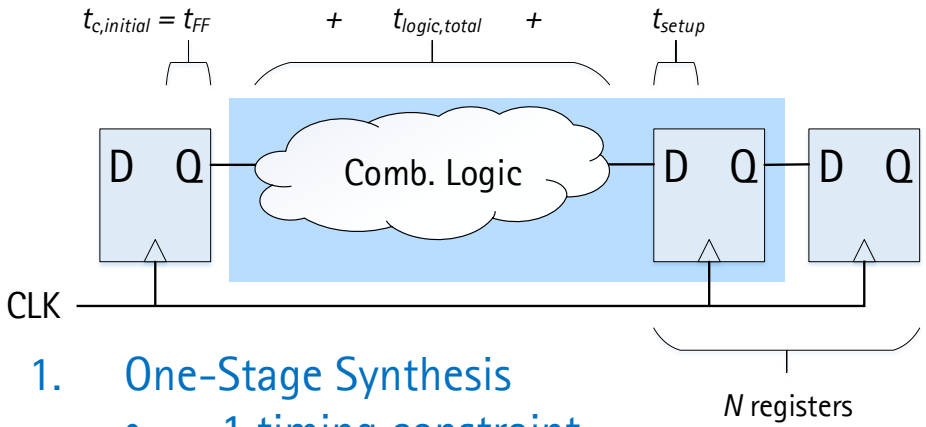

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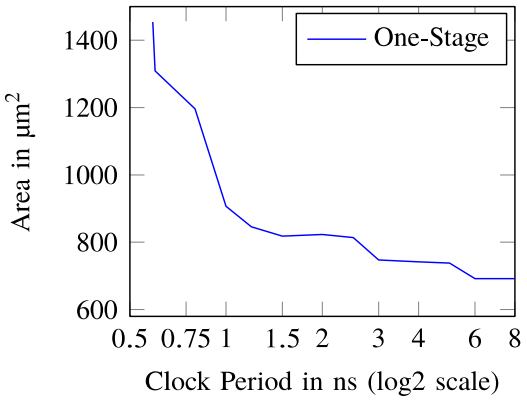

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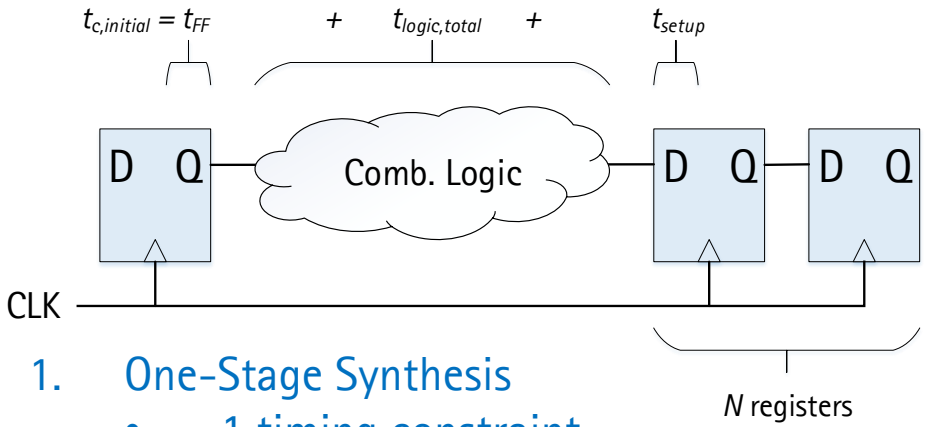

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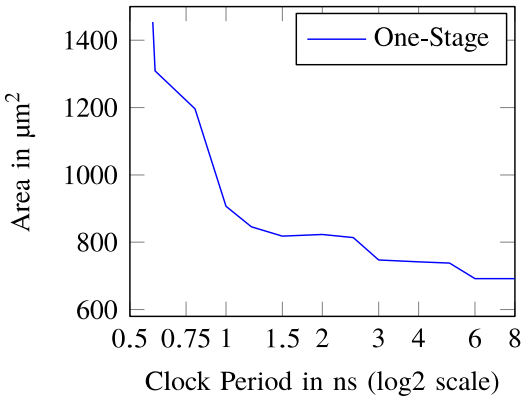

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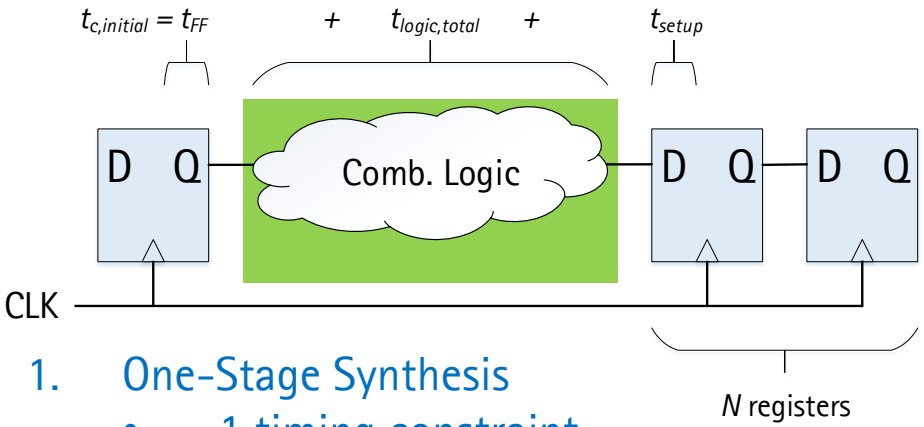

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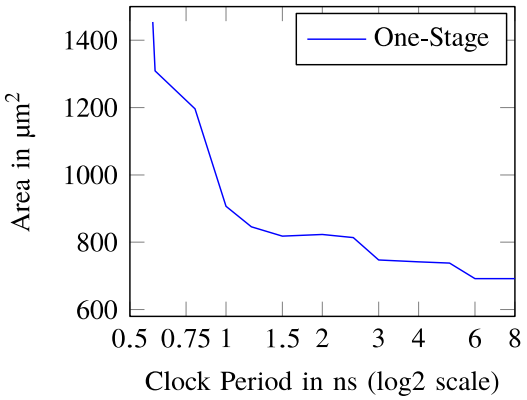

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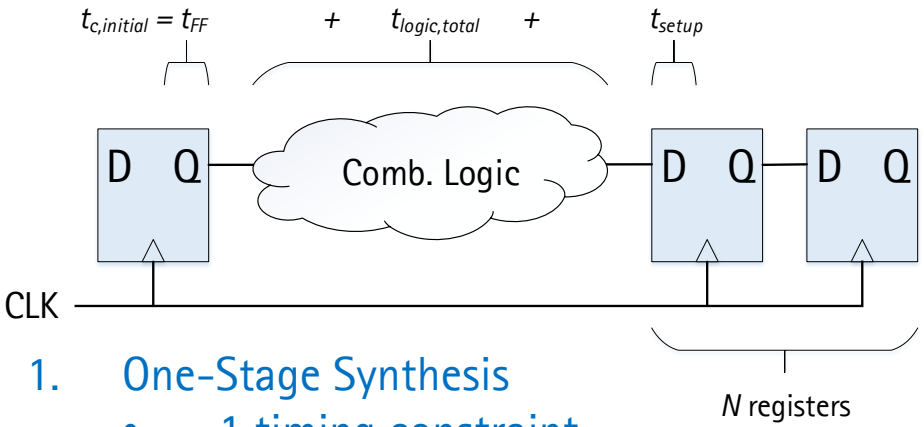

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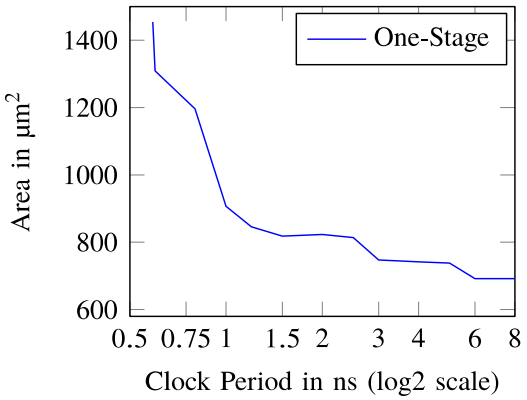

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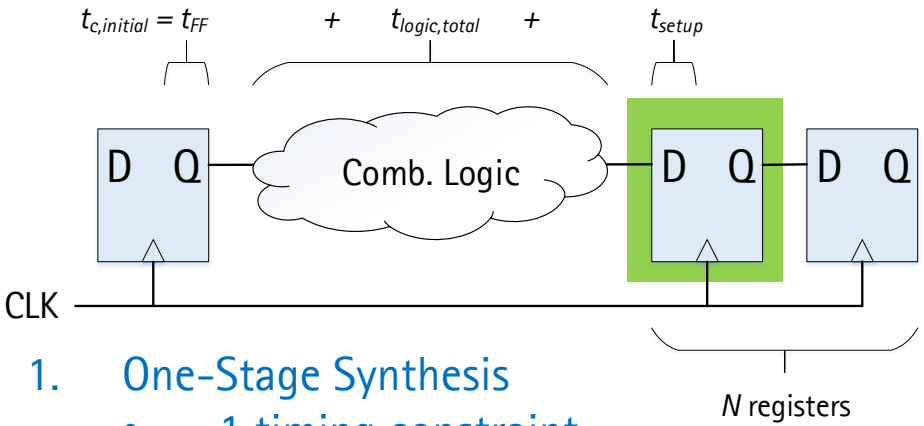

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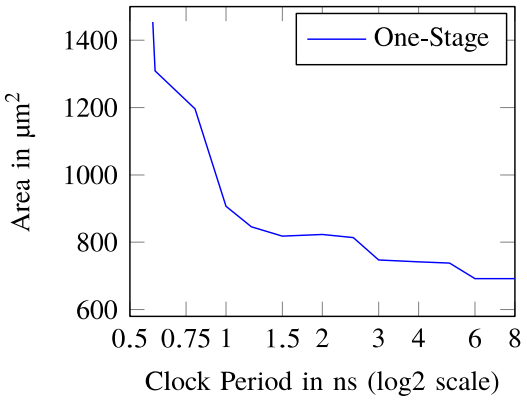

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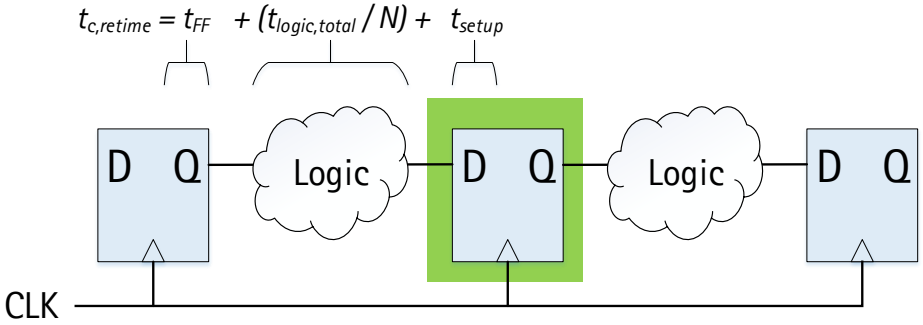

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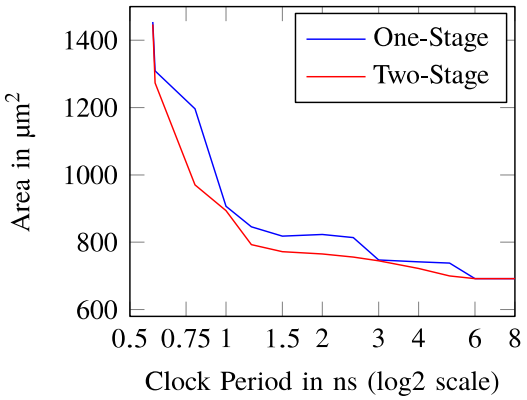

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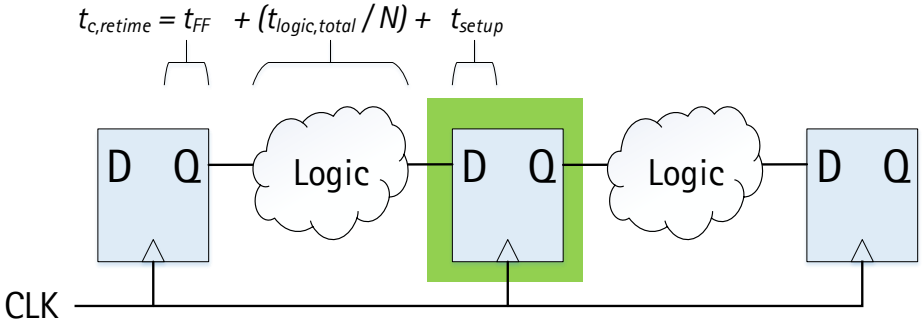

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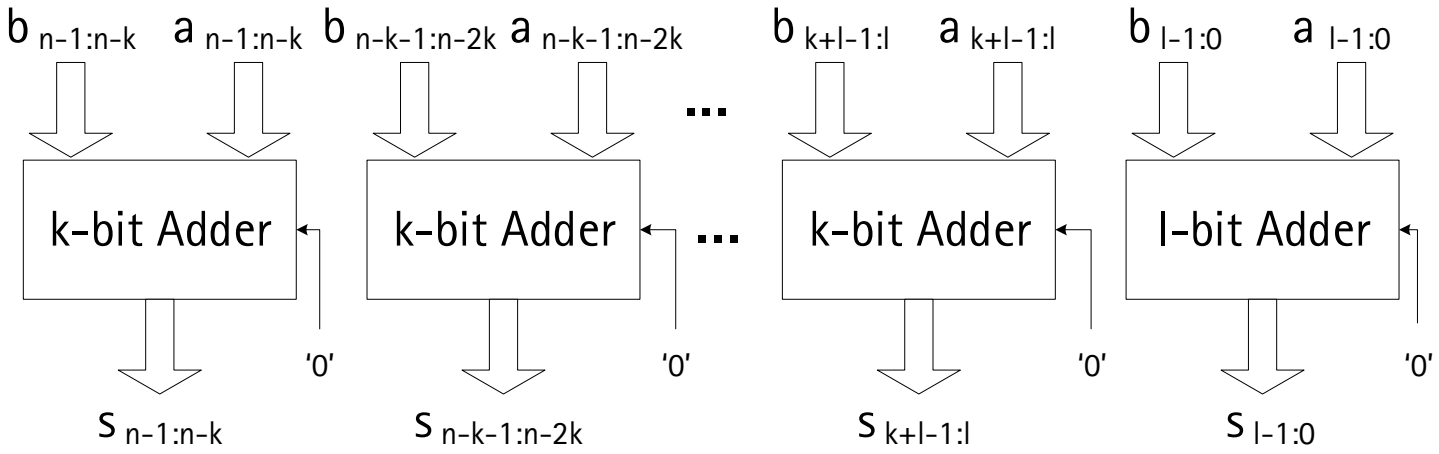

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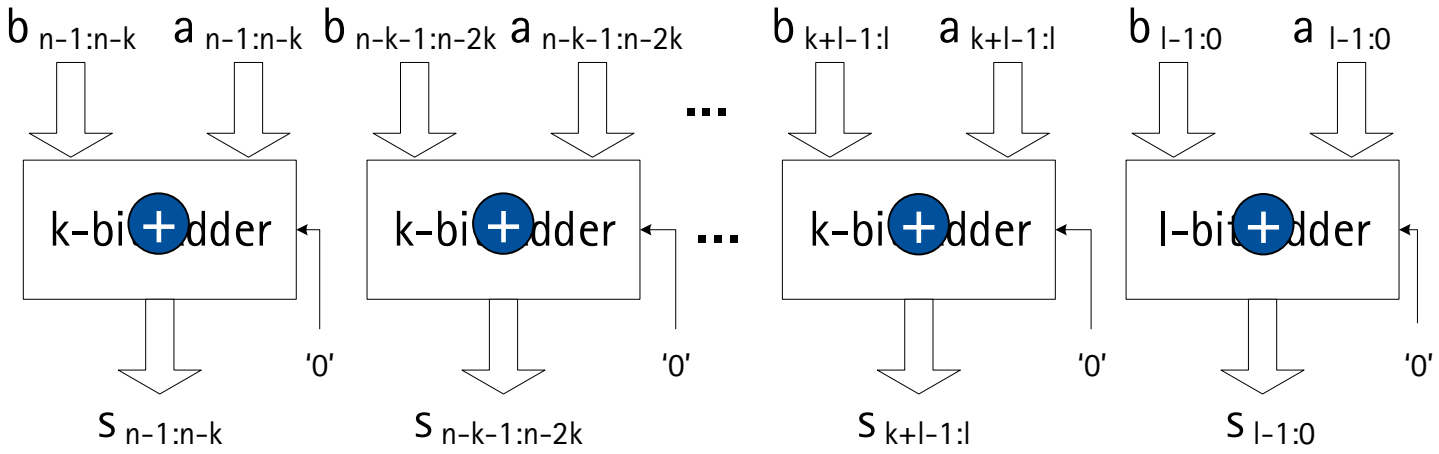

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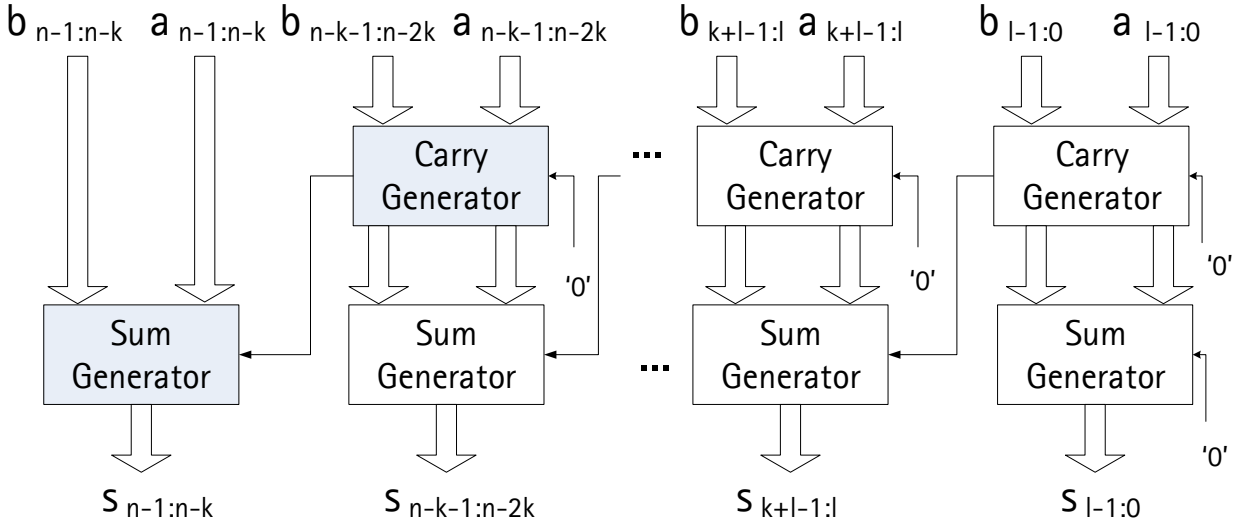

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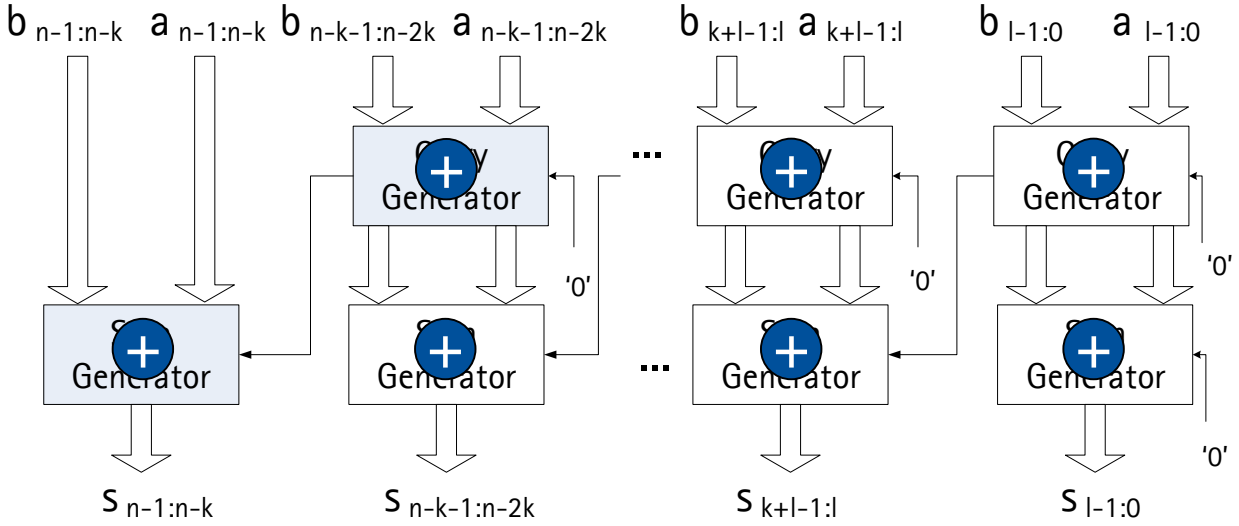

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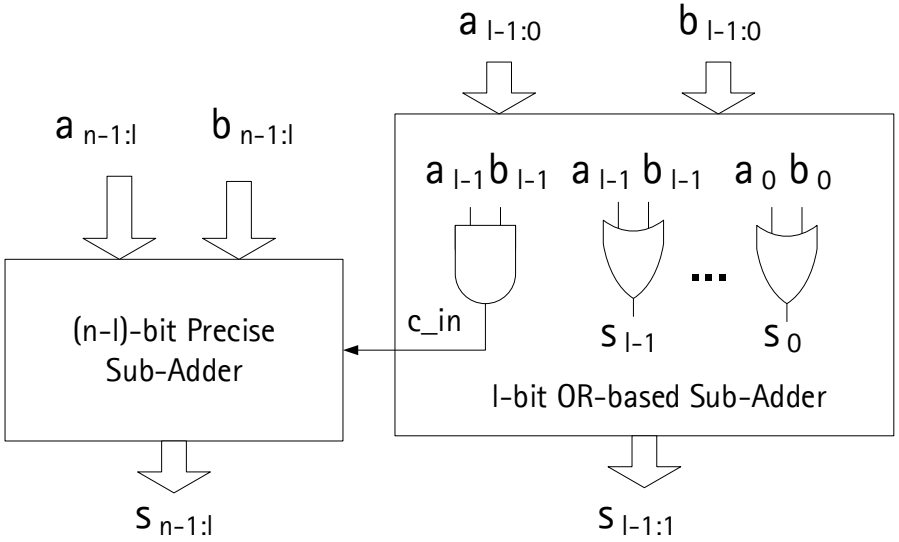

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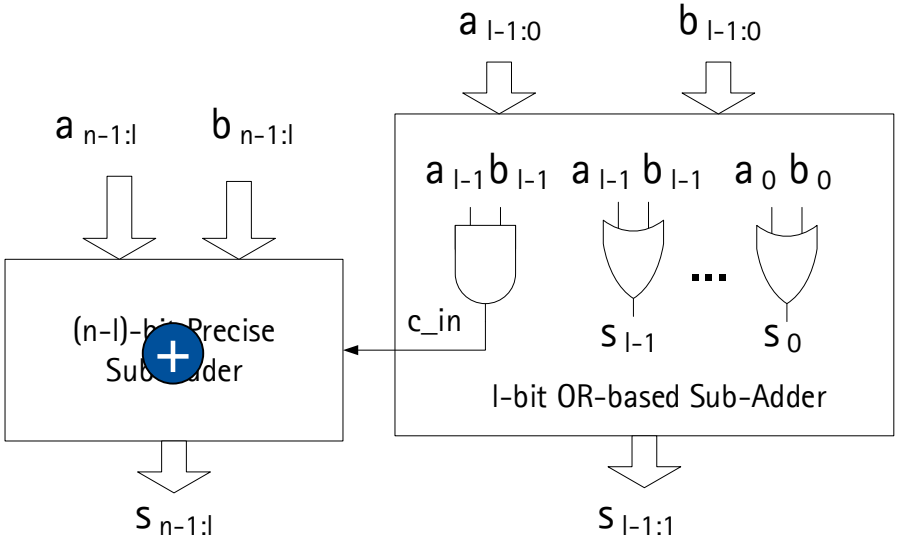

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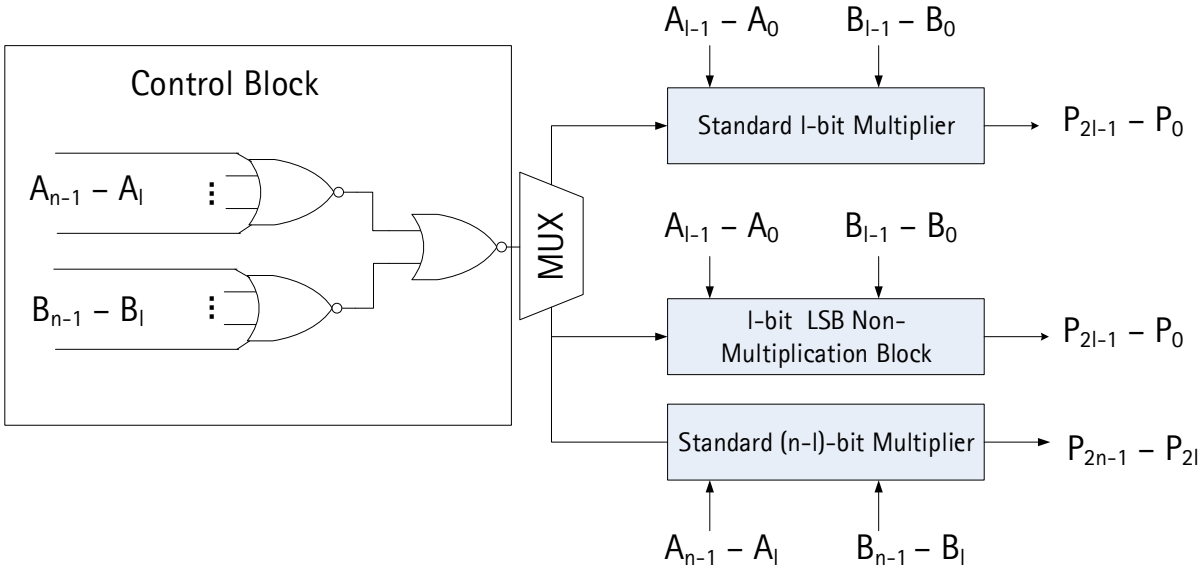

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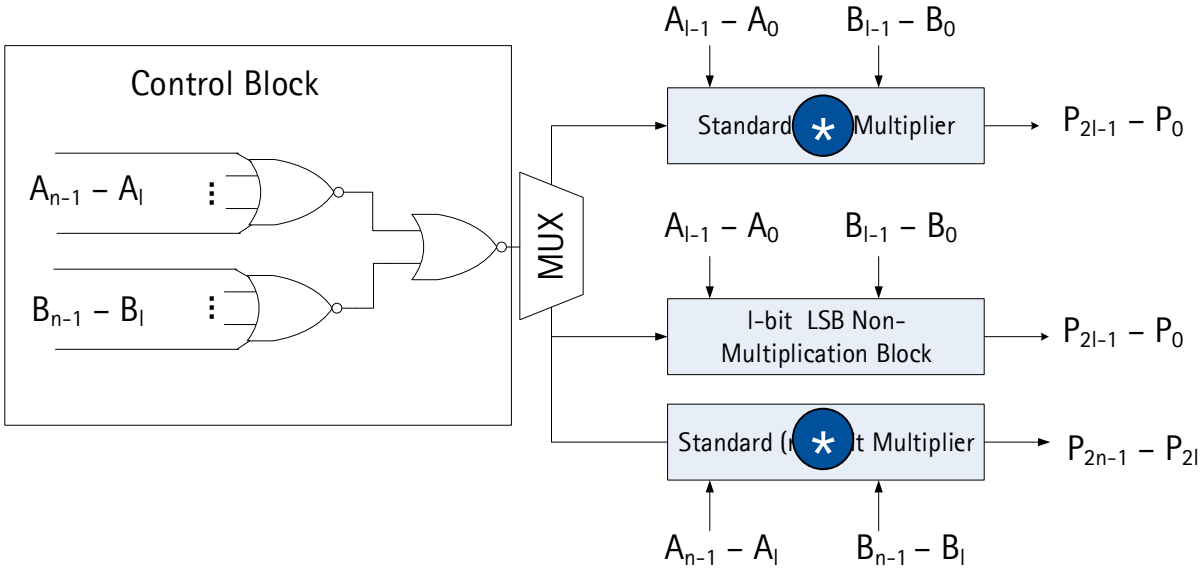

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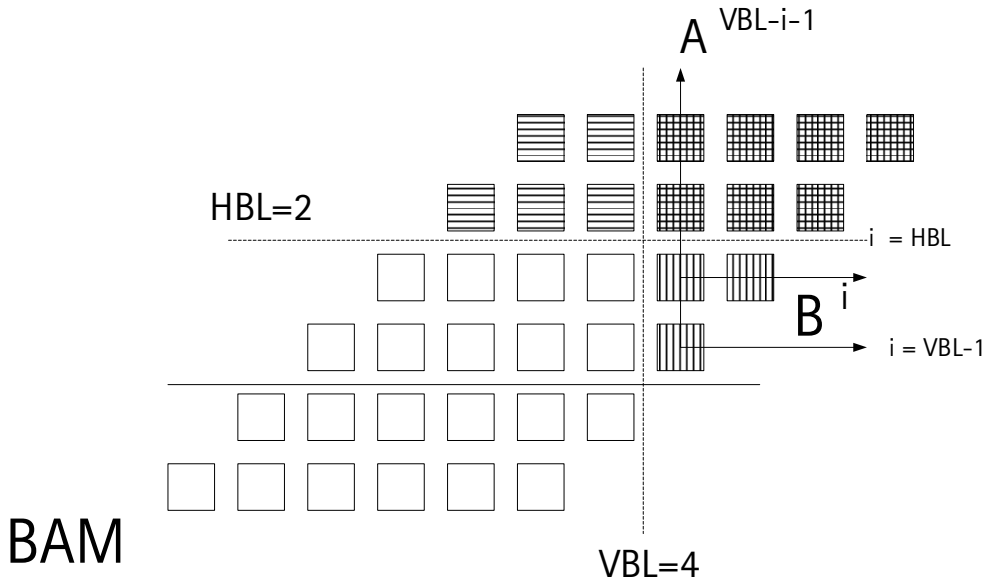

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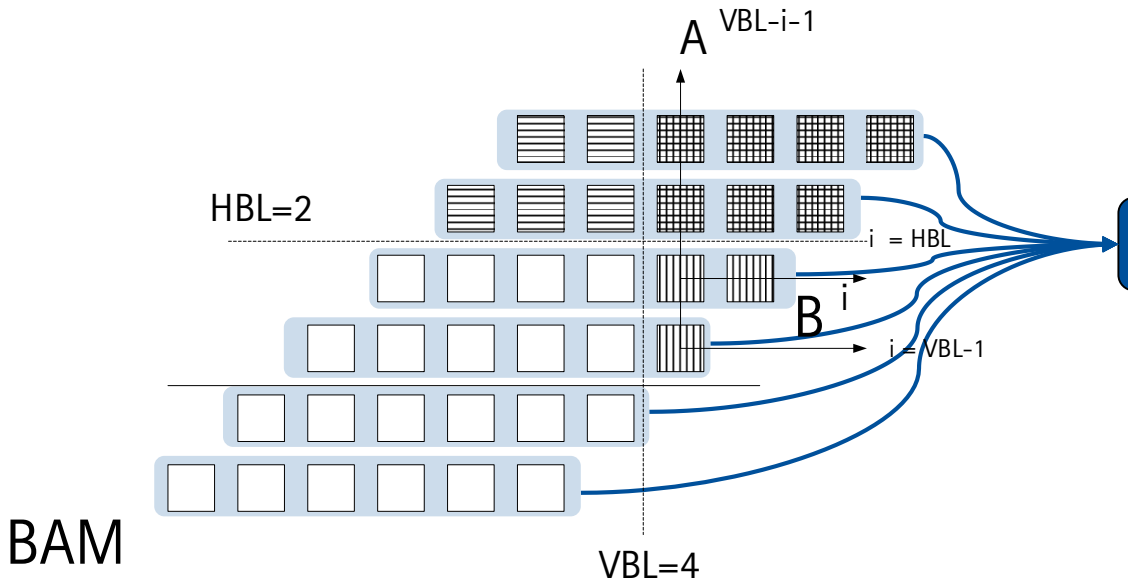

DWF_sum

Synopsys Design Compiler:
DesignWare library function for implementing an optimized carry-save adder tree

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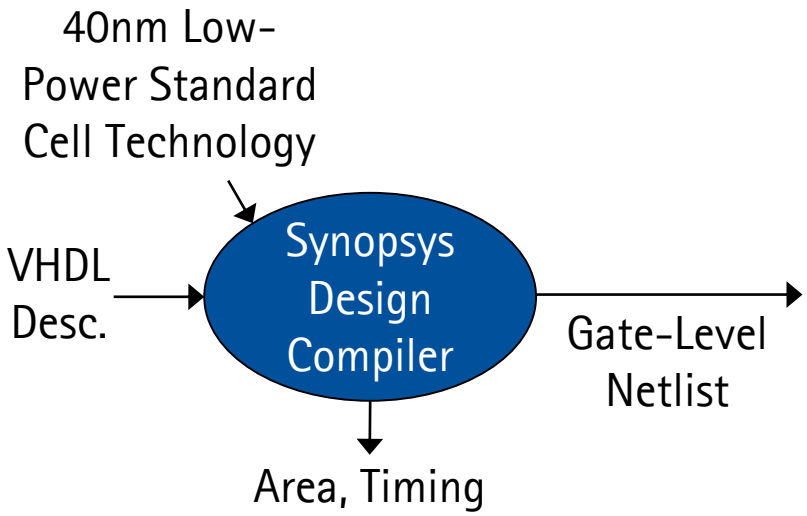

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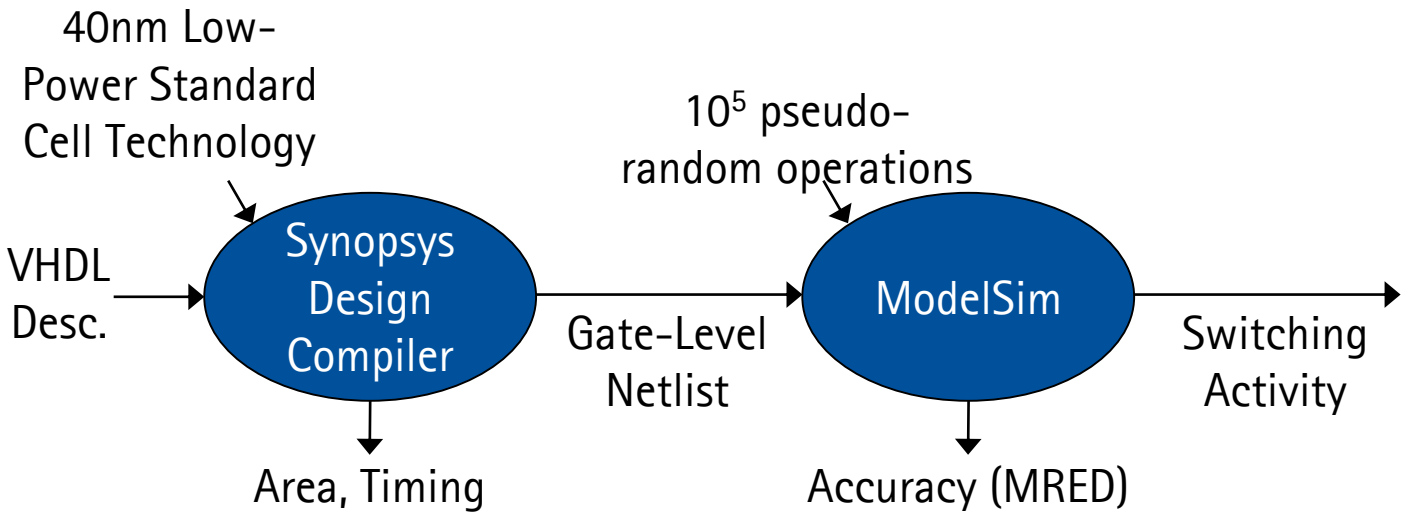

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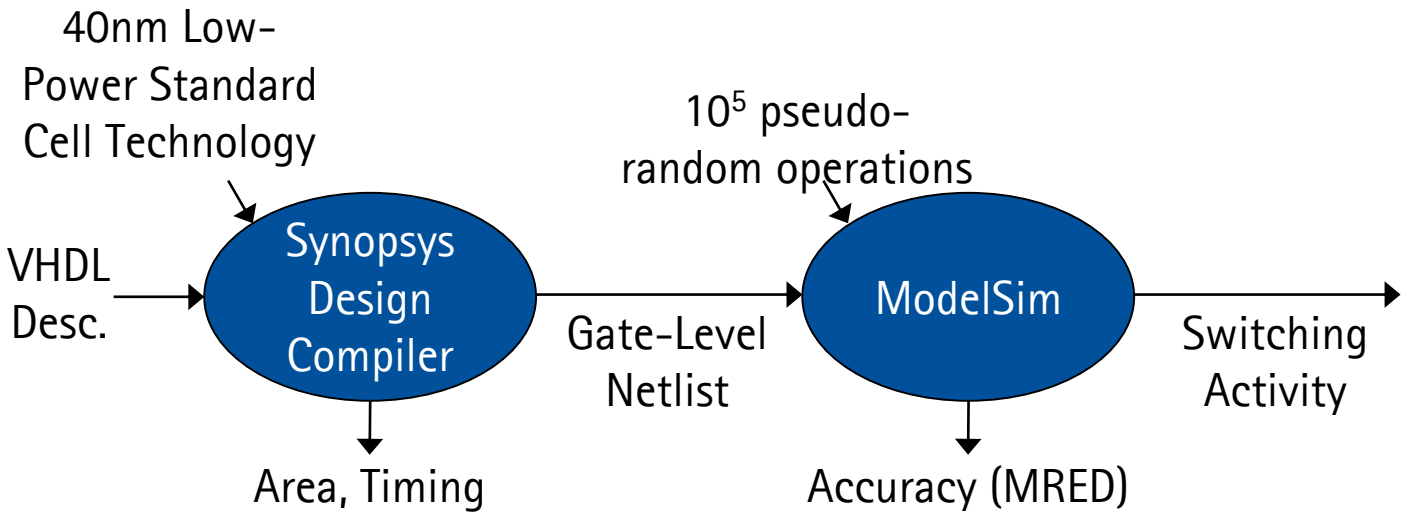

Relative Error Distance

$$\mathrm{RED} = \frac{|M' - M|}{M}$$

M	Precise Result
M'	Approximate Result
n	Bitwidth
N	Number of pseudo-random operations

Mean Relative Error Distance

$$\mathrm{MRED} = E[\mathrm{RED}] = \frac{1}{2^{-2n}} \sum_{i=0}^{2^n-1} \sum_{j=0}^{2^n-1} \frac{|M'_{ij} - M_{ij}|}{M_{ij}} \approx \frac{1}{N} \sum_{i=0}^{N-1} \frac{|M'_i - M_i|}{M_i}$$

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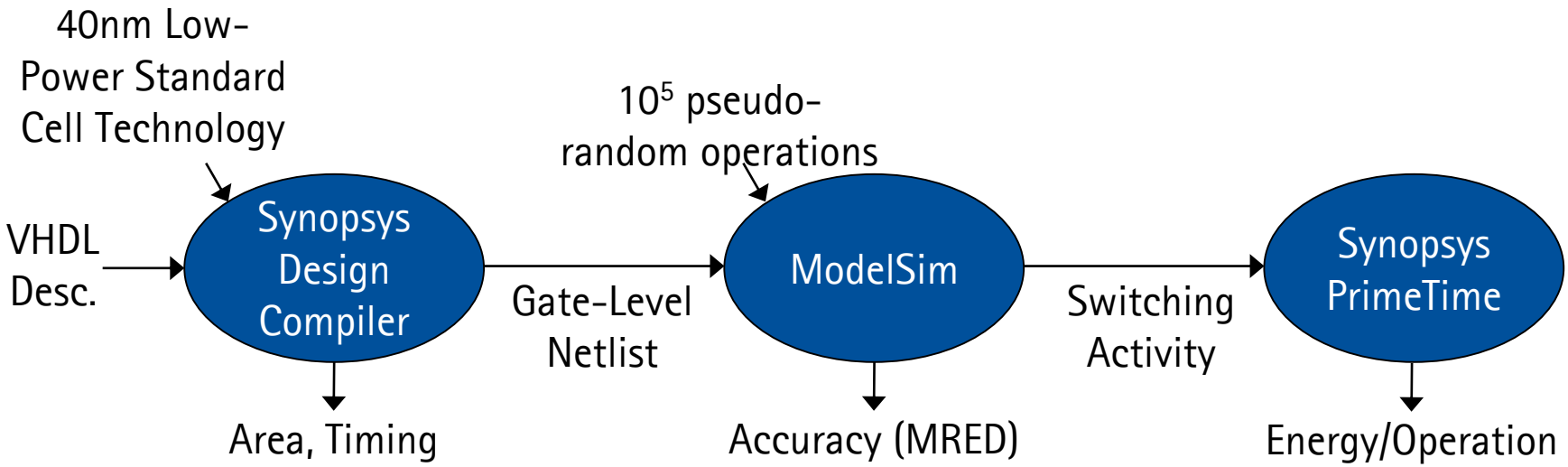

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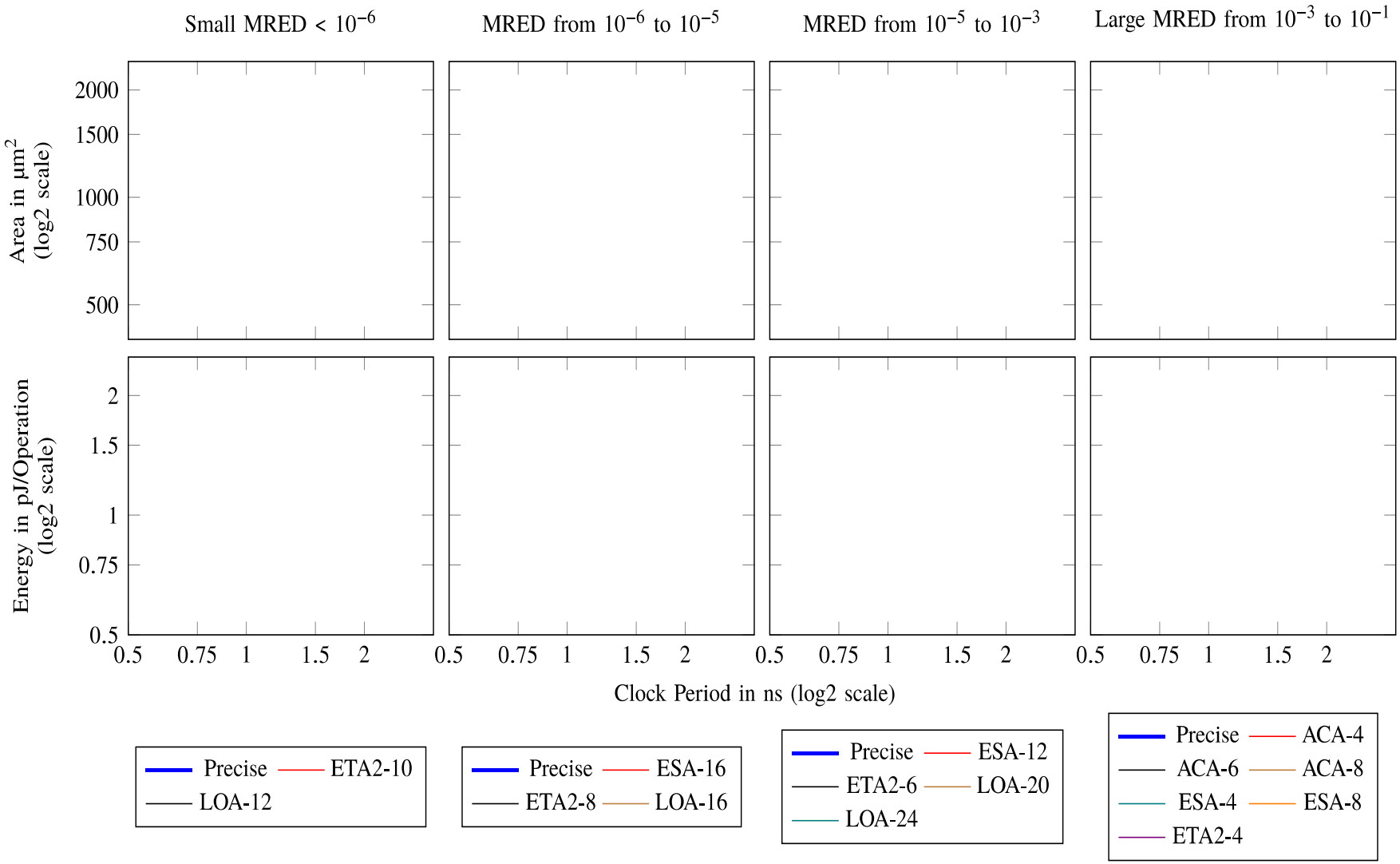

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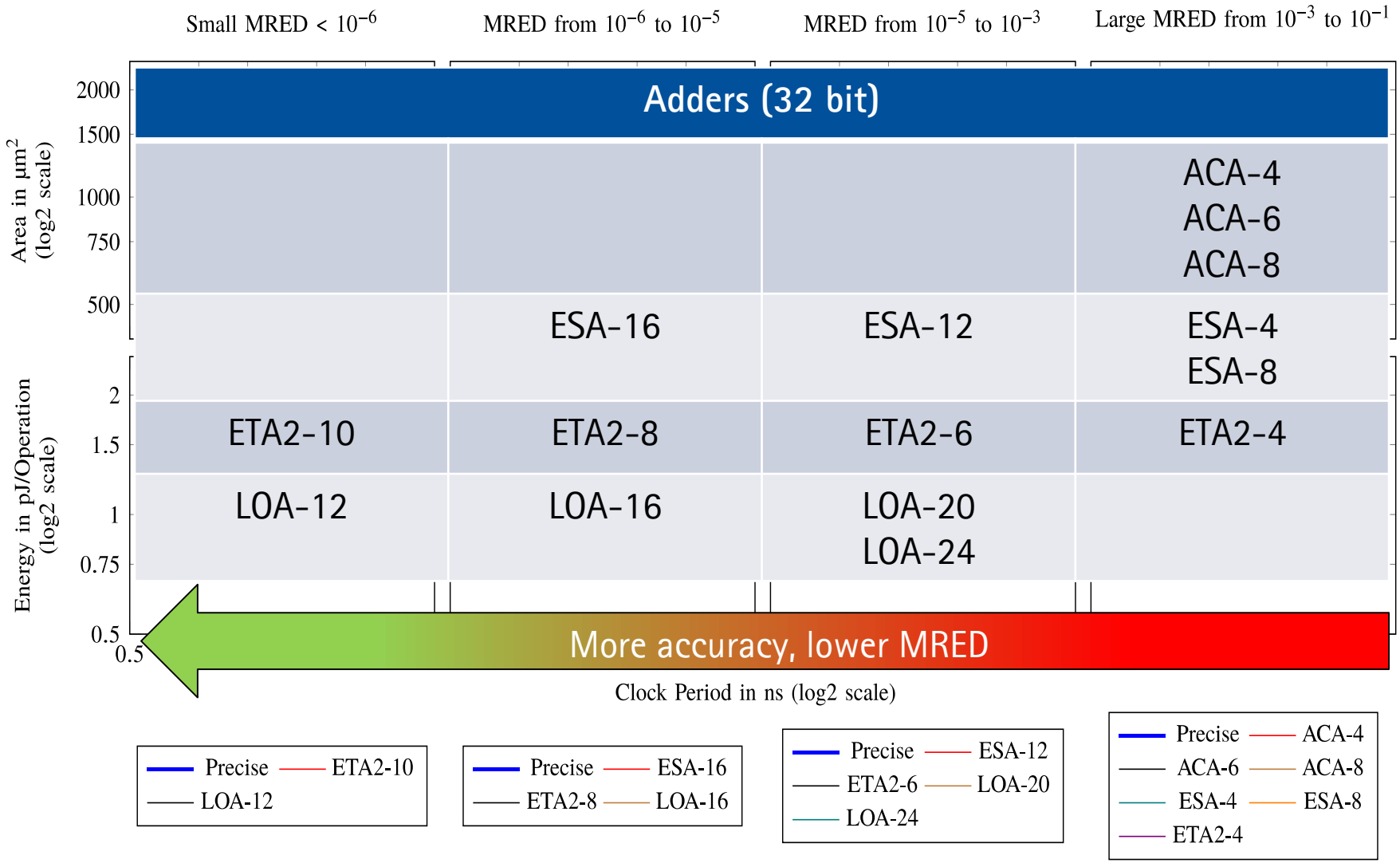

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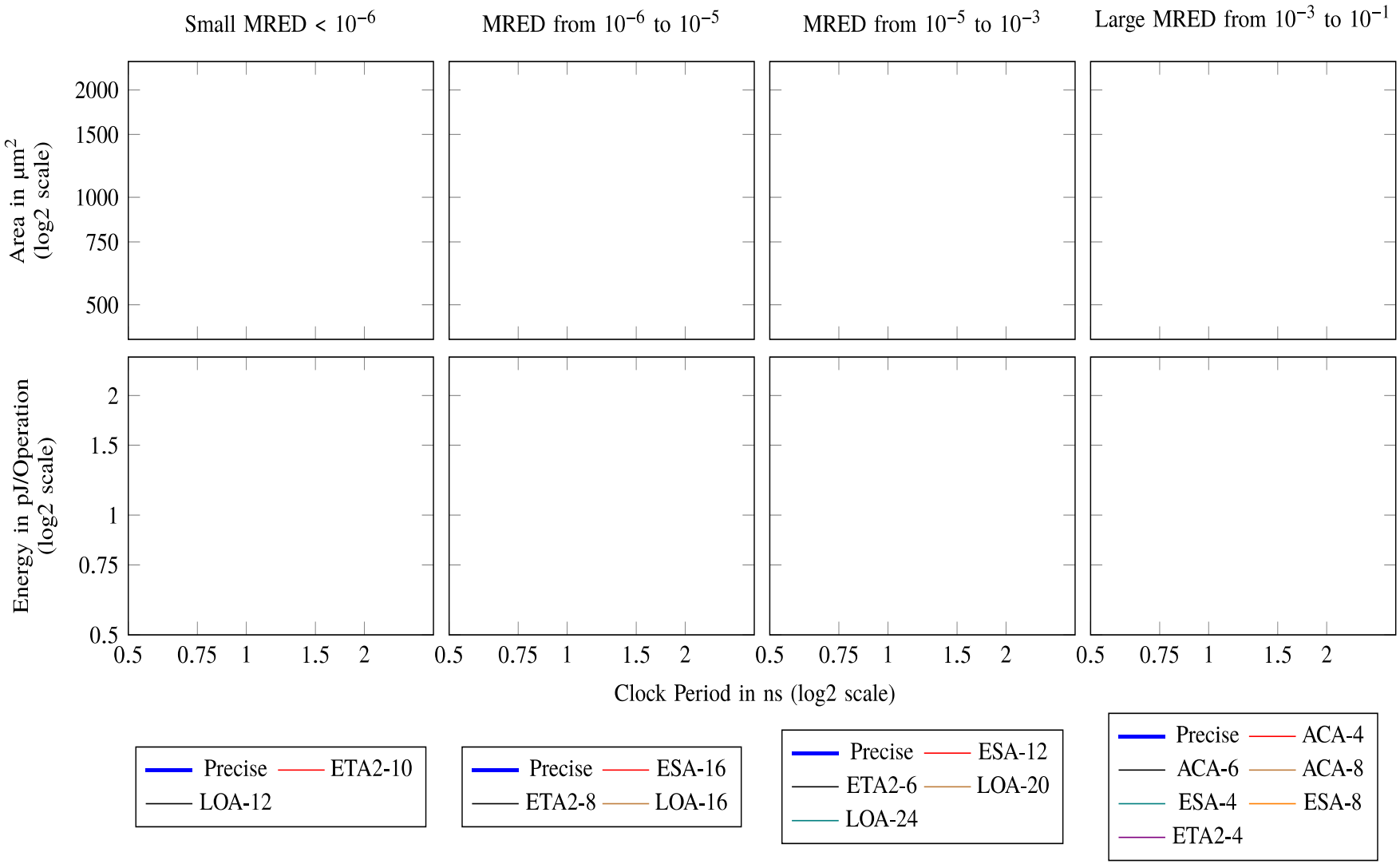

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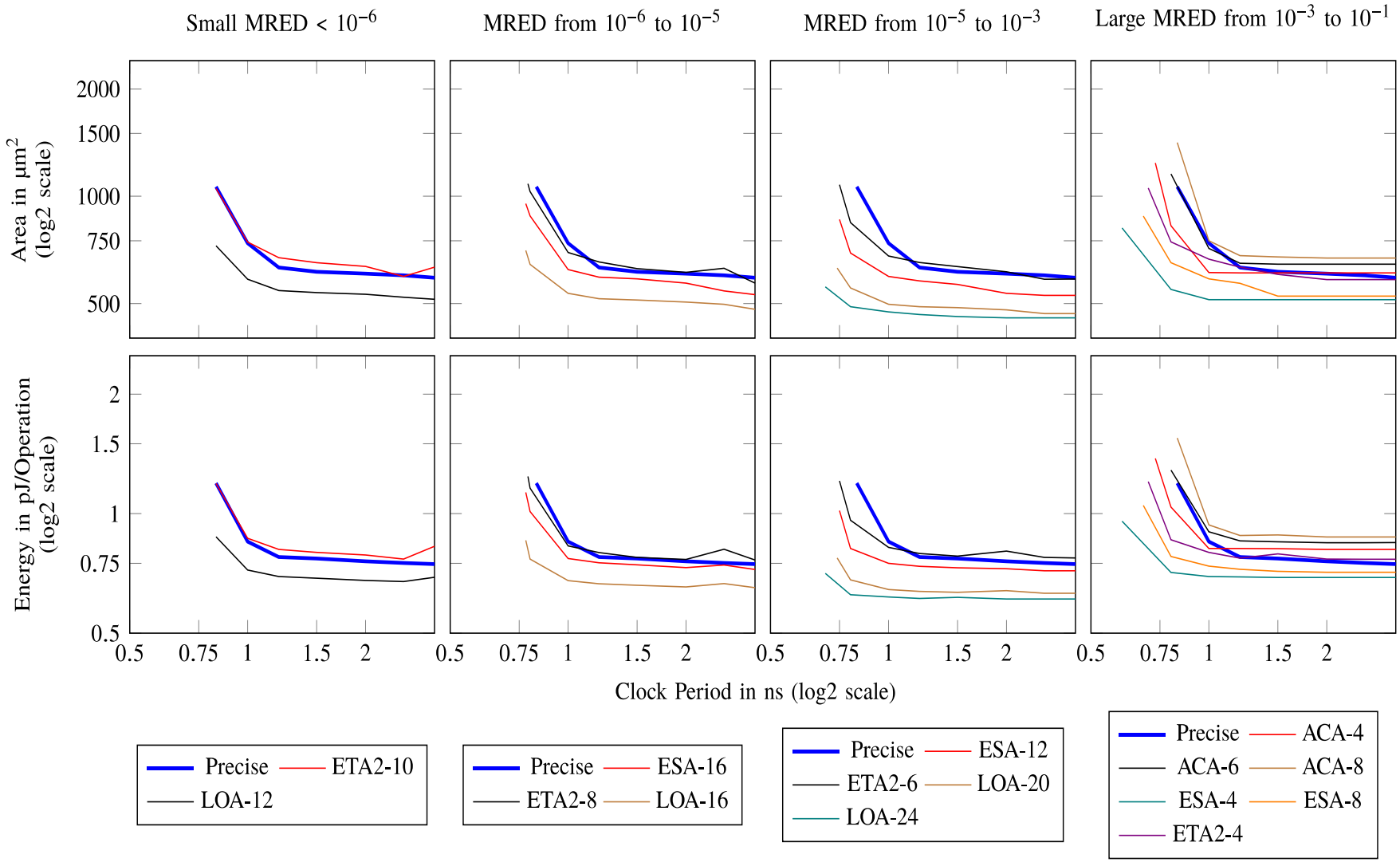

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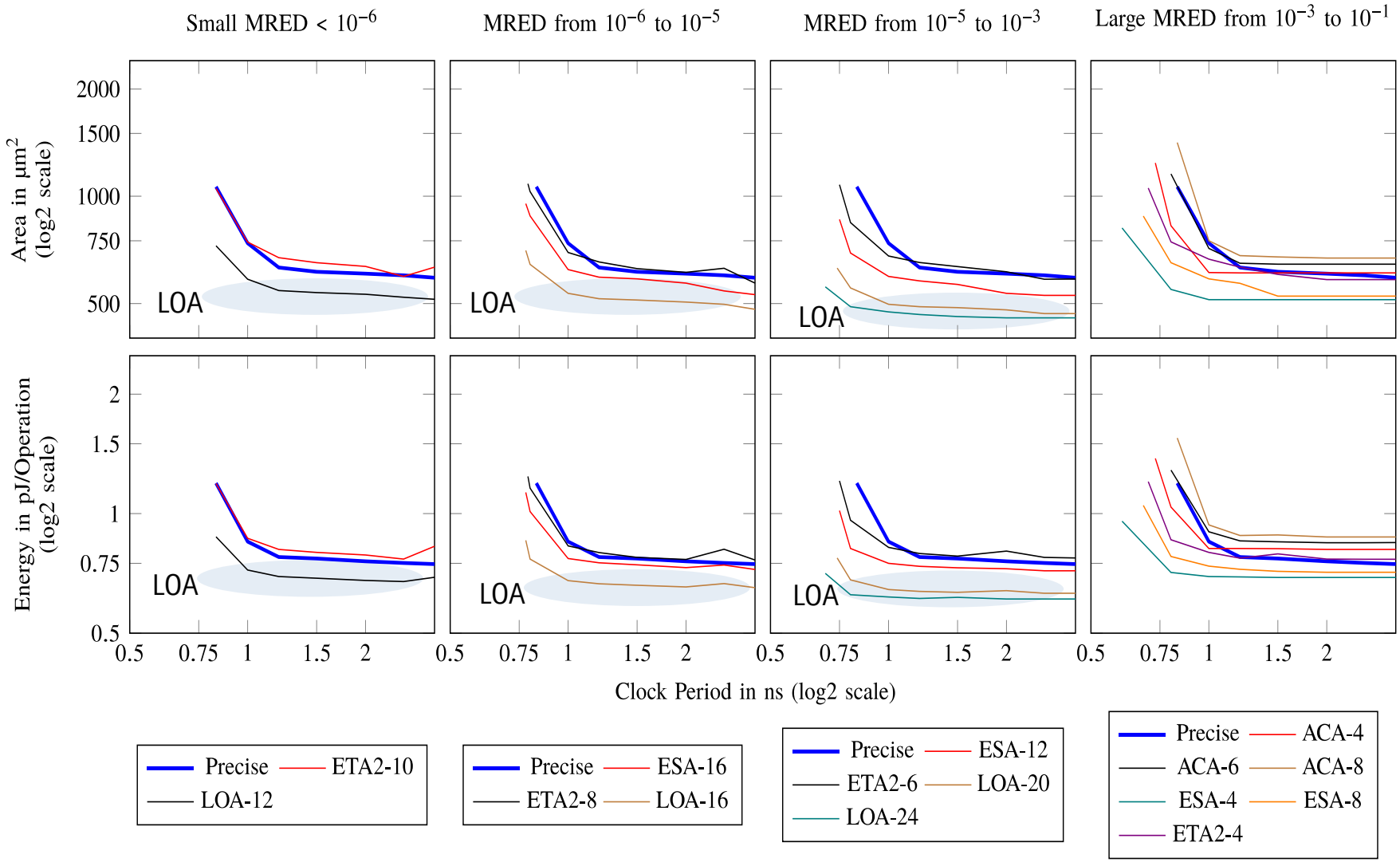

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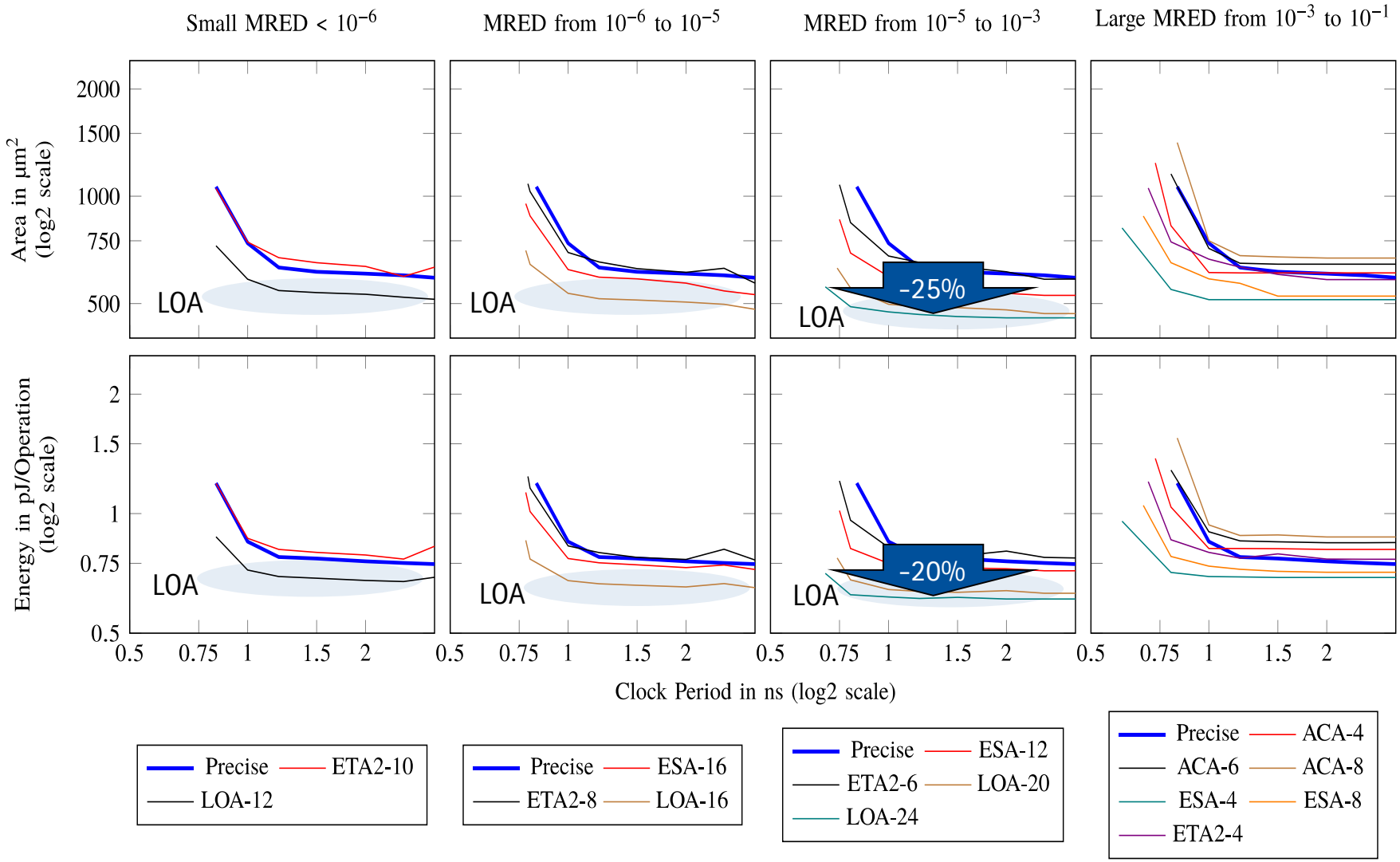

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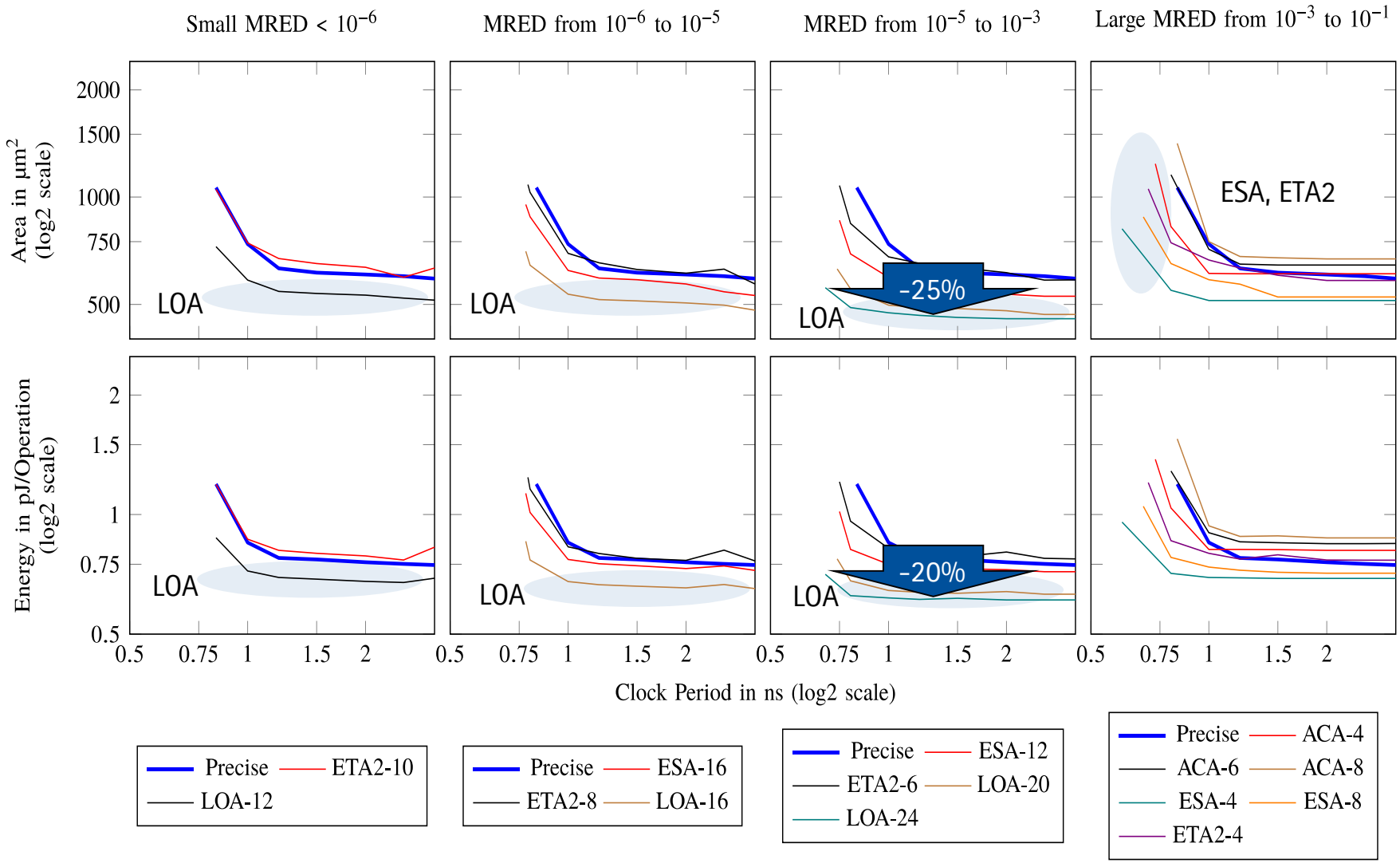

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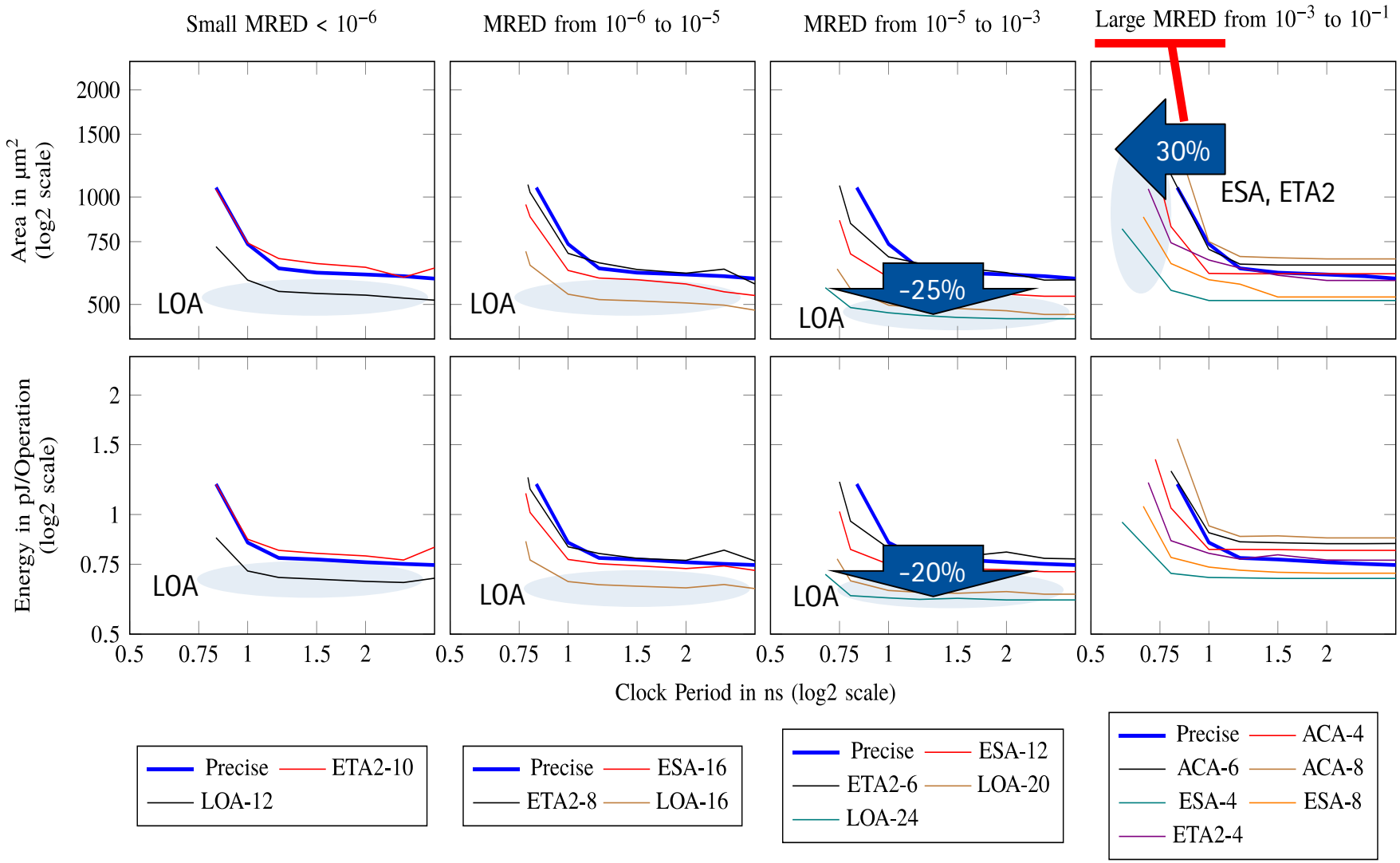

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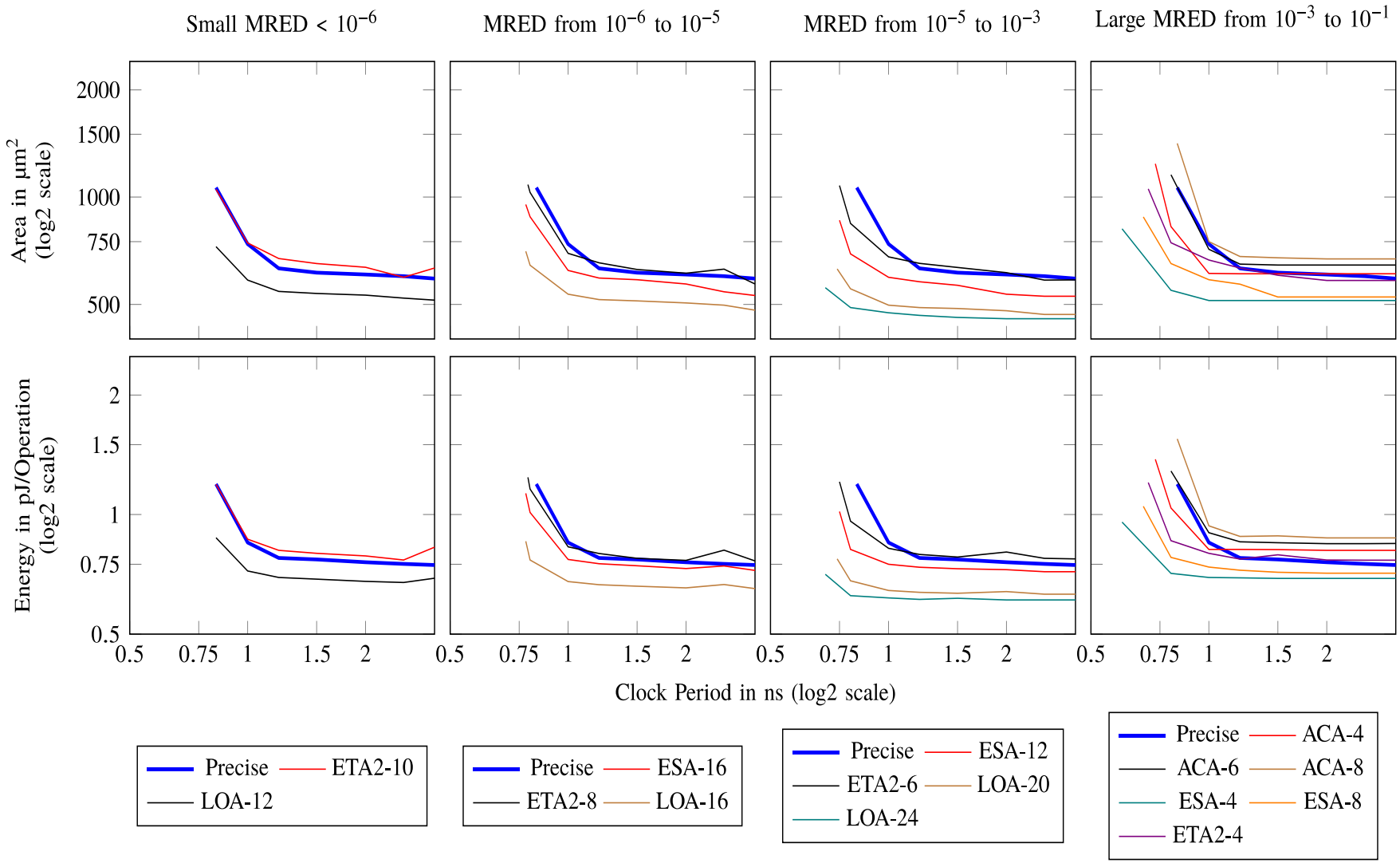

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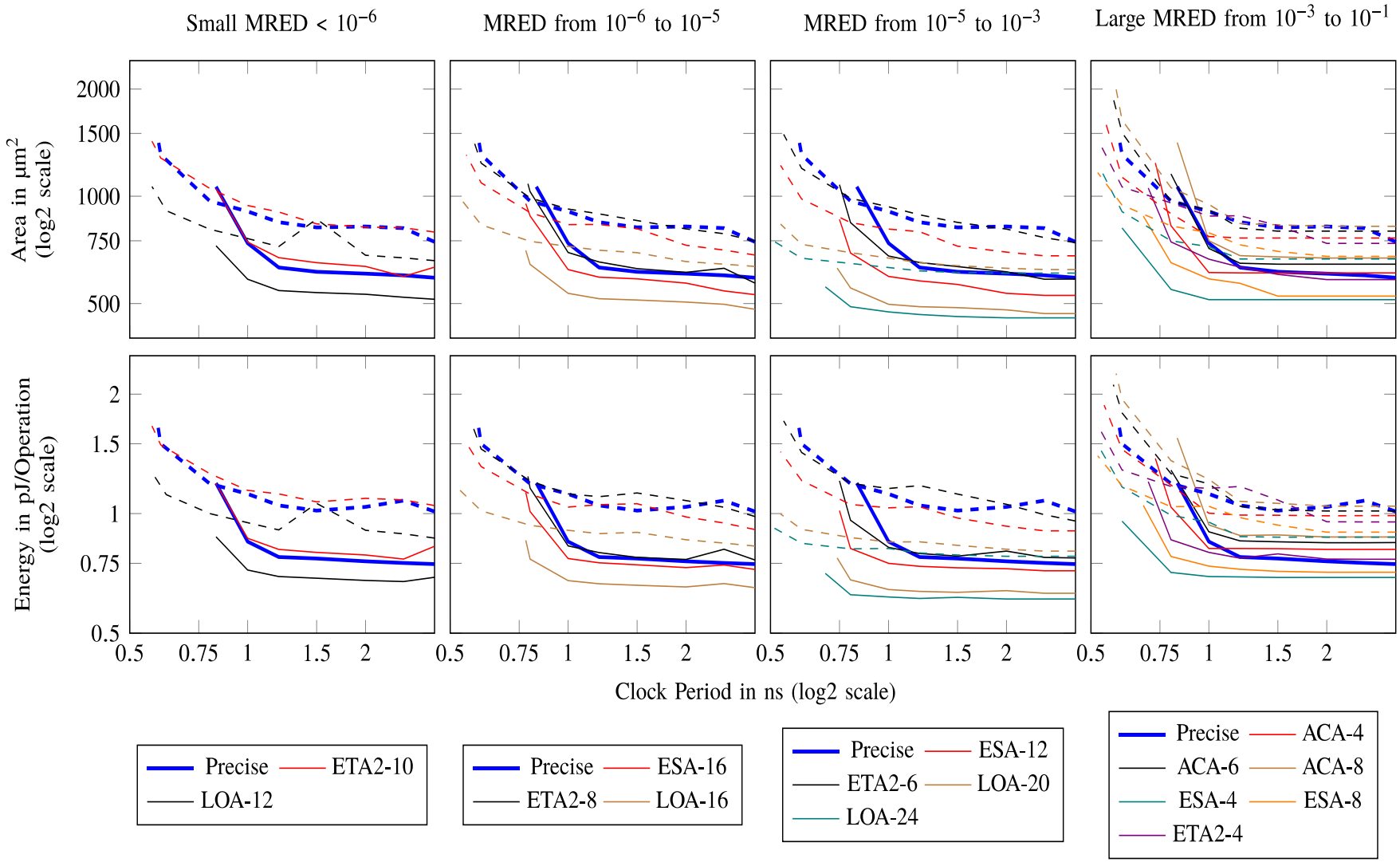

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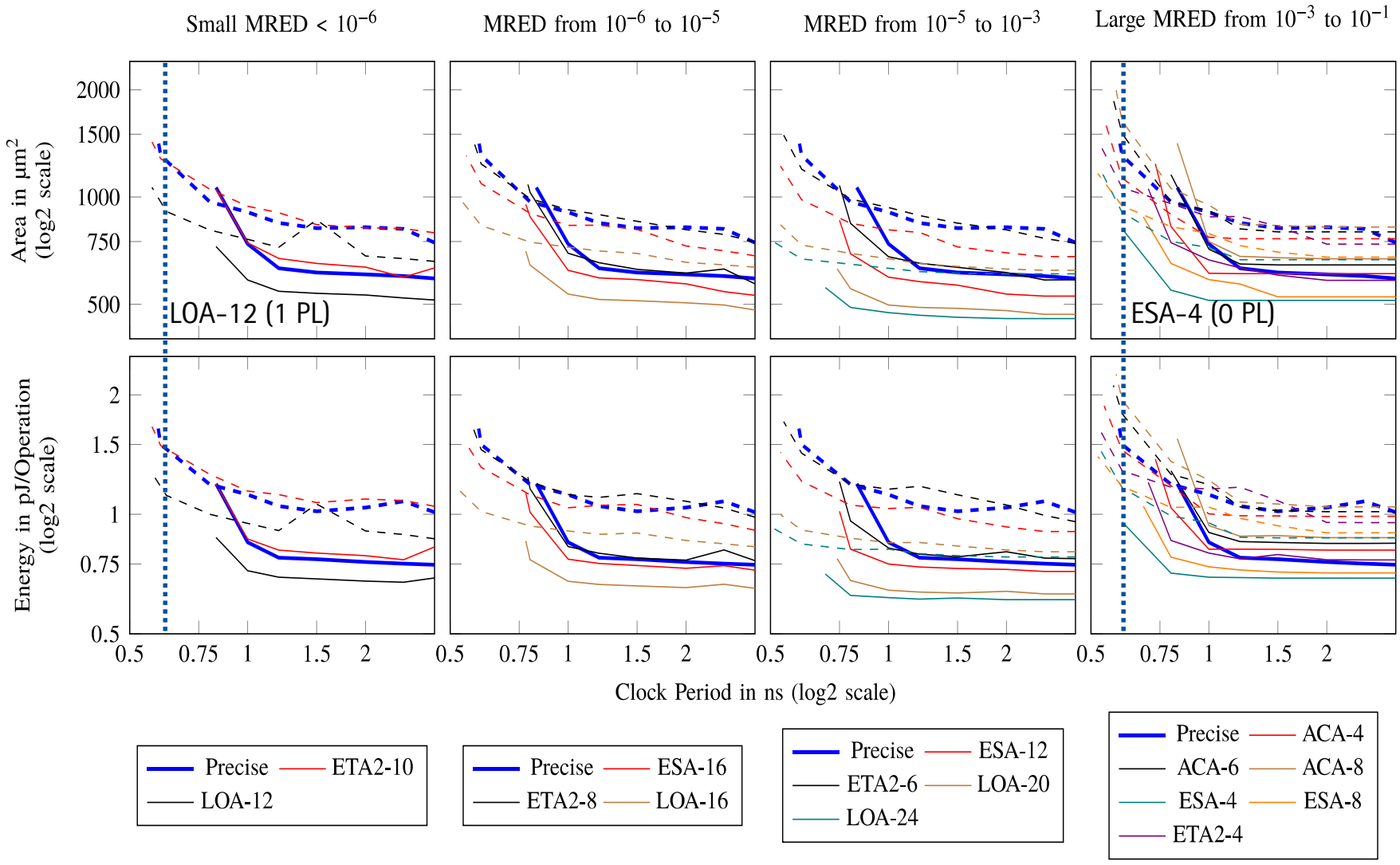

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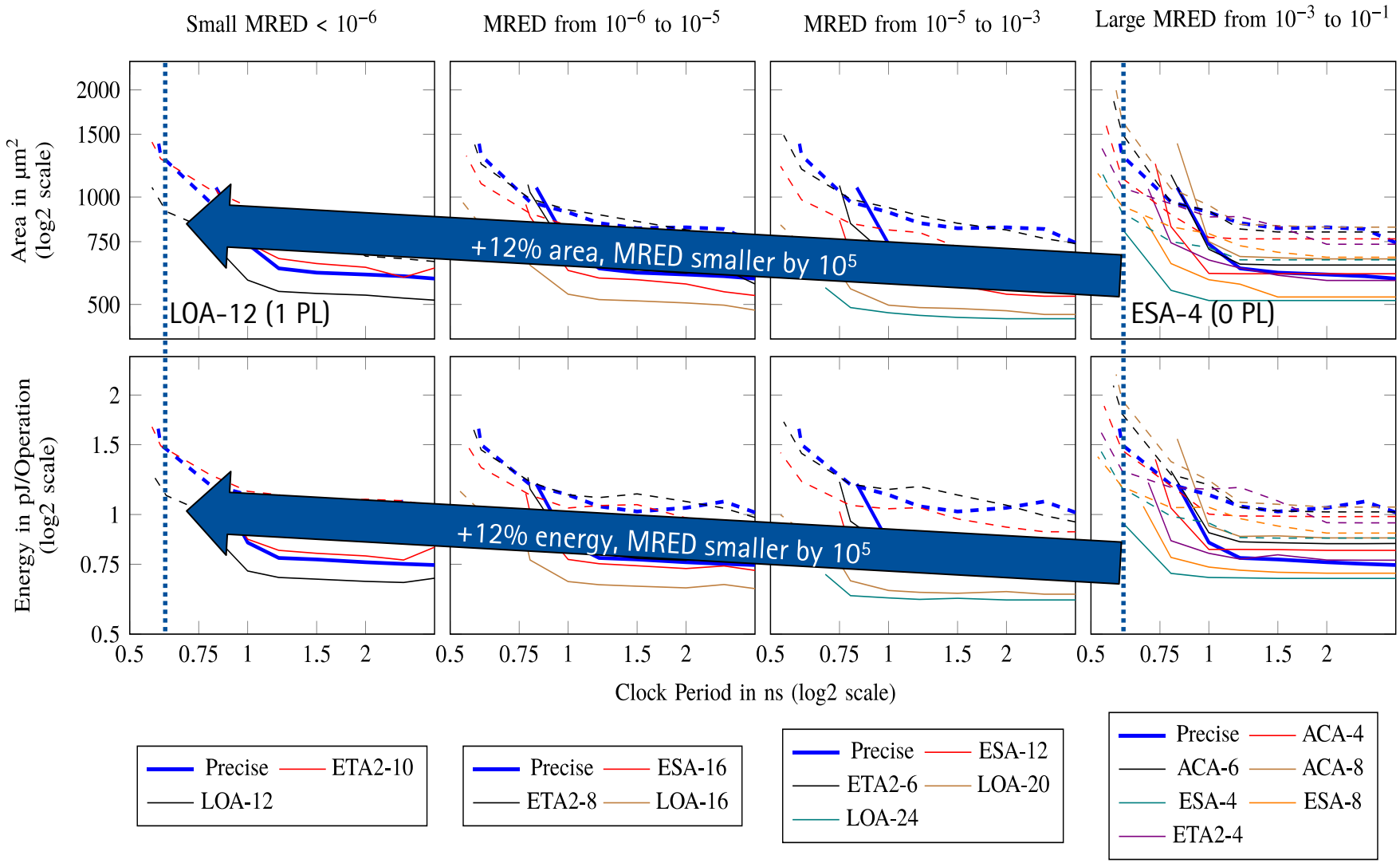

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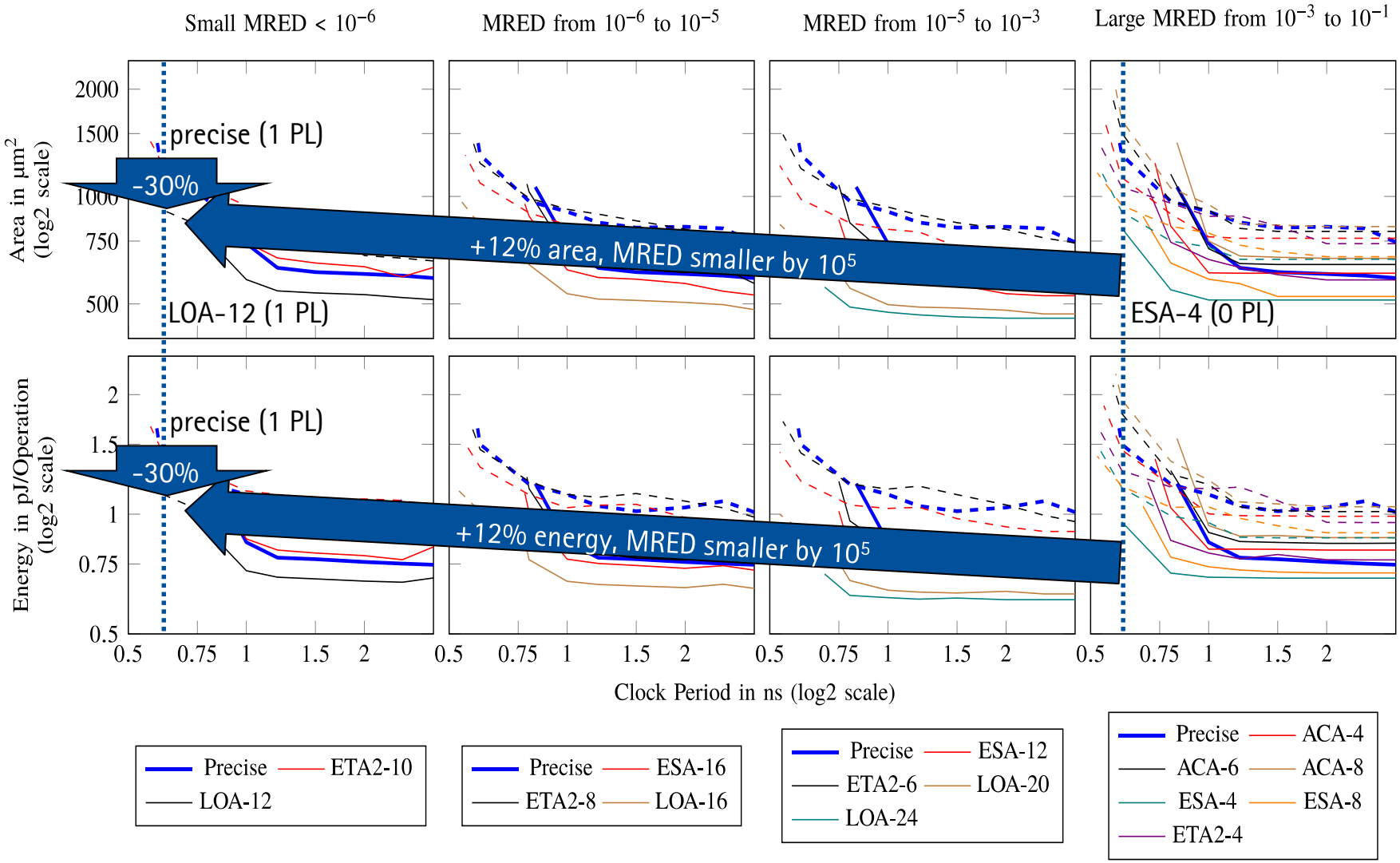

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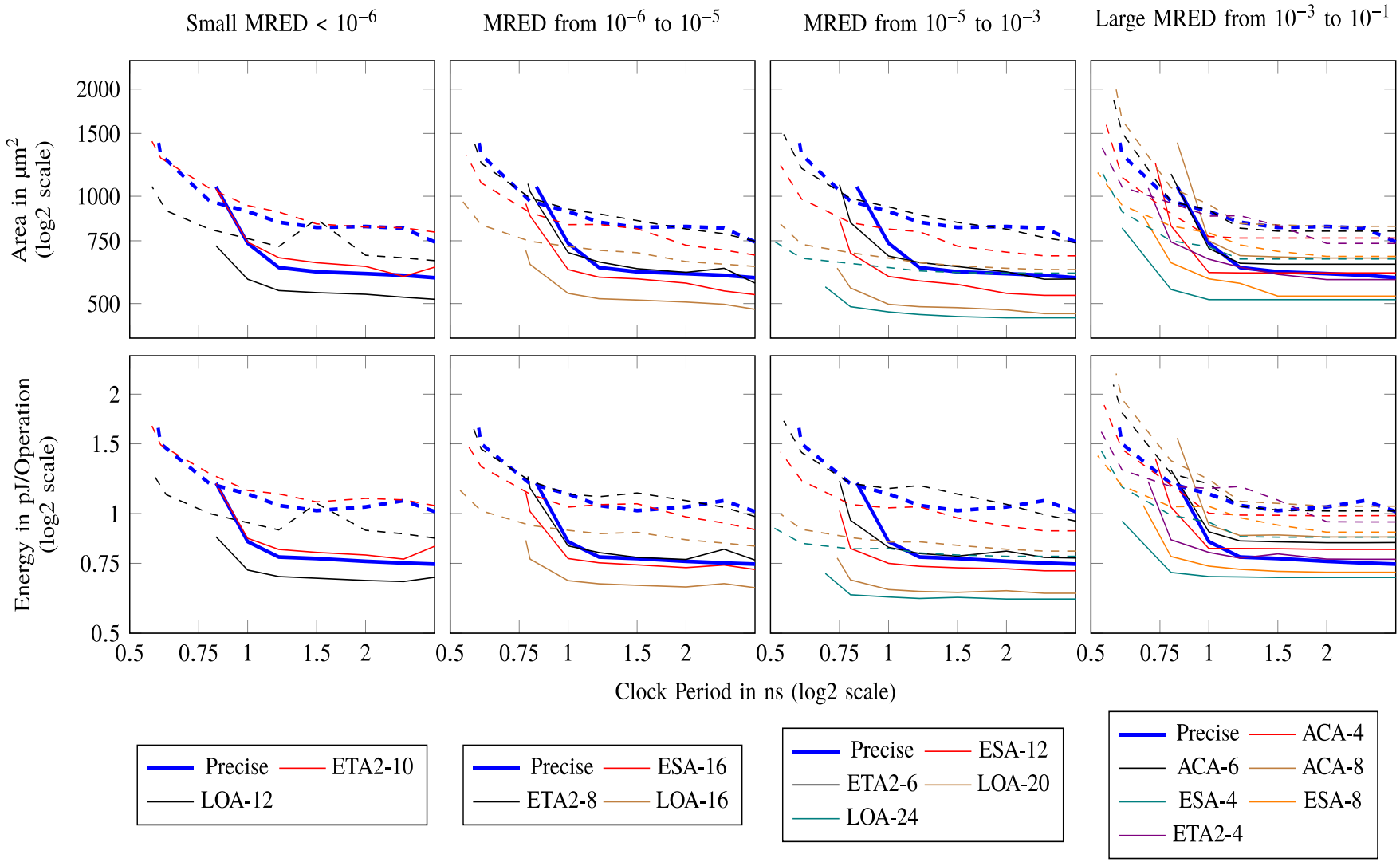

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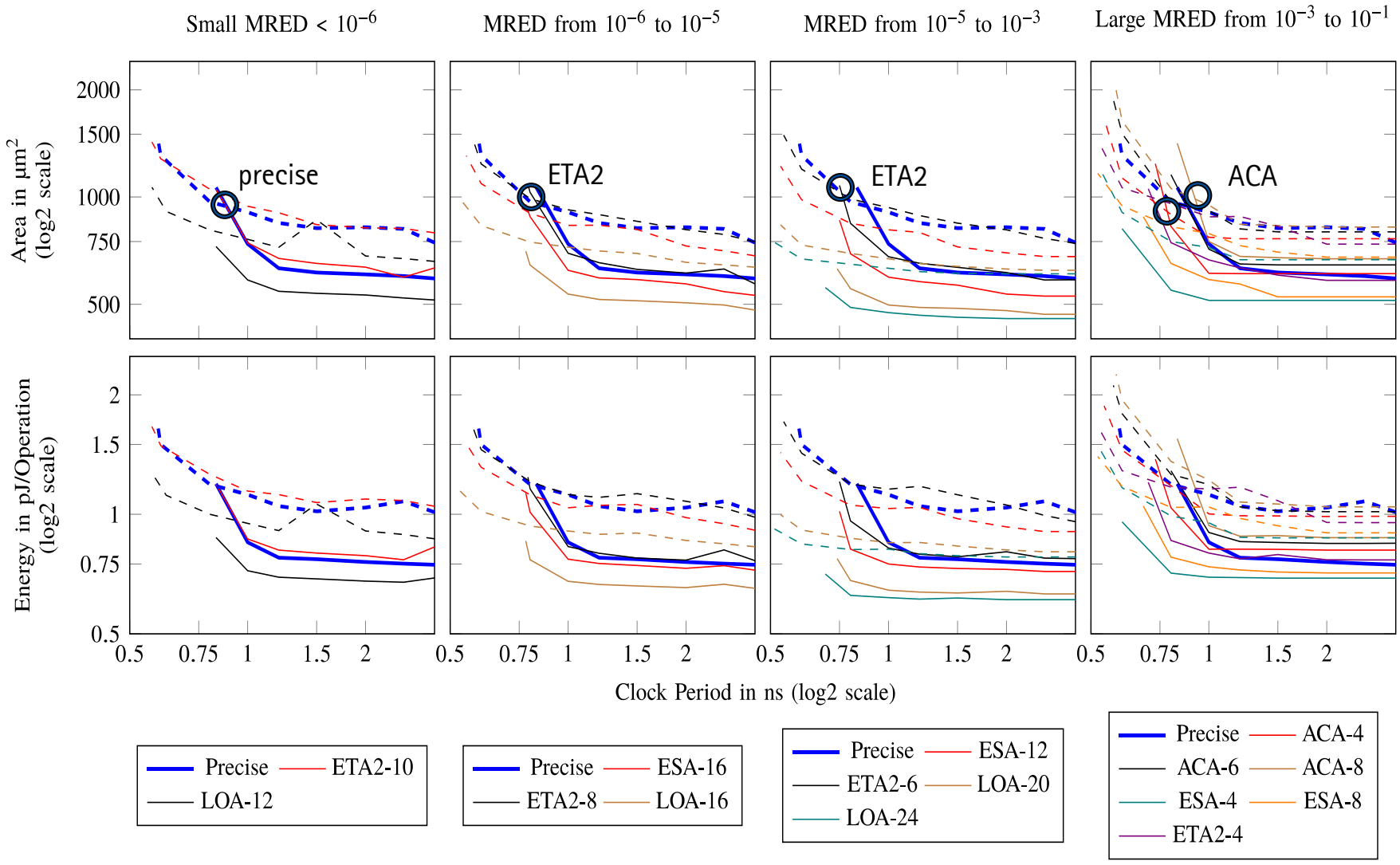

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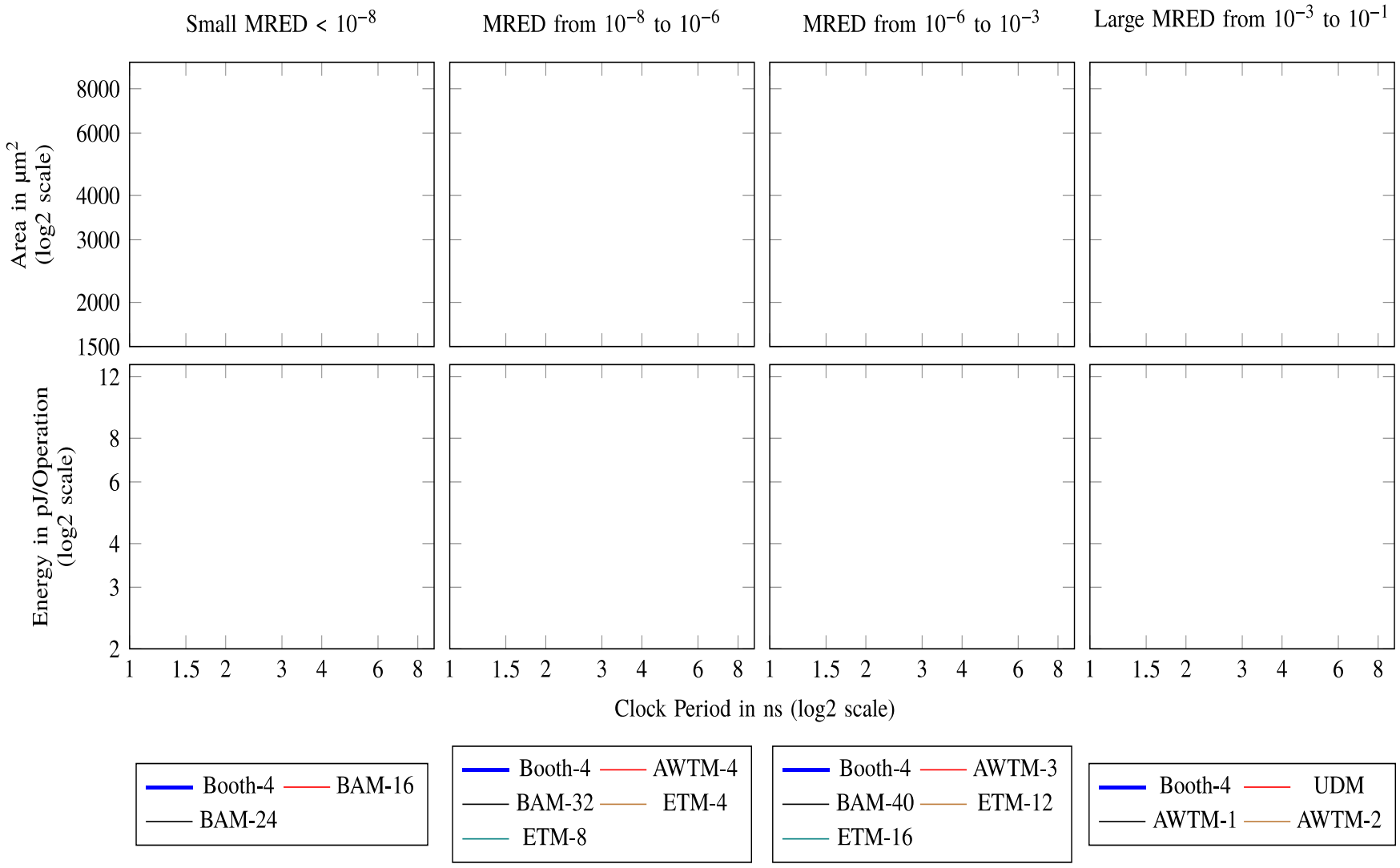

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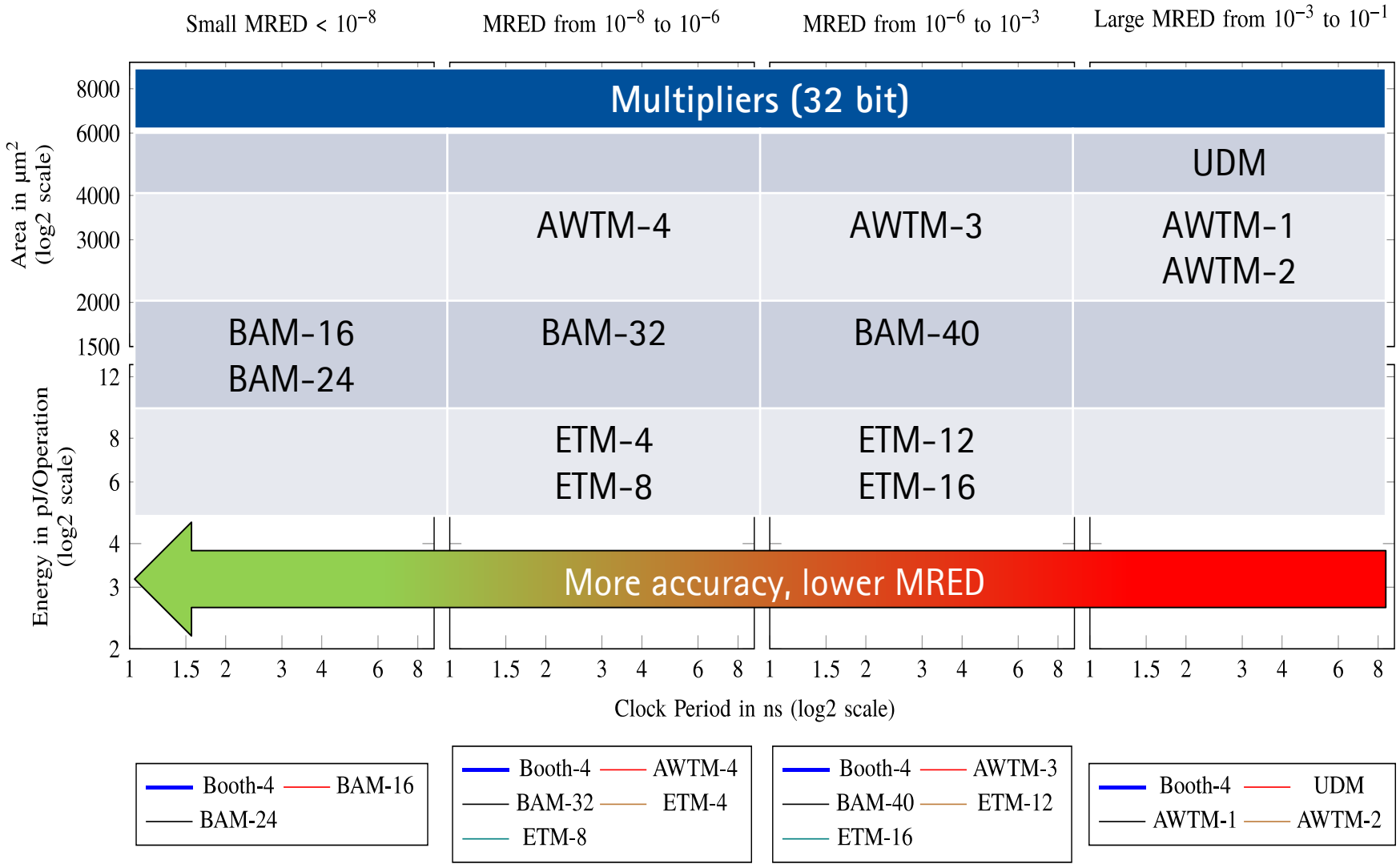

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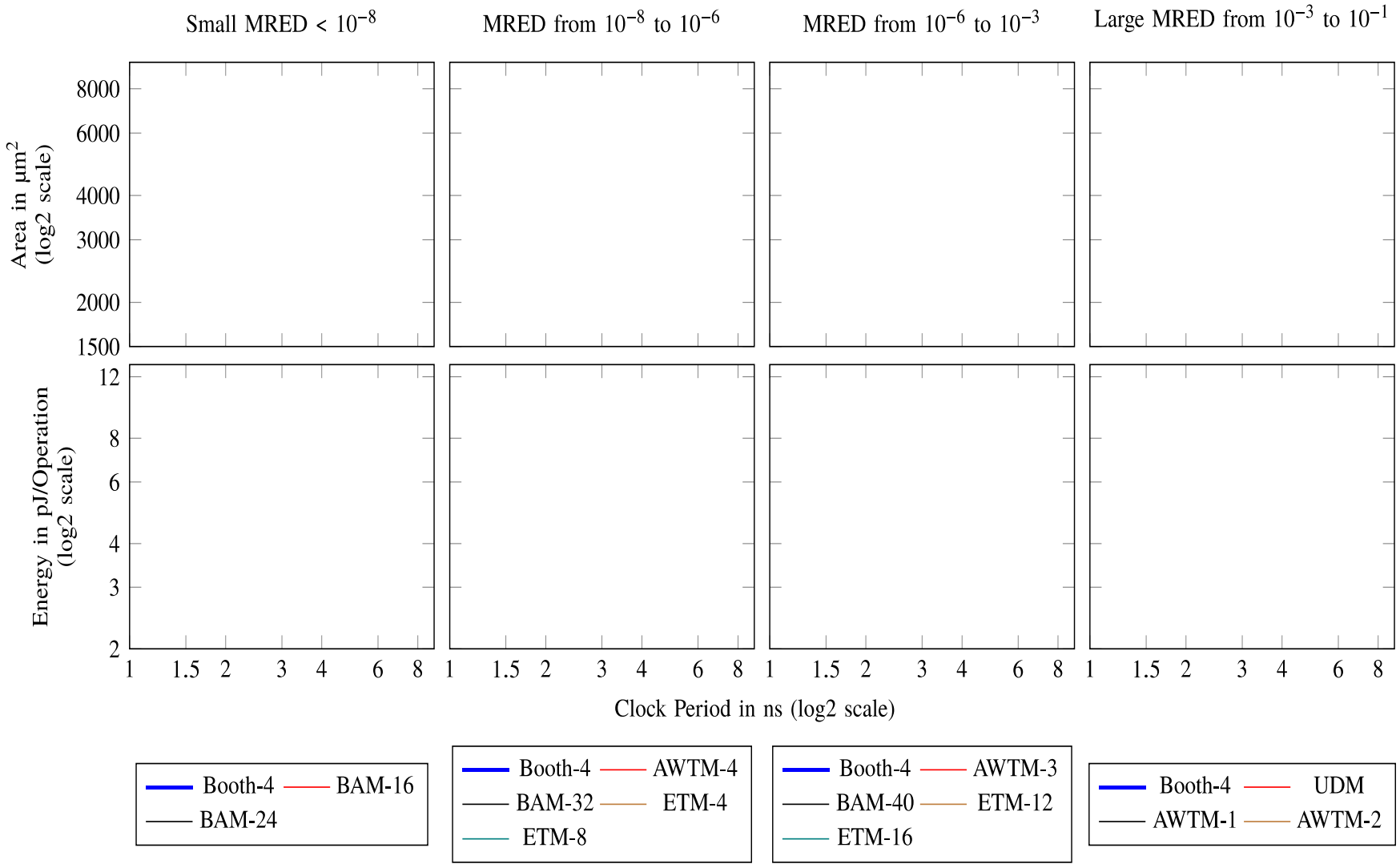

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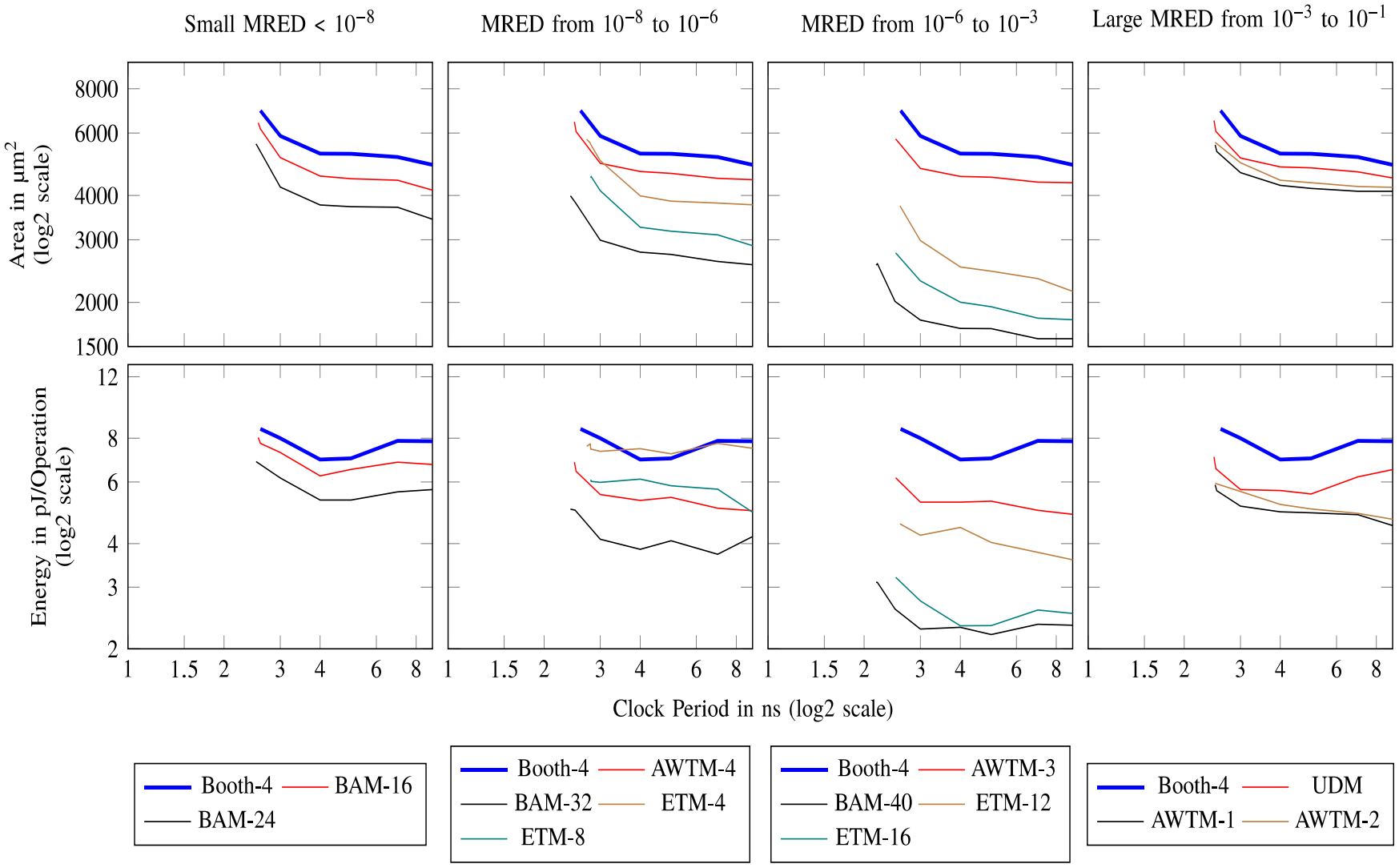

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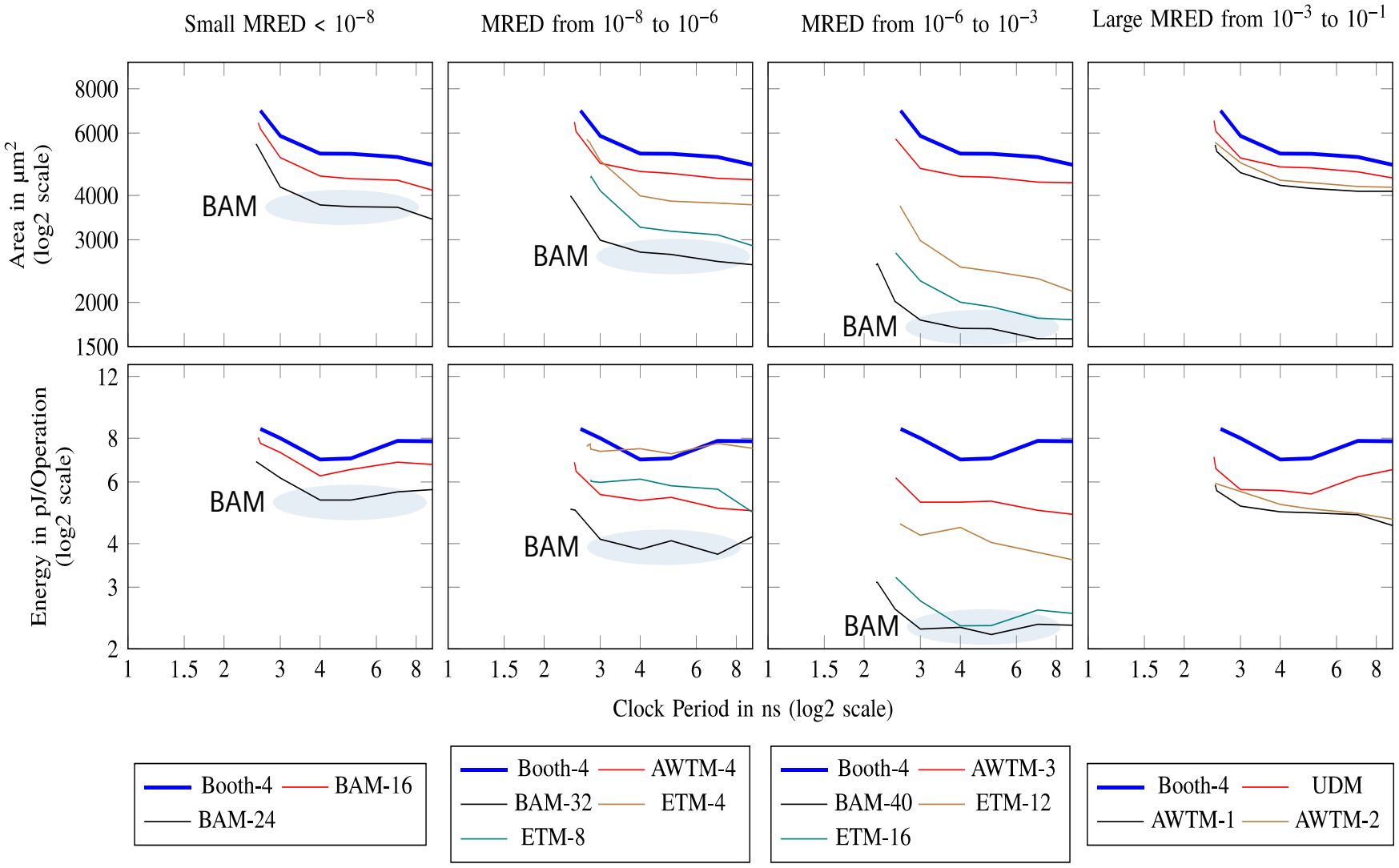

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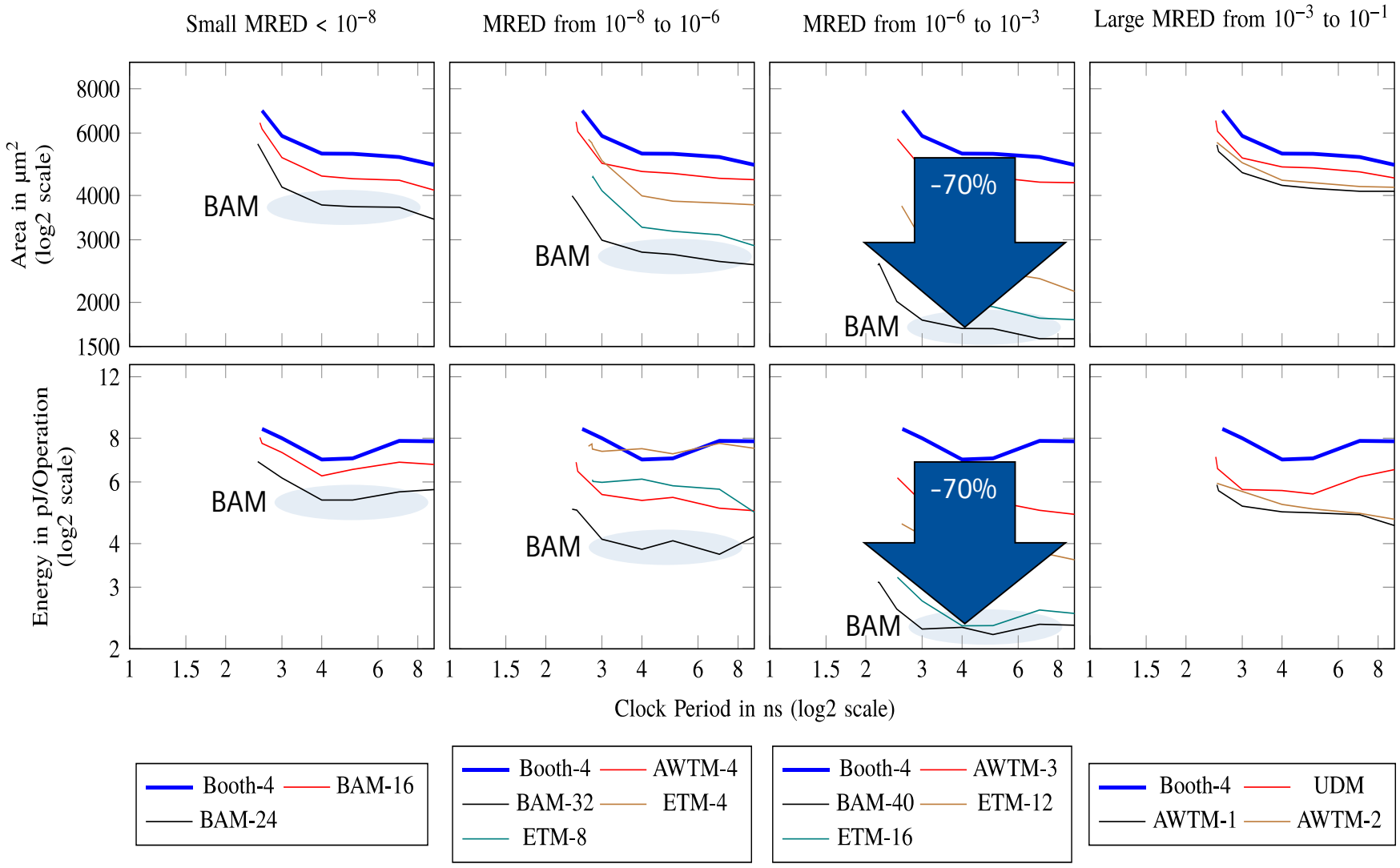

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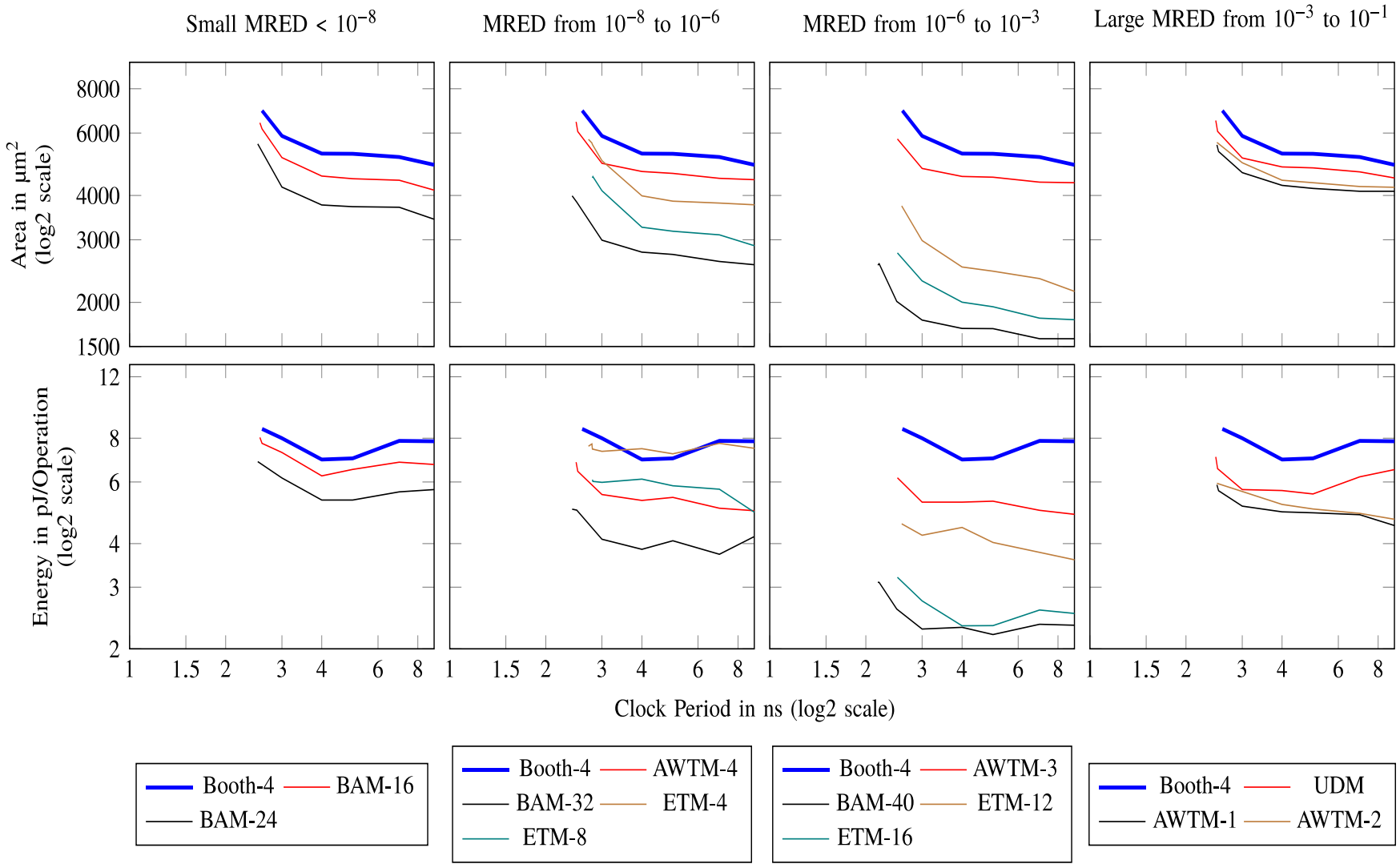

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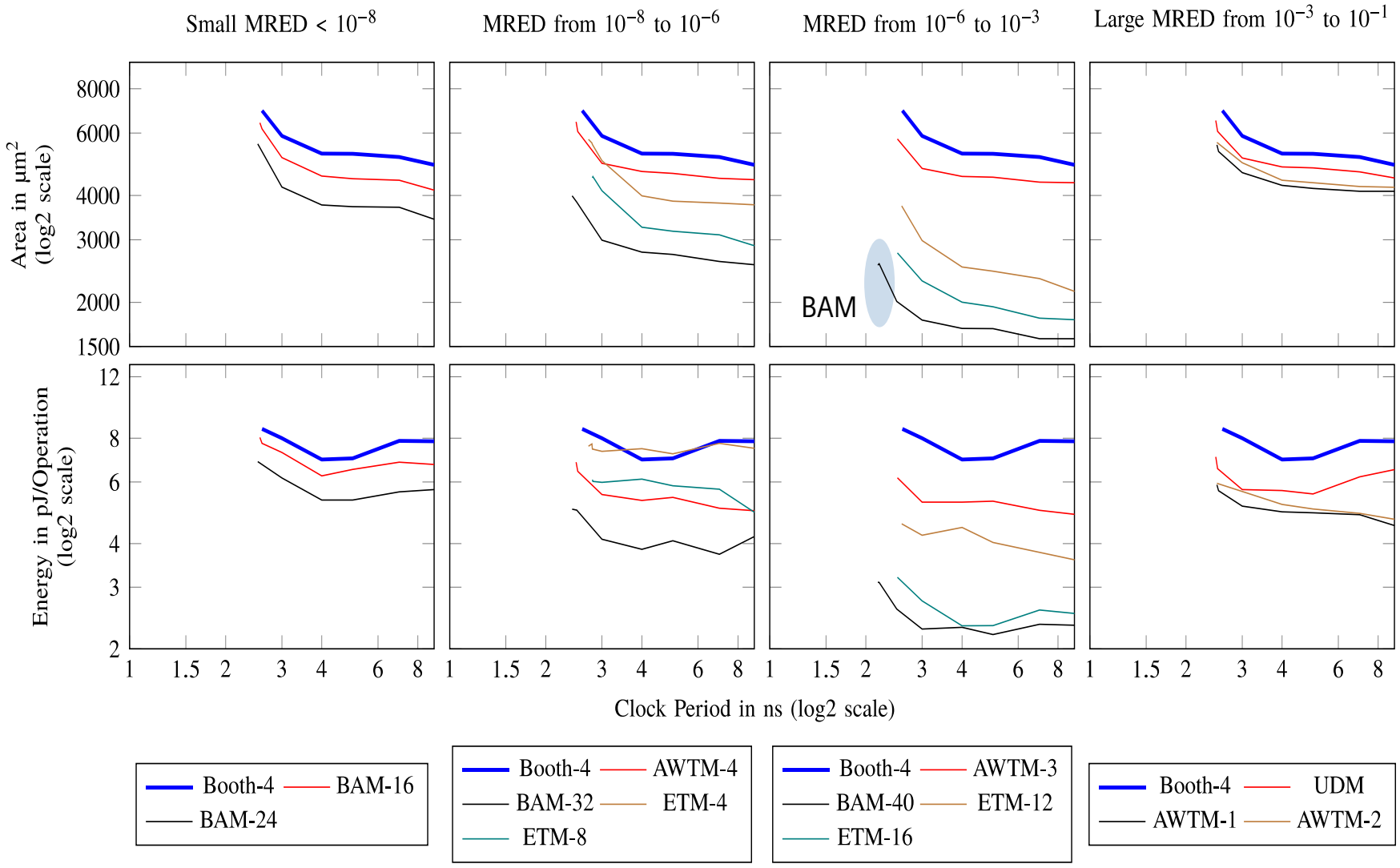

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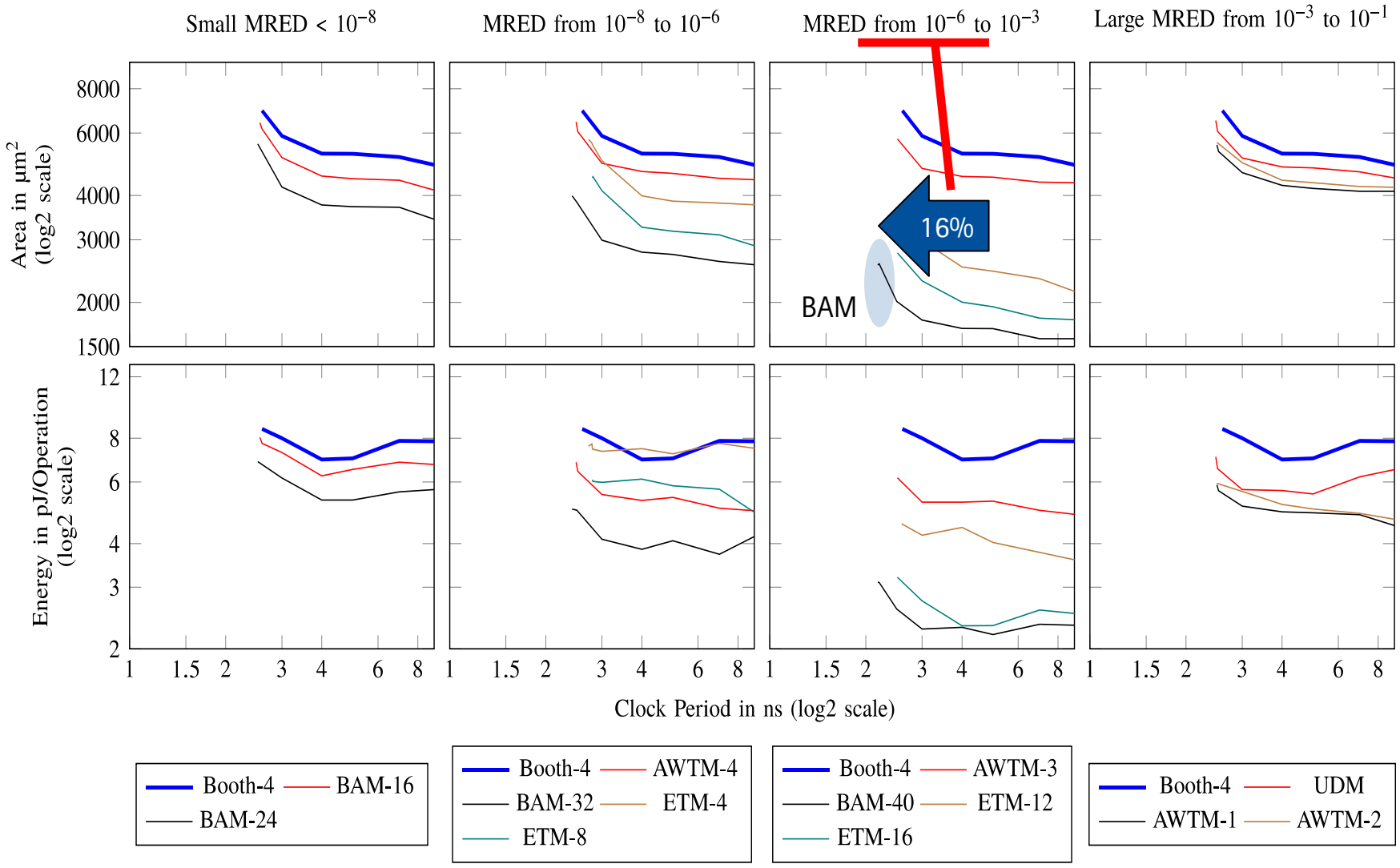

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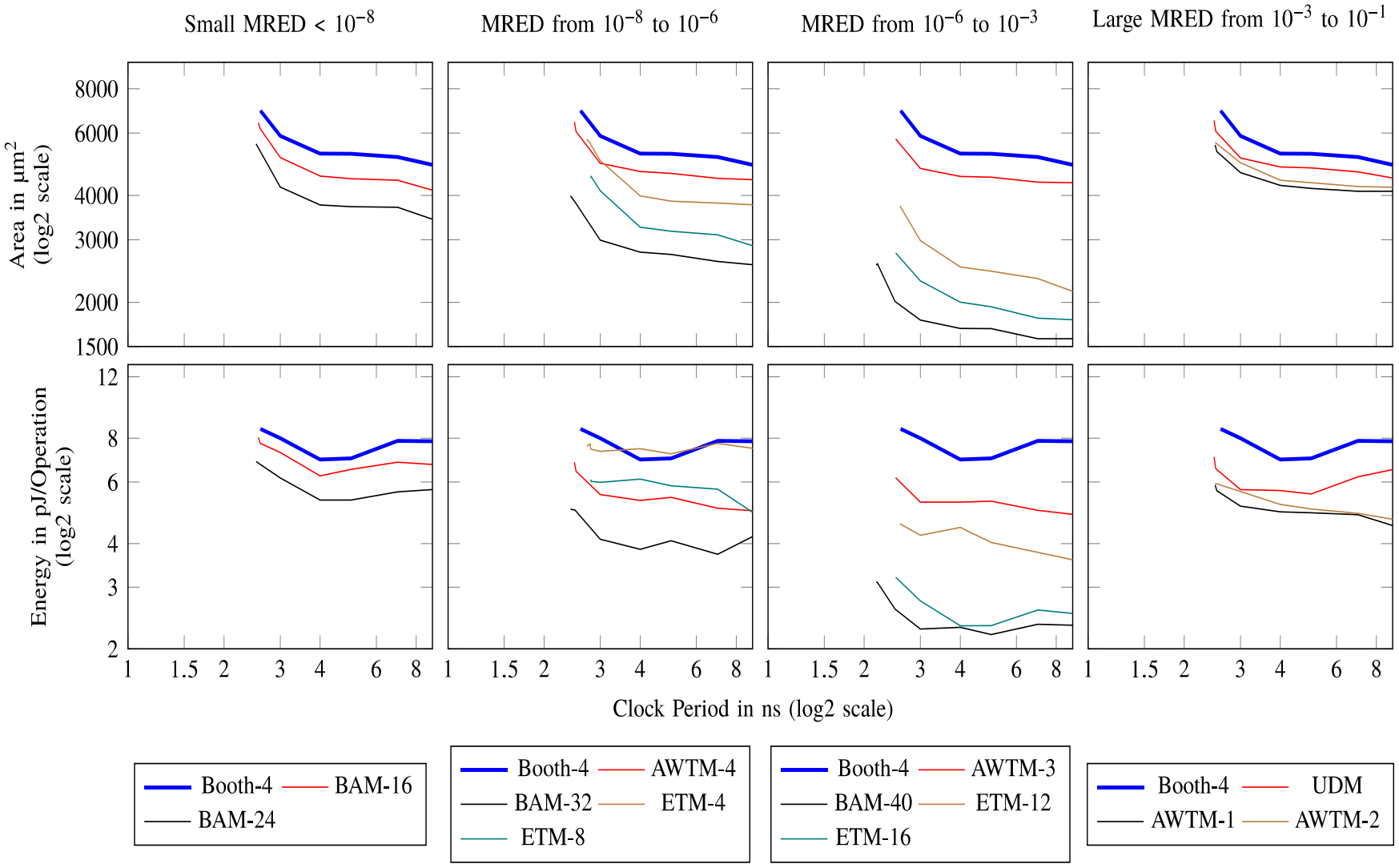

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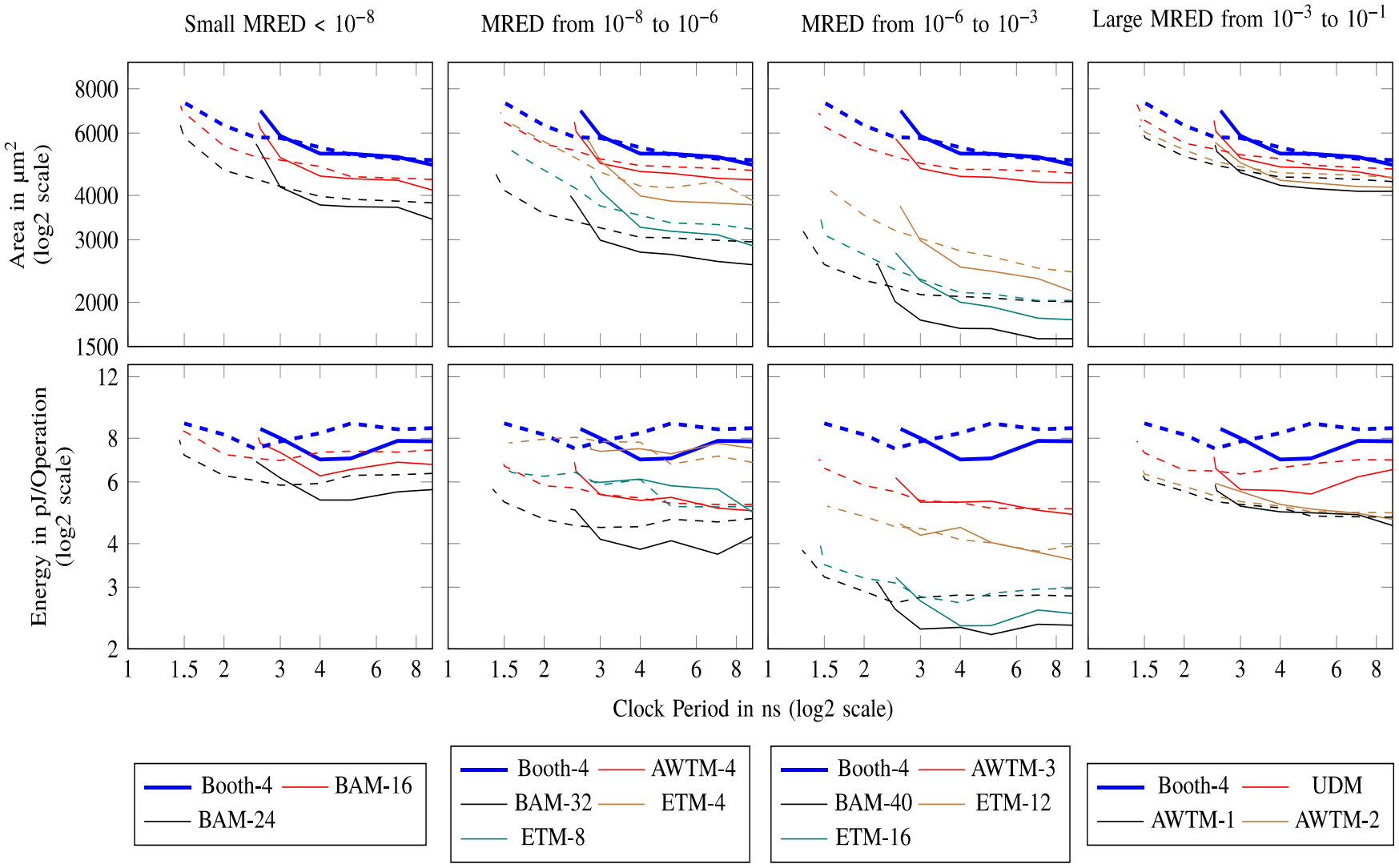

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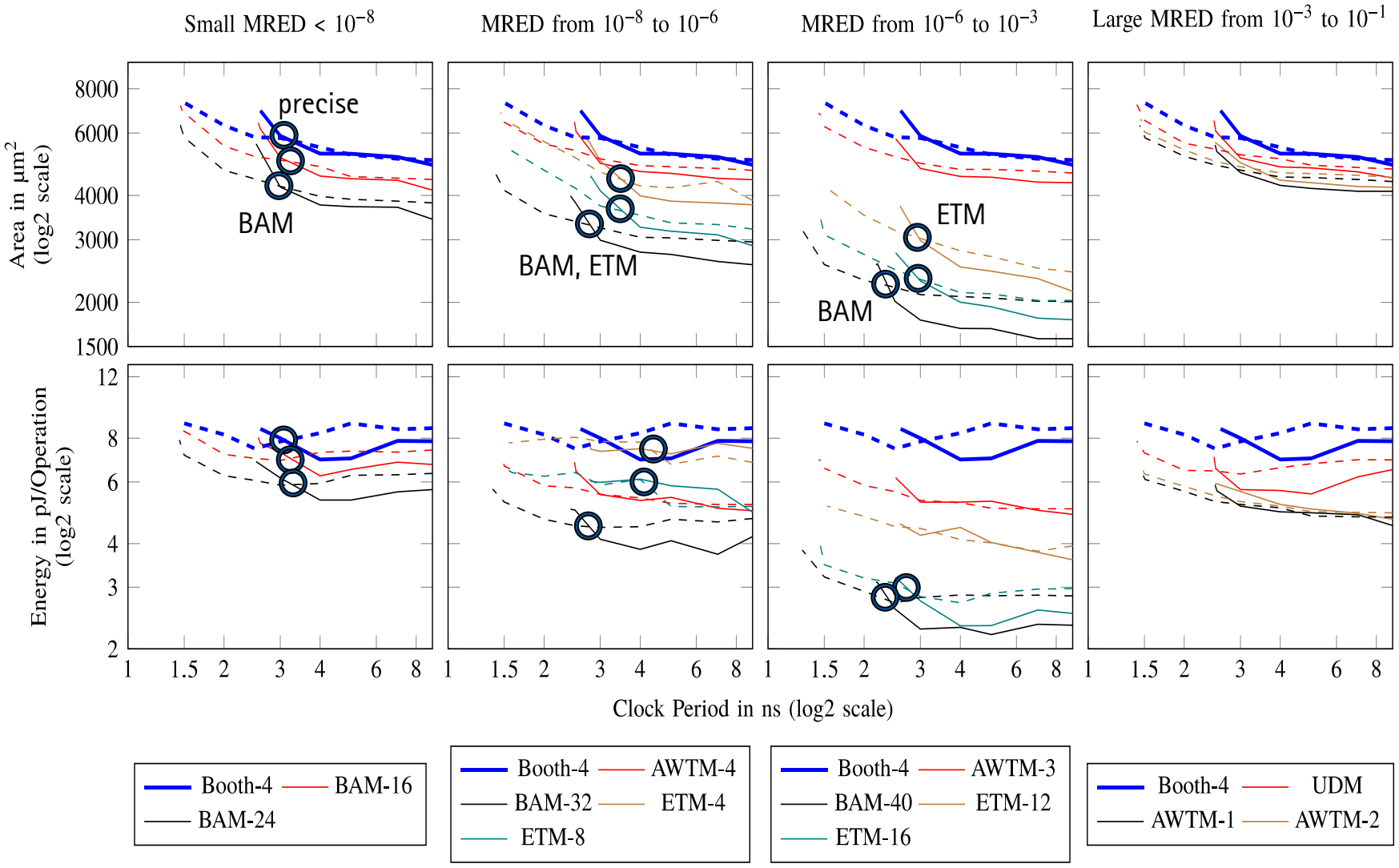

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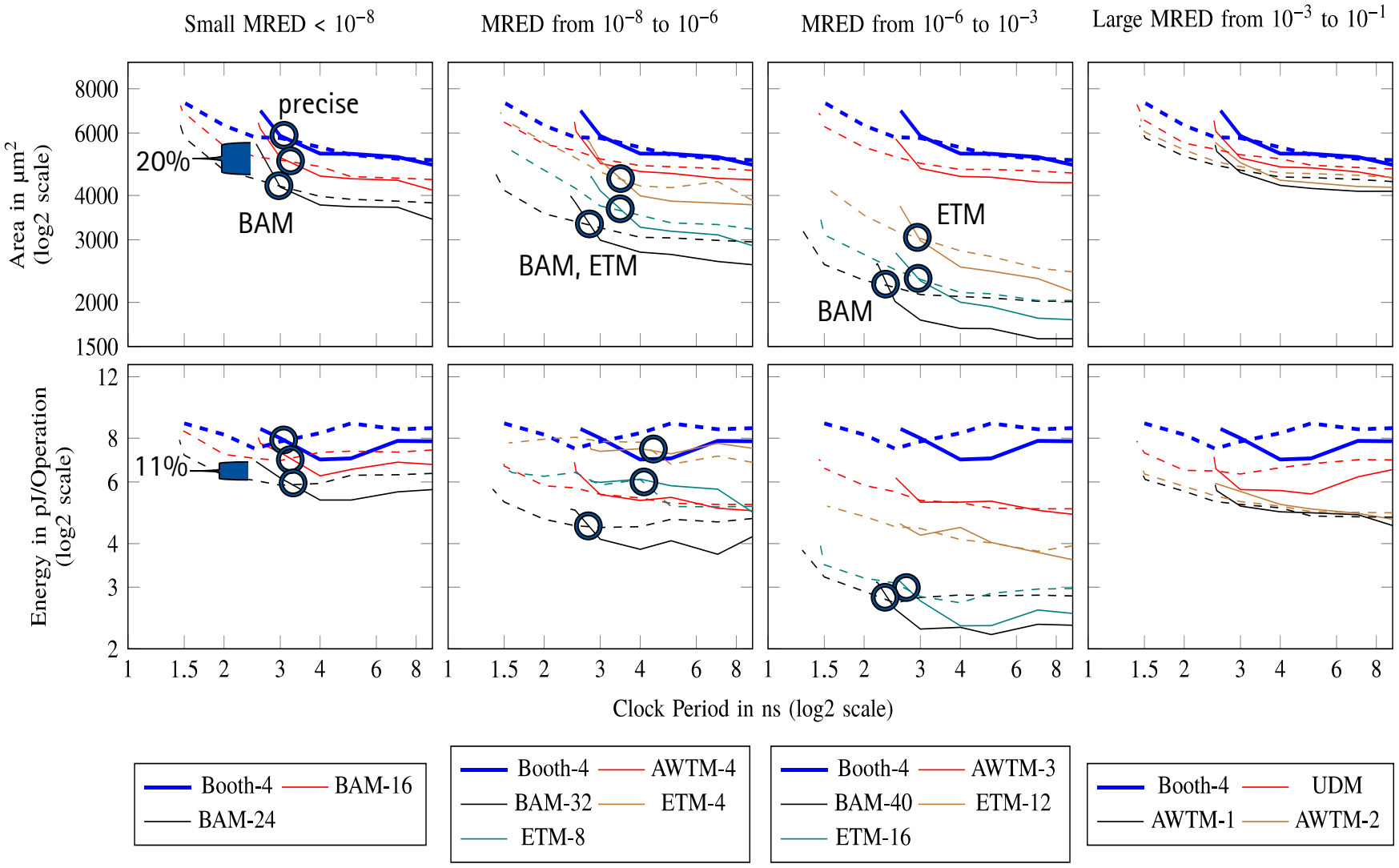

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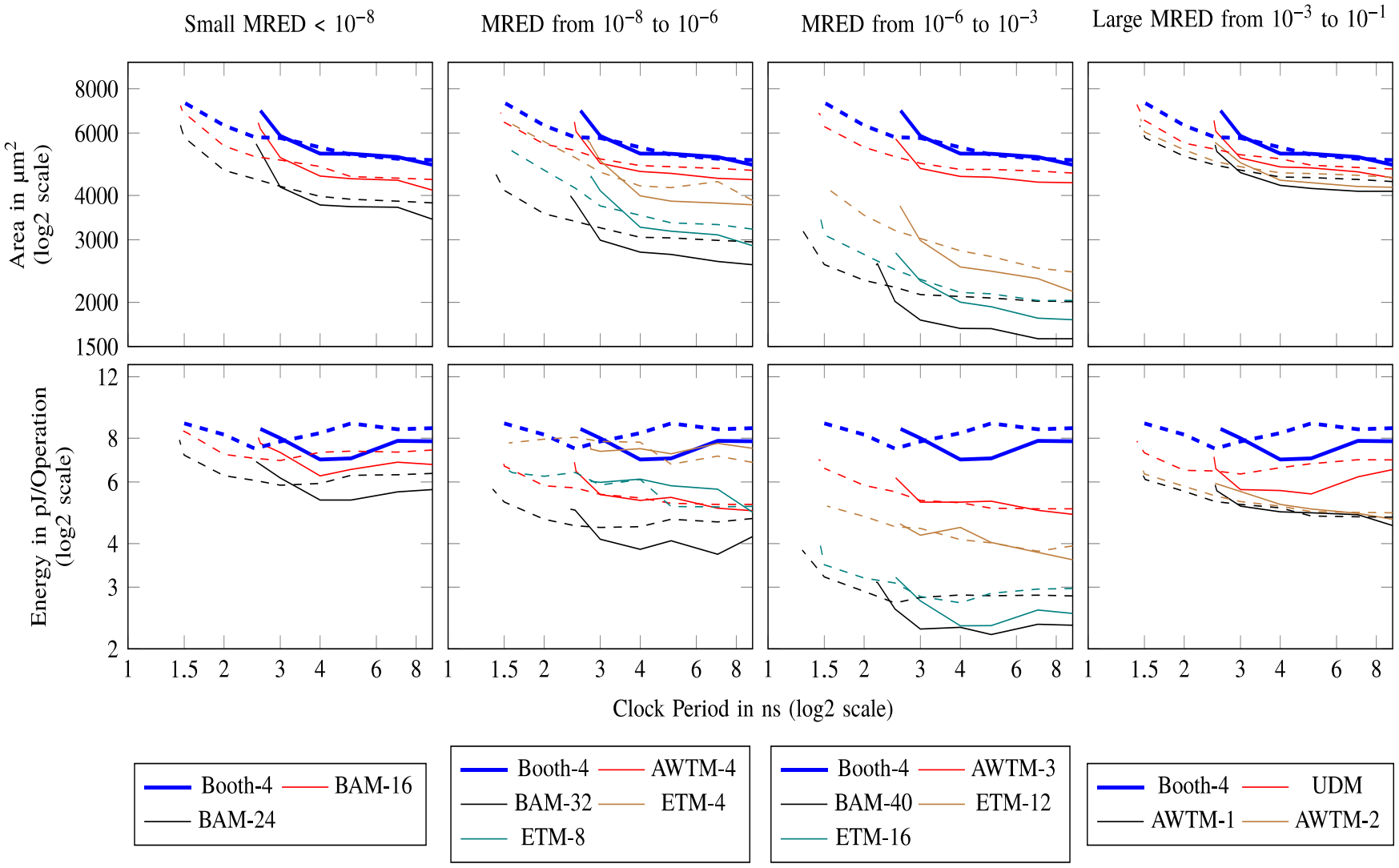

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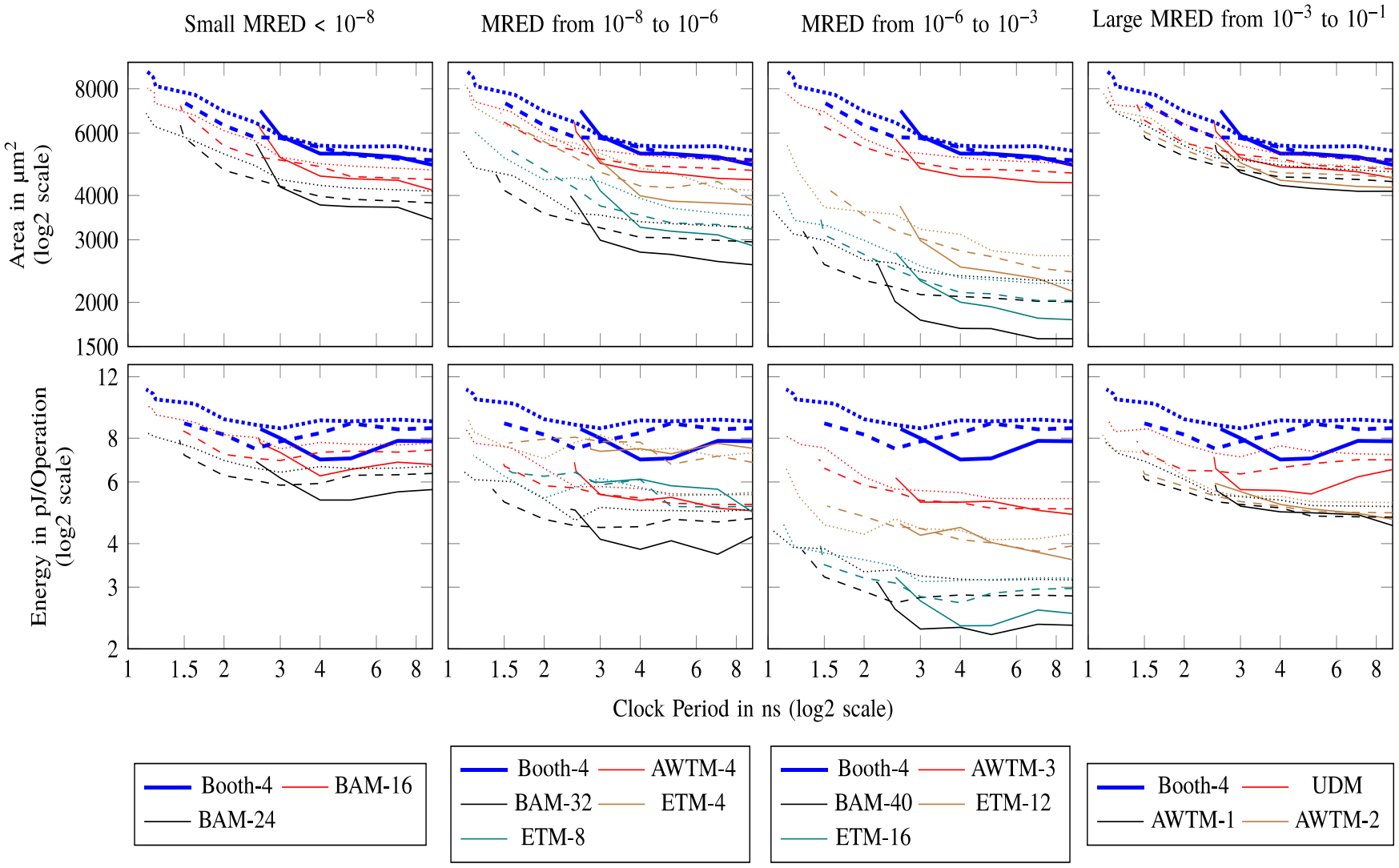

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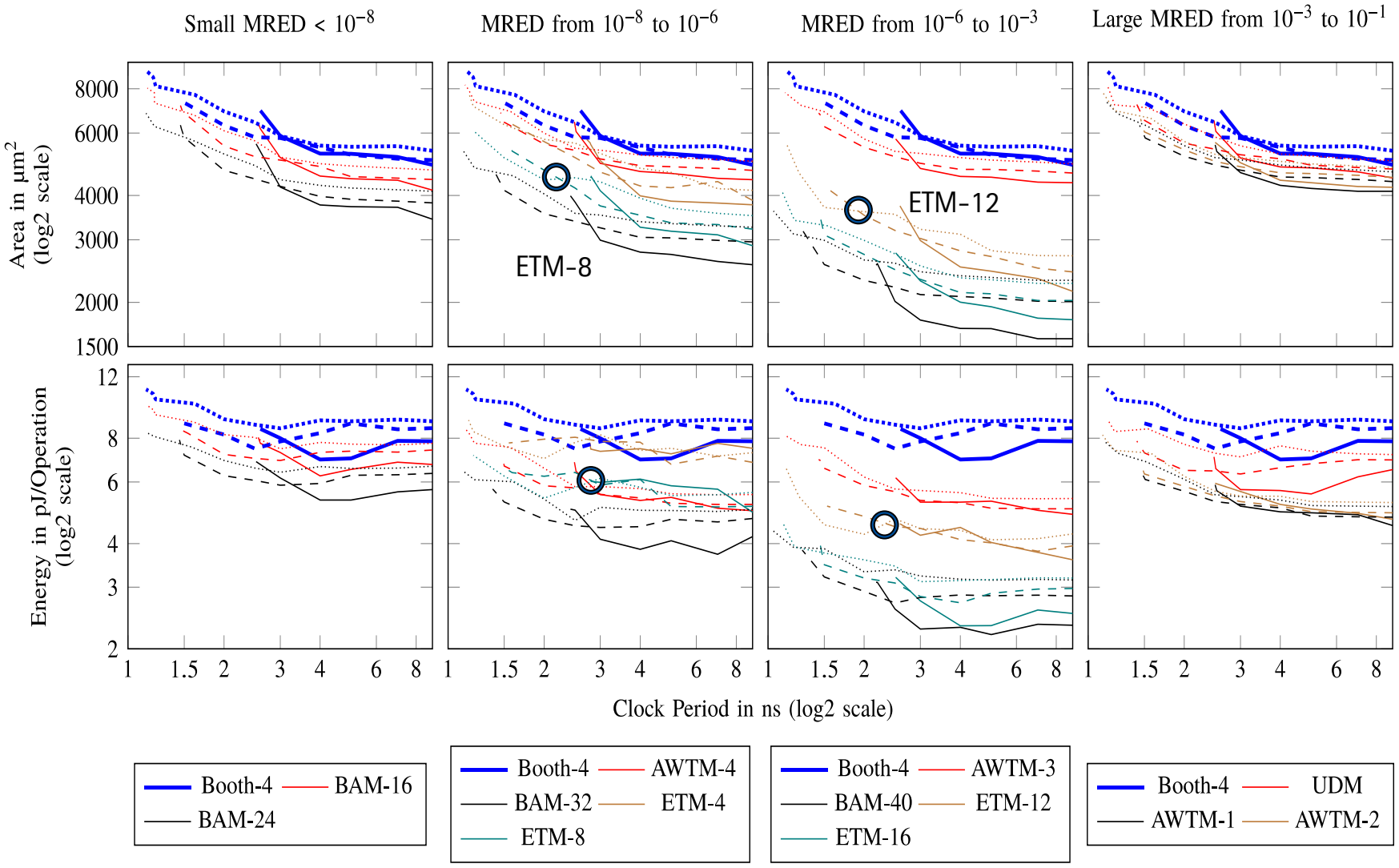

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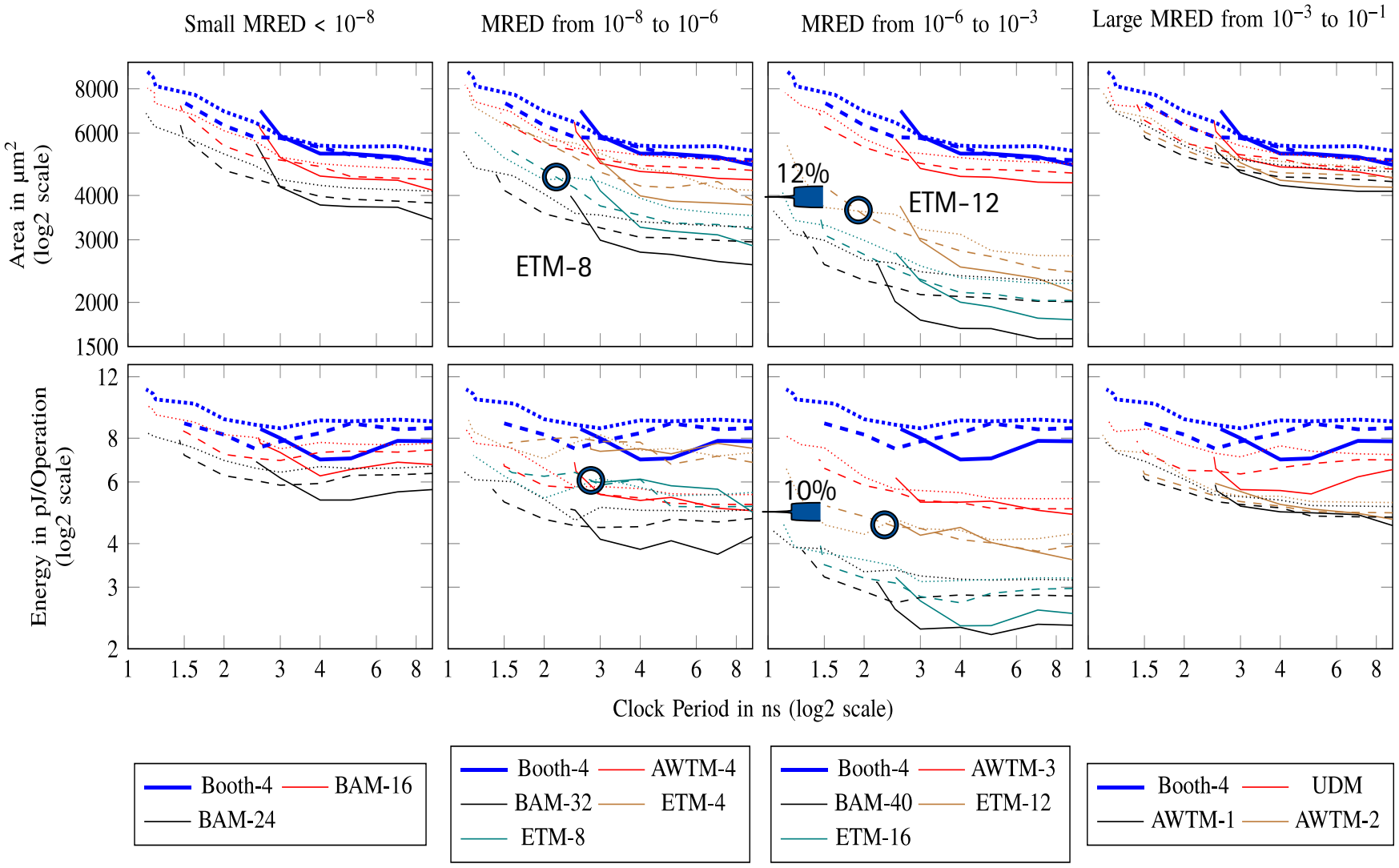

Conclusion

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  - Pipelining applied by register balancing

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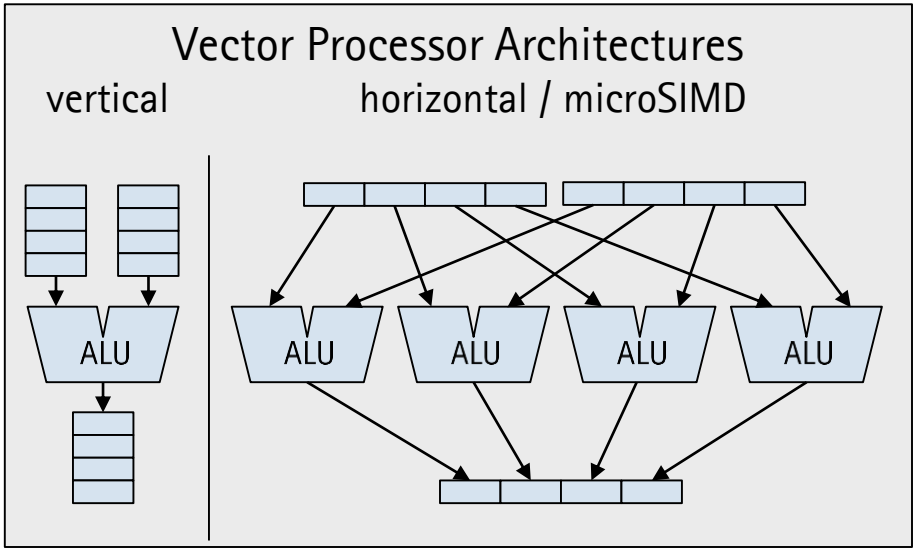
Pipelining aids in meeting the target timing constraint without switching to an approximate unit with lower accuracy

Thank you for your attention!

Backup: Vector Processor Architectures

- Specialized architectures for operating on independent, massively vectorizable data



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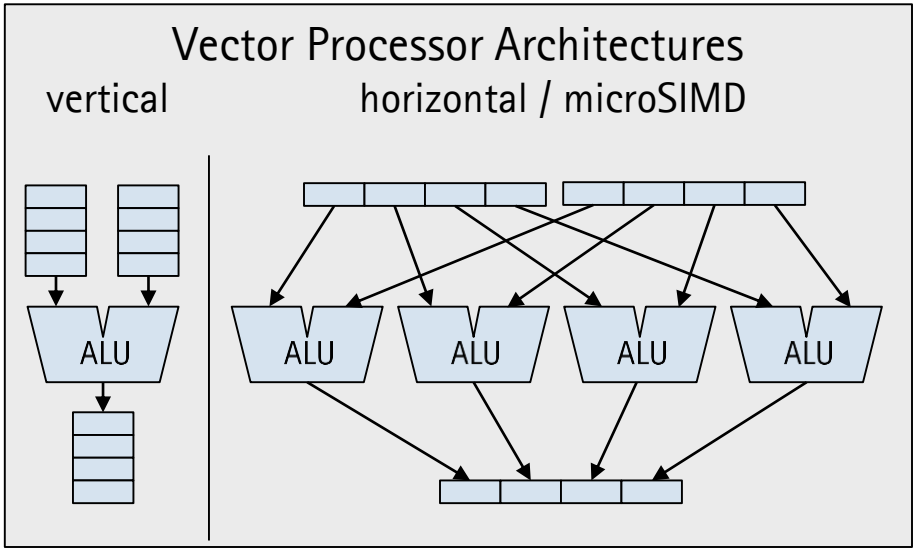

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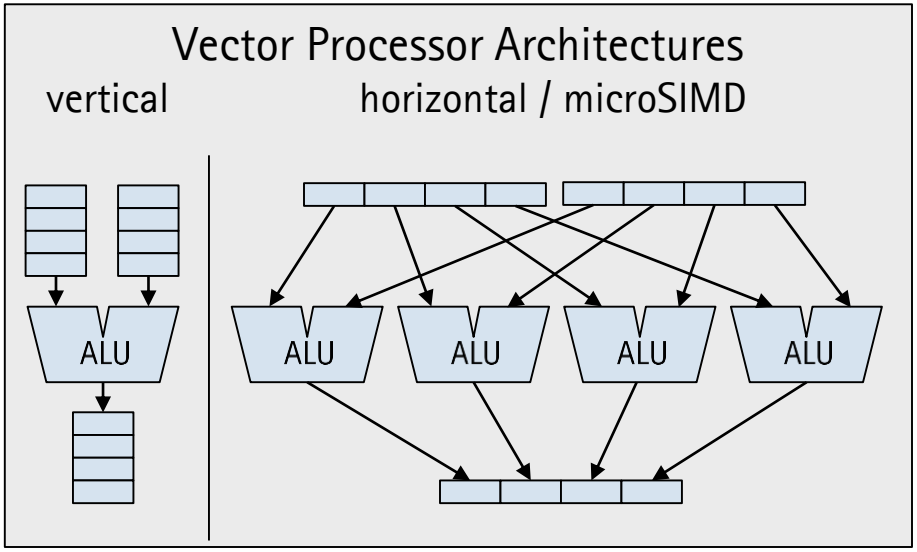

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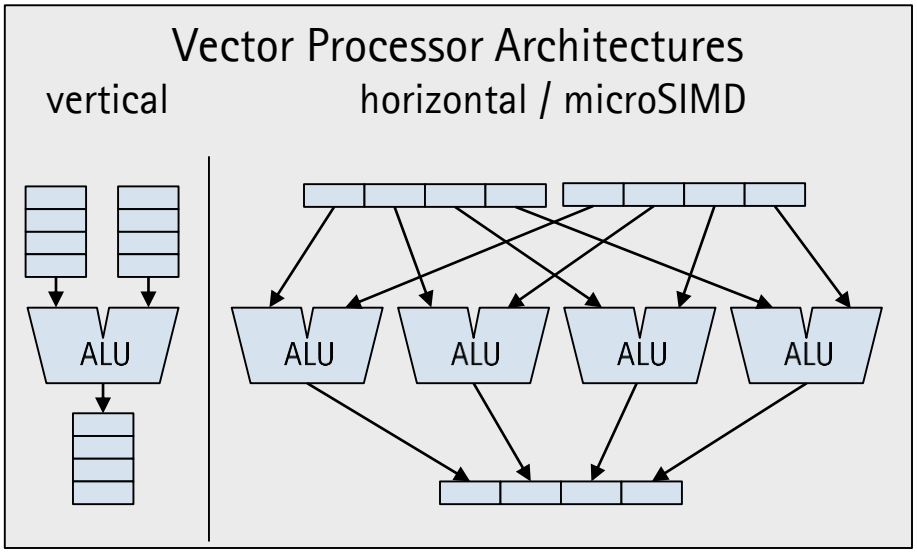
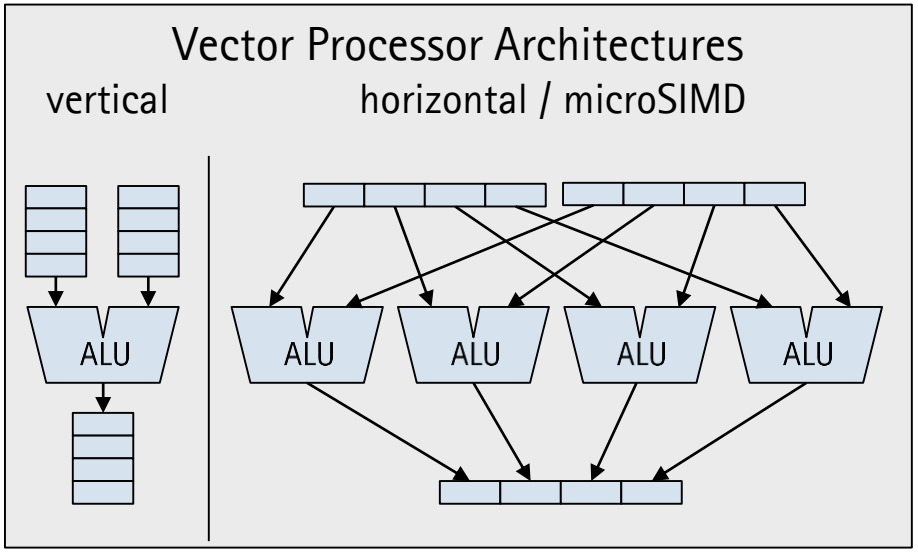
    - Approximate adder and multiplier designs



Backup: Analysis Framework for *Approximate* and *Stochastic Computing* Processor Architectures



Generic VHDL description, exploit data-level parallelism of image processing algorithms

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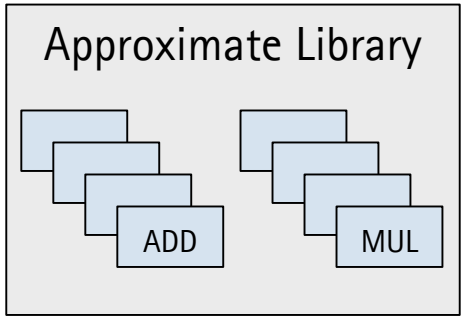
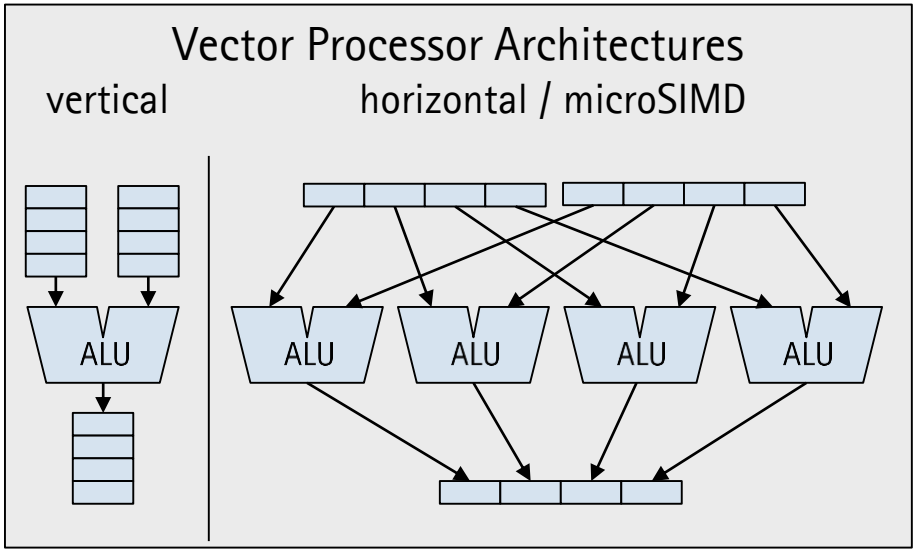


Generic VHDL library of approximate adders & multipliers



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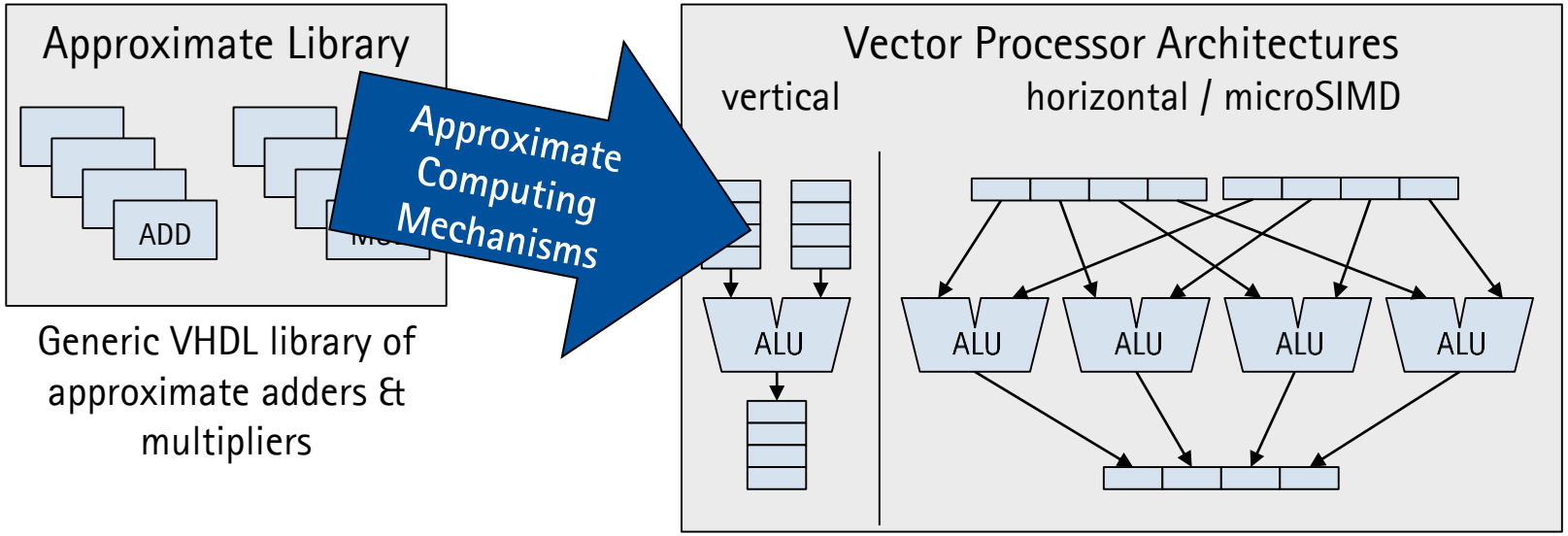

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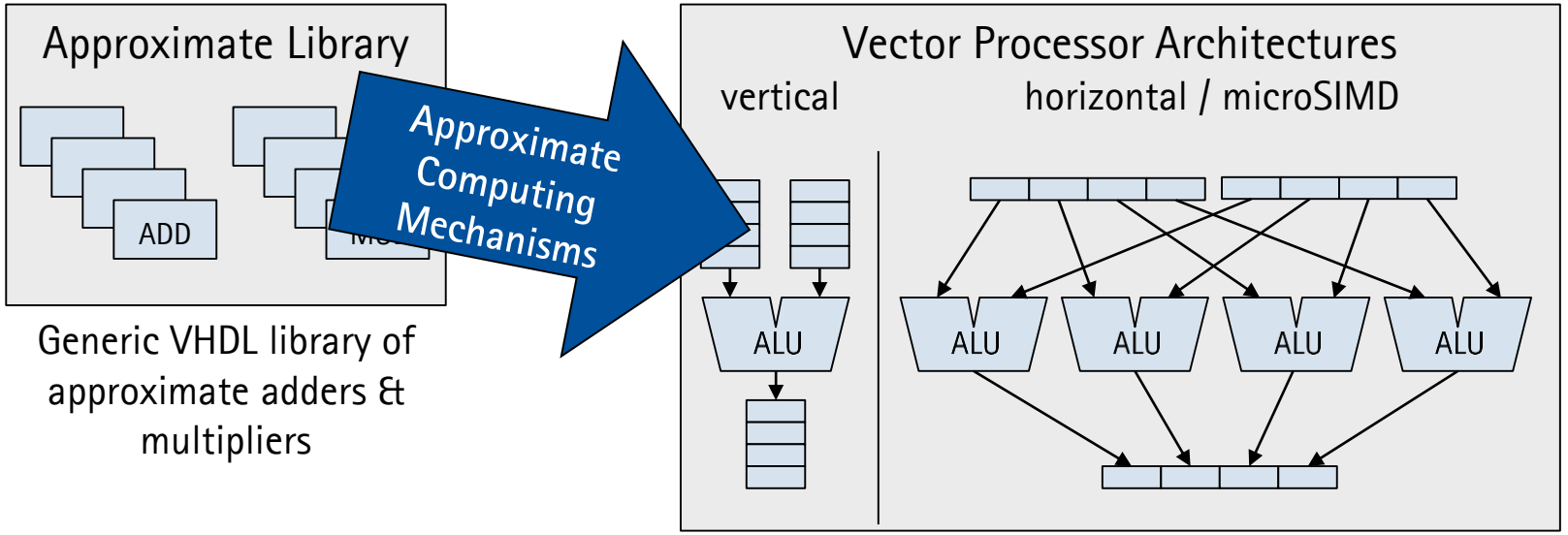

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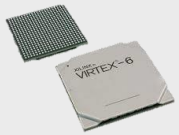
FLINT+

FPGA-based Timing Analysis Framework for Stochastic Computing Operation



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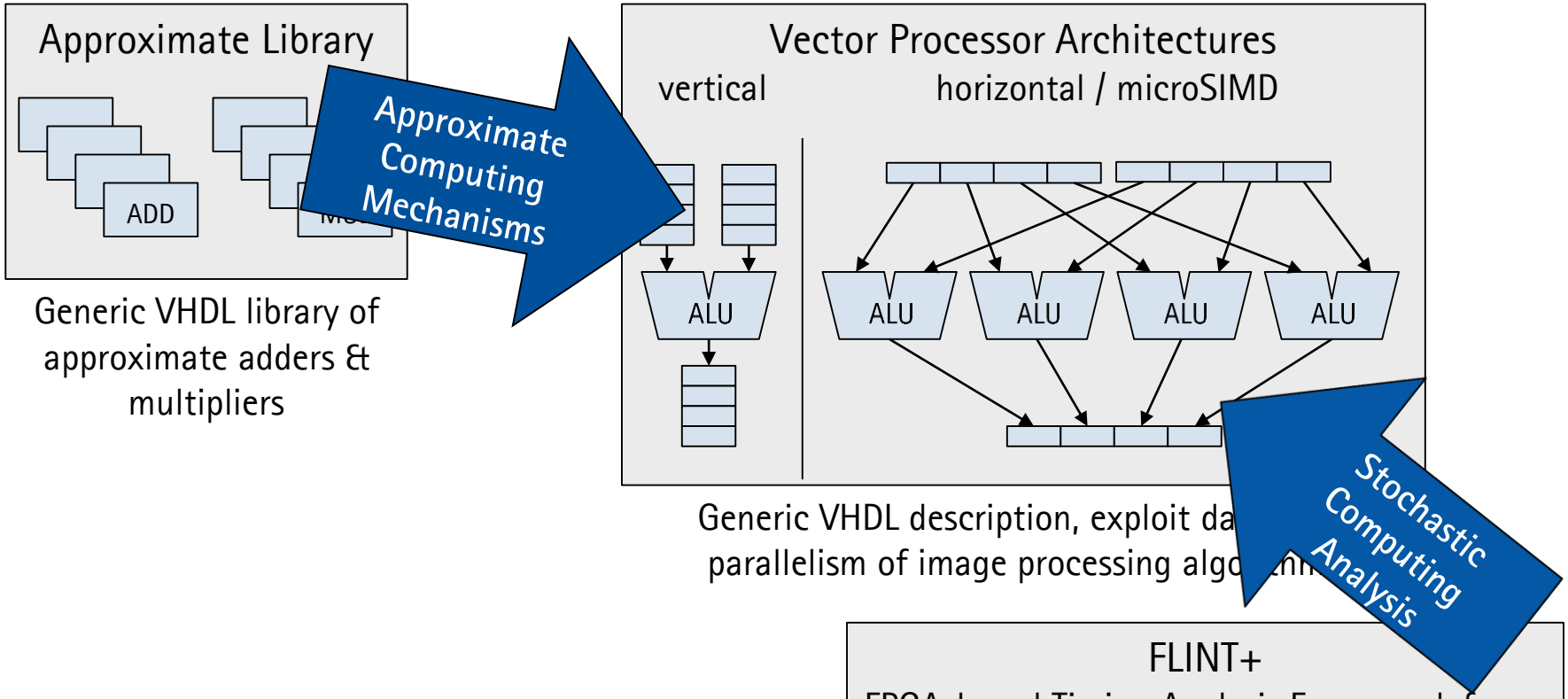

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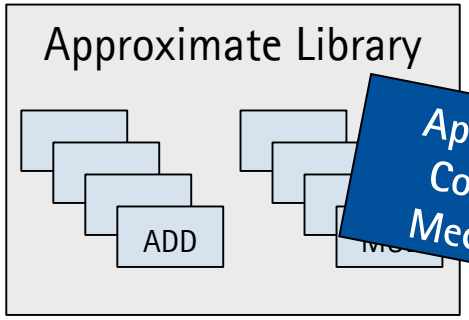

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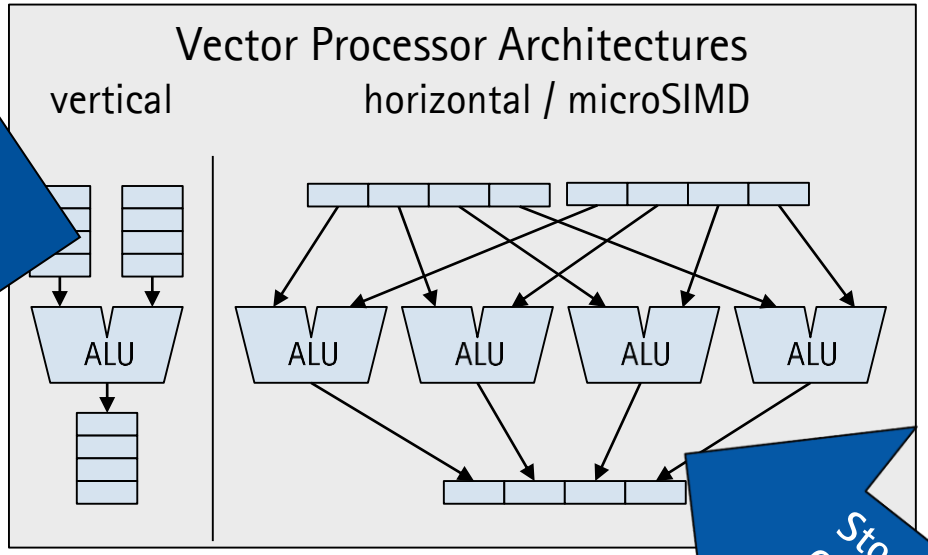
Approximate Computing Mechanisms



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Stochastic Computing Analysis

CV Application
e.g., SIFT feature extraction, stereo image rectification

FLINT+
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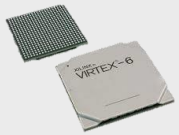

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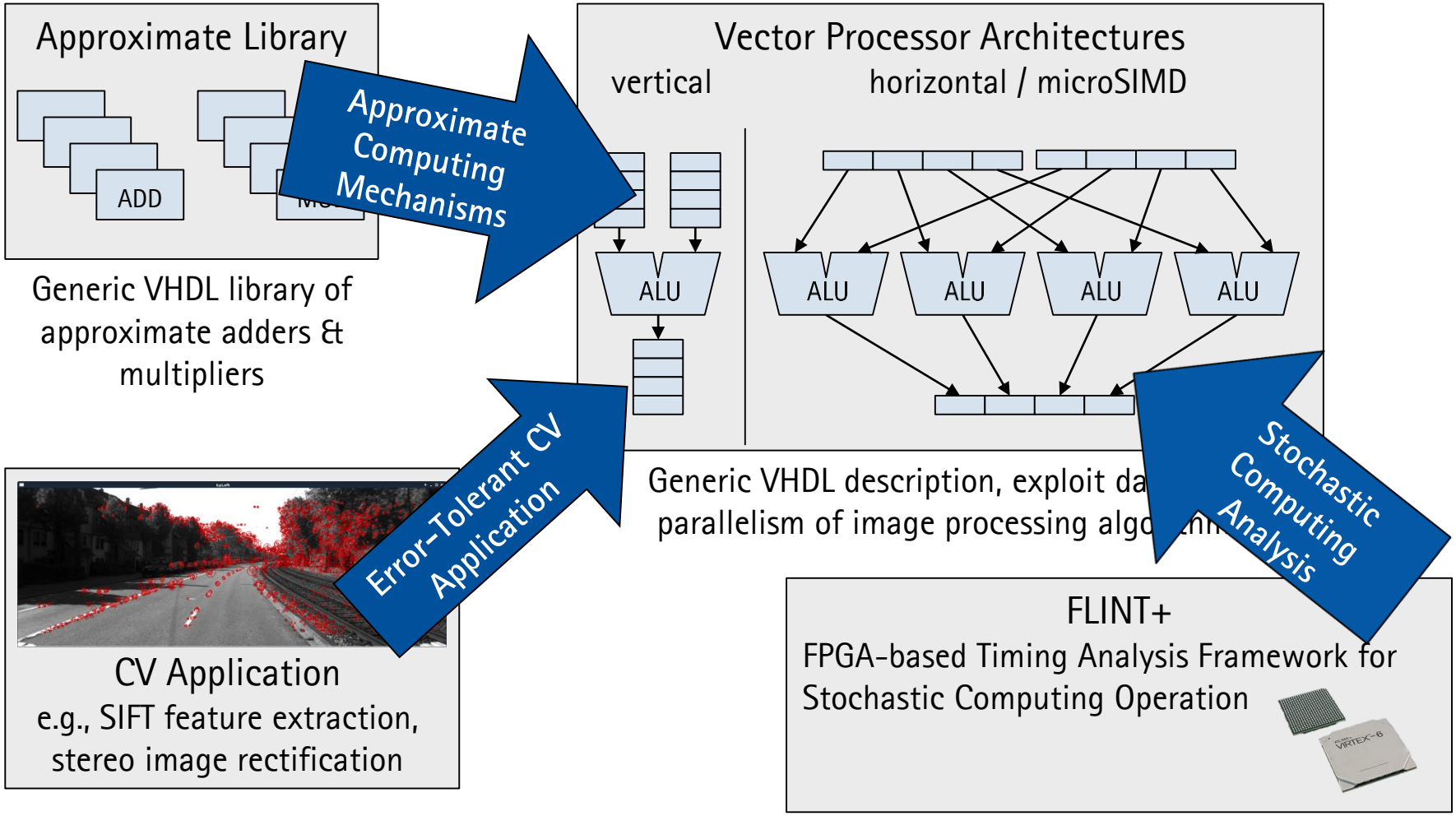

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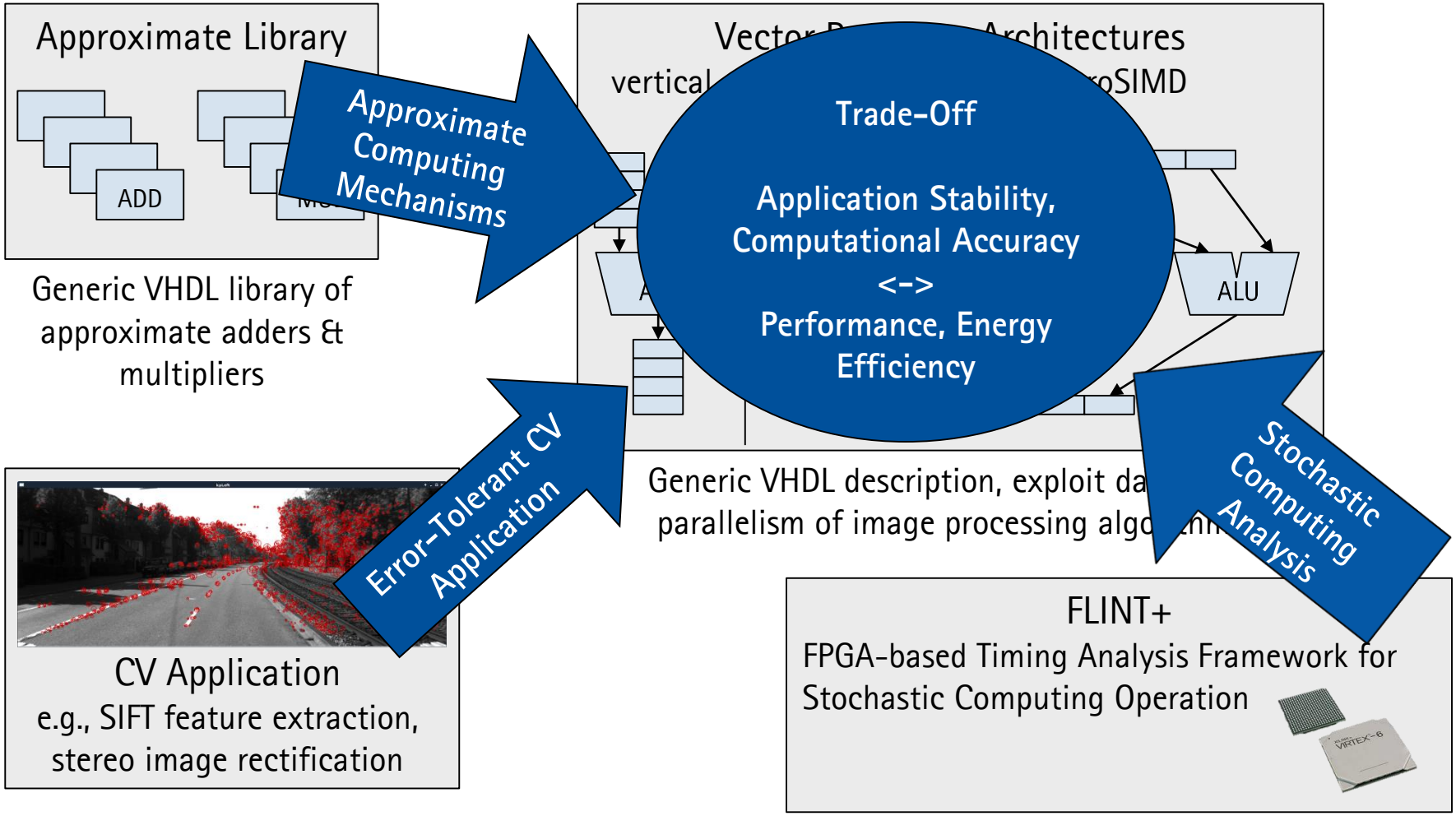

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  - Inferring optimized precise sub-components

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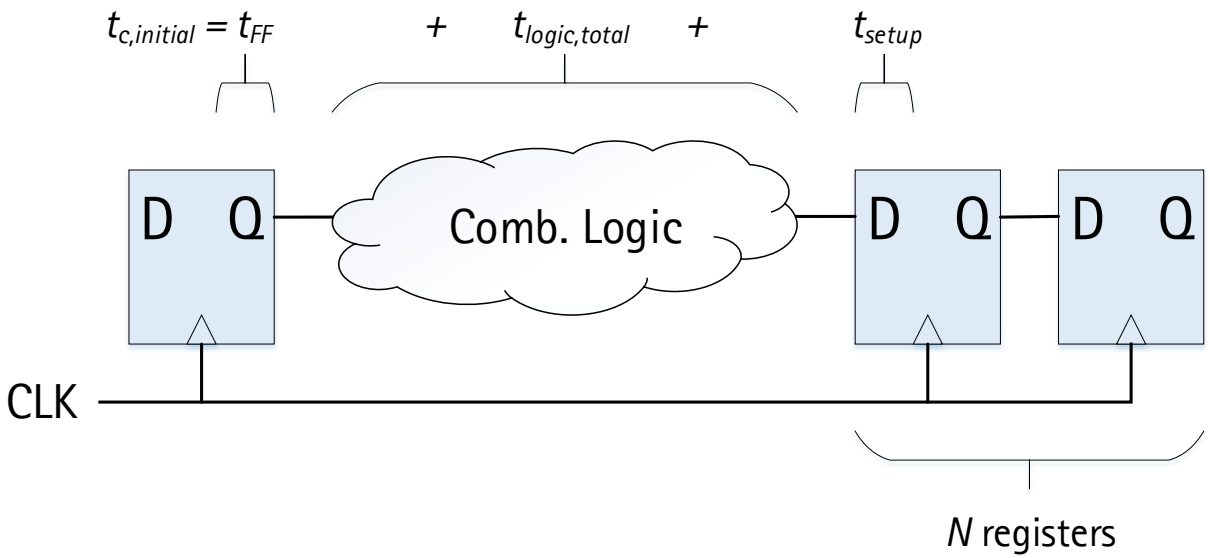

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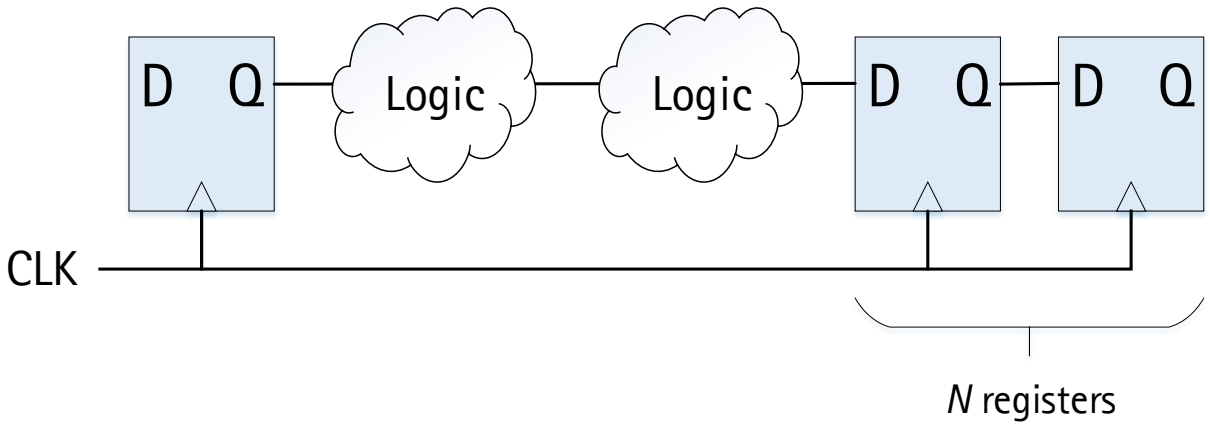

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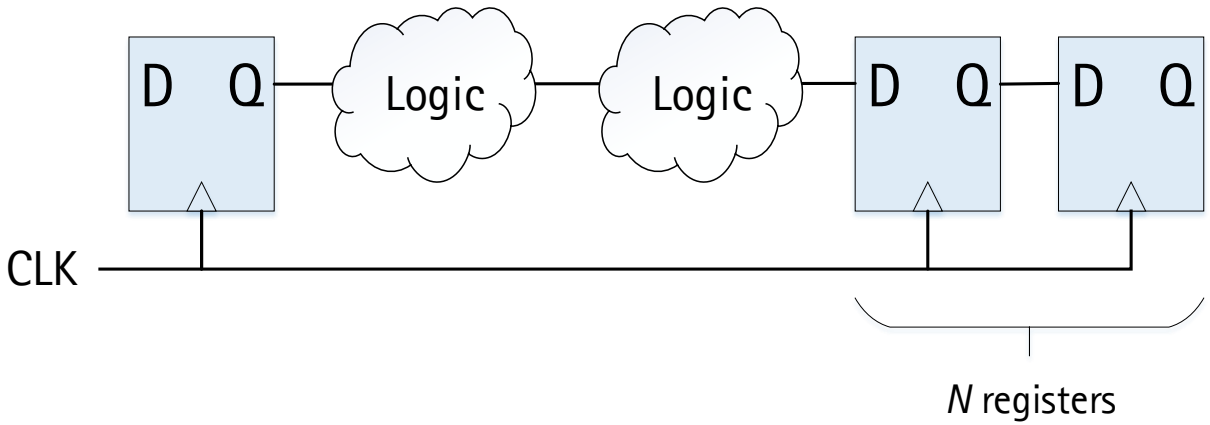

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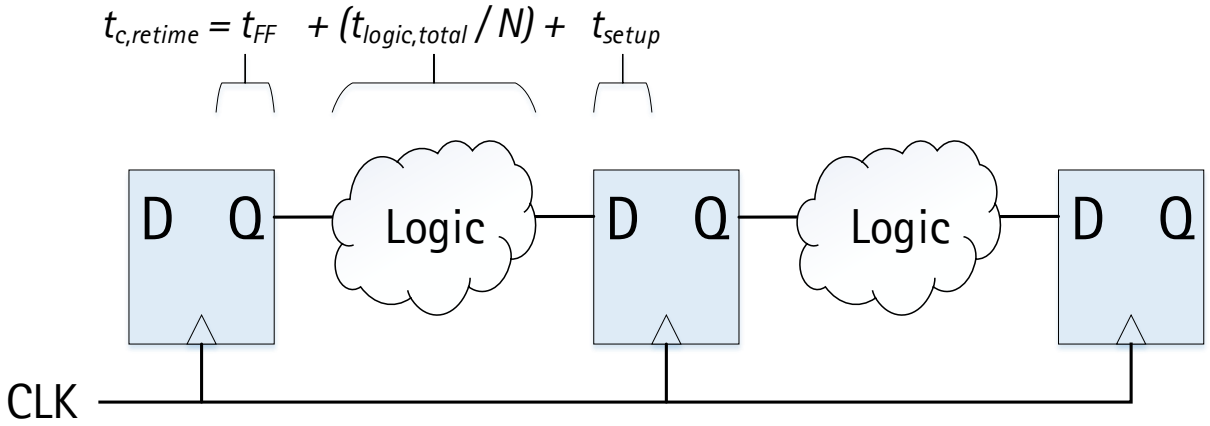

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