

CIRCA: Towards a Modular and Extensible Framework for Approximate Circuit Generation

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- Motivation
- Related Work
 - Classification
 - Requirements & Goals
- The CIRCA Framework
 - Concept
 - Current State: Implementation & Exemplary Results
- Conclusion & Outlook

- Approximate Computing (AC) on circuit level
 - AC exploits gap between required and provided computational accuracy
 - Trade off computational accuracy against area, delay, or energy consumption
- Large approximation space for complex Circuits
 - Large amount of possible approximation candidates
 - Effects of approximations become non-intuitive
- Demand for an automated approximation process

Related Work: Classification

Category	SASIMI [1]	SALSA [2]	AIG RW [3]	ABACUS [4]	SCALS [5]	ASLAN [6]
Circuit Type	Input					
Input Model						
Error Model						
Search Method	Generation/synthesis					
AC Technique						
Quality Assurance						
Output	Output					
Output Model						
Target Technology						
Publicly Available	Availability					

Related Work: Classification

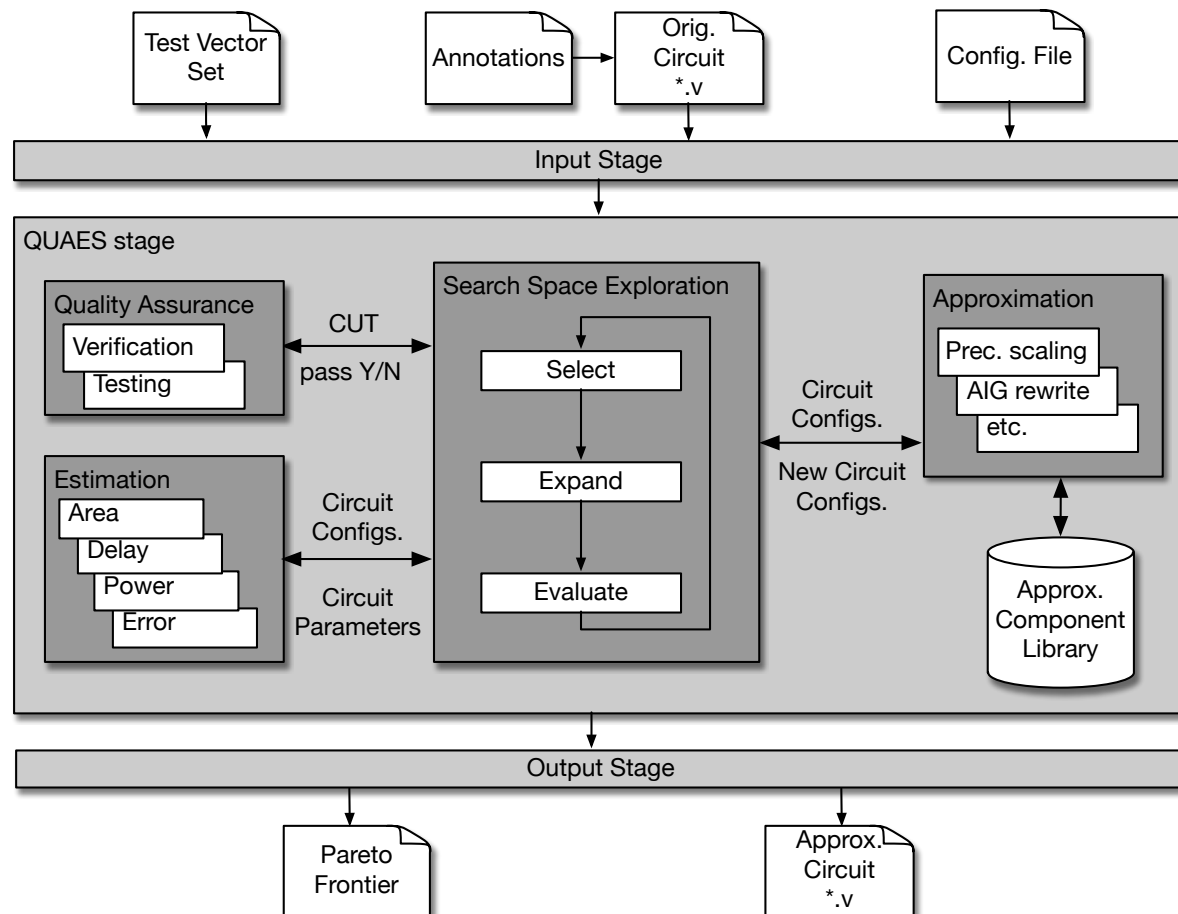
<i>Category</i>	<i>SASIMI</i> [1]	<i>SALSA</i> [2]	<i>AIG RW</i> [3]	<i>ABACUS</i> [4]	<i>SCALS</i> [5]	<i>ASLAN</i> [6]
<i>Circuit Type</i>	Comb.	Comb.	Comb.	Comb. + seq.(?)	Comb.	Seq.
<i>Input Model</i>	Gate netlist	Gate netlist	Gate netlist/AIG	Behavioral HDL	Gate/LUT netlist	Structural HDL + annotations
<i>Error Model</i>	Error bound	Quality function	Error bound	#Iterations	Error bound	Quality Evaluation Circuit
<i>Search Method</i>	Heuristic (hill climbing)	-	Heuristic (greedy)	Heuristic (greedy)	Heuristic (Metropolis-Hastings)	Heuristic (hill climbing)
<i>AC Technique</i>	Substitute-and-Simplify	Approx. don't care	AIG re-writing	AST transforms	Logic transforms	Precision scaling
<i>Quality Assurance</i>	Testing	By construction	Formal verification	Testing	Testing	Formal verification
<i>Output</i>	Approx. circuit	Approx. circuit	Approx. circuit	Pareto front	Approx. circuit	Approx. circuit
<i>Output Model</i>	Gate netlist	Gate netlist	Gate netlist (AIG)	Behavioral HDL	Gate/LUT netlist	Structural HDL
<i>Target Technology</i>	Std. cell	Std. cell	Technology Independent	Std. cell	Std. cell/LUT-based	Std. cell
<i>Publicly Available</i>	-	-	Yes	Yes	-	-

Related Work: Requirements & Goals

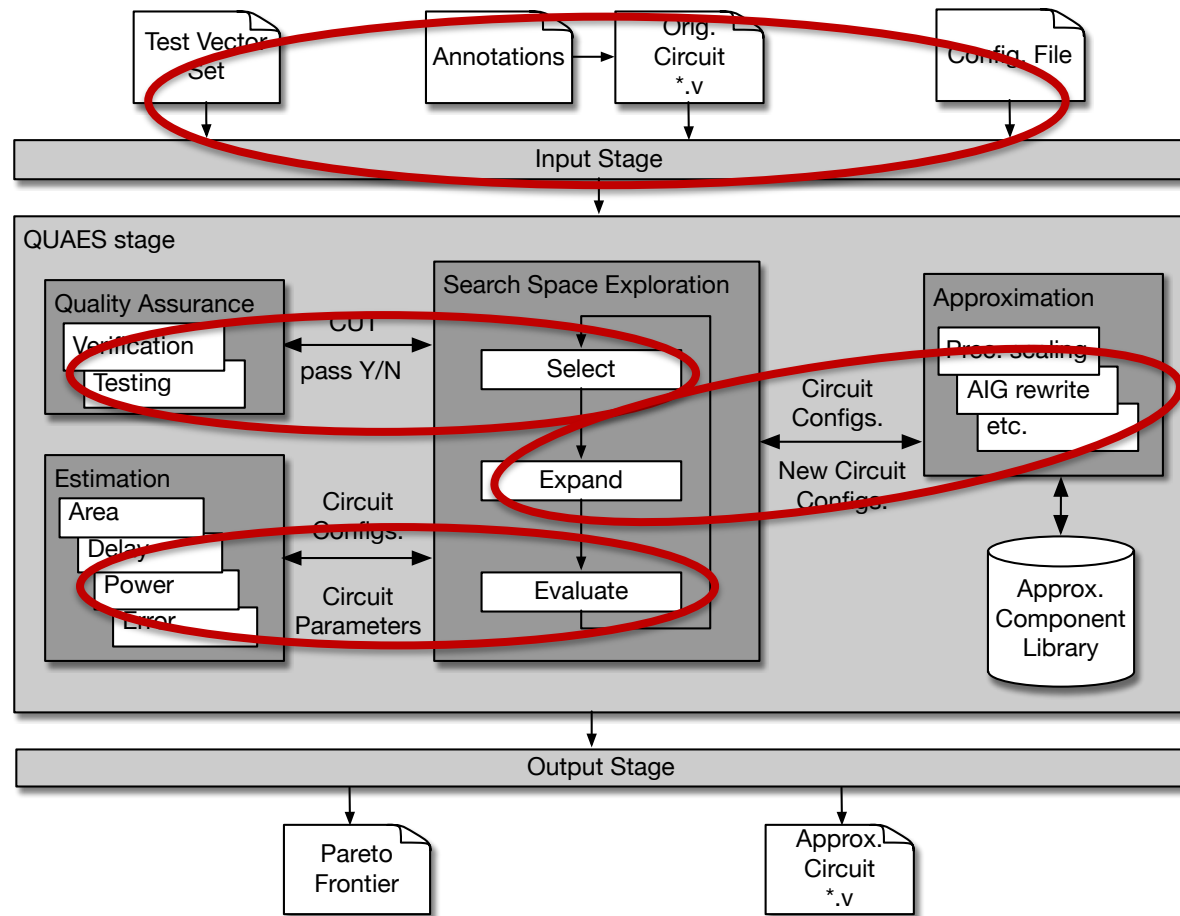
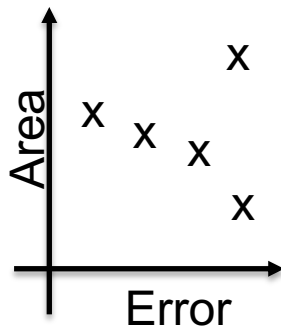
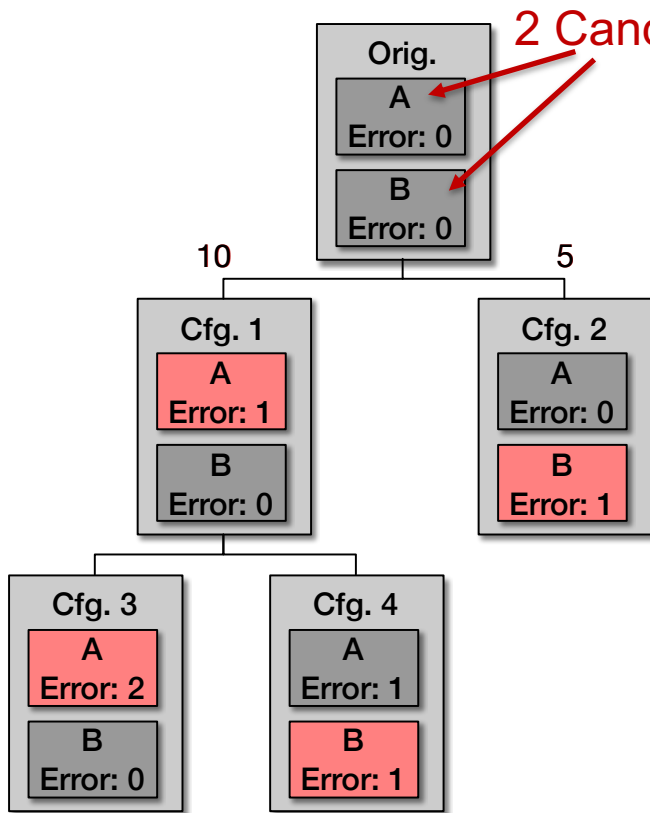
- Requirements to a framework
 - Compatible 
 - Open-source 
 - General 
 - Extensible 
 - Modular 
- Goal: Develop framework which satisfies these requirements

CIRCA: Concept

- Pre-process input data
- Perform
 - Search
 - Quality assurance
 - Approximations
 - Estimate circuit parameters

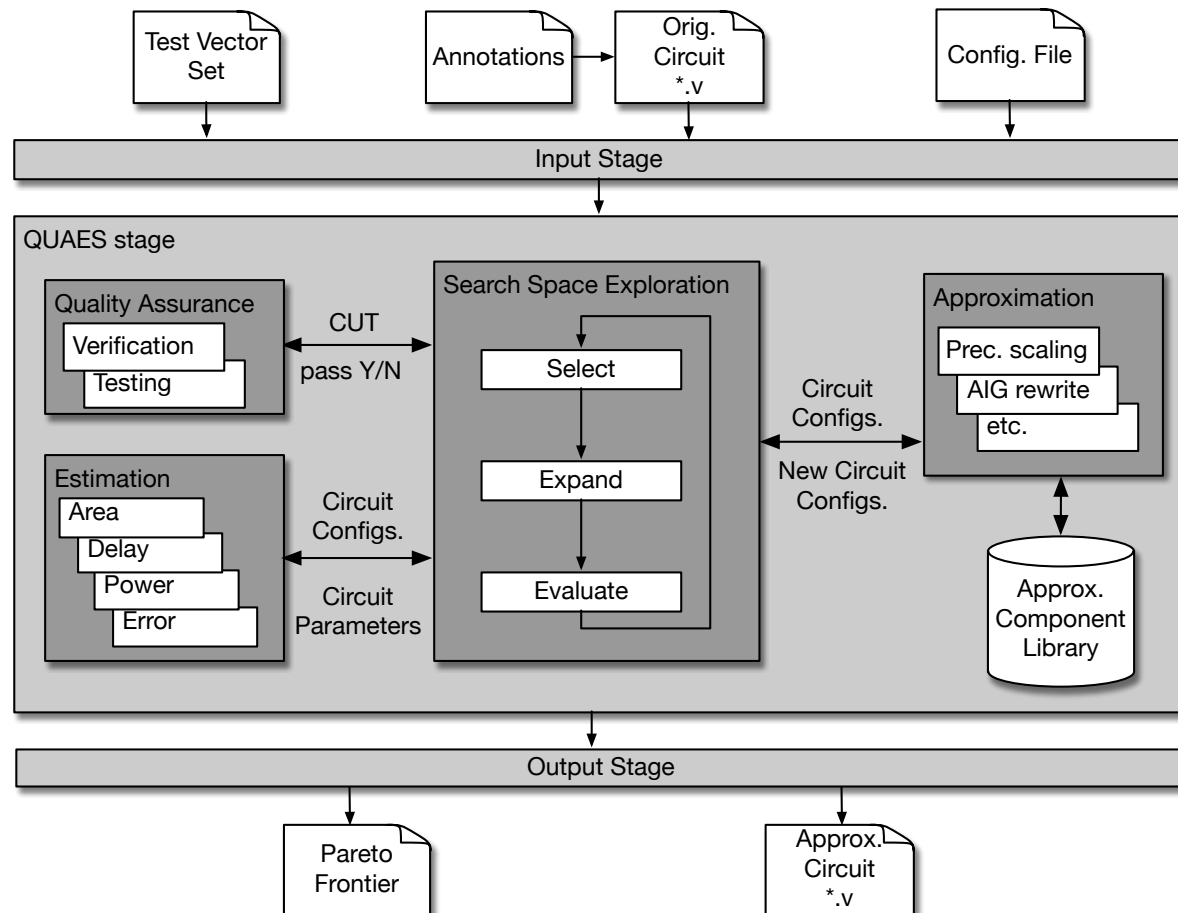


CIRCA: Concept



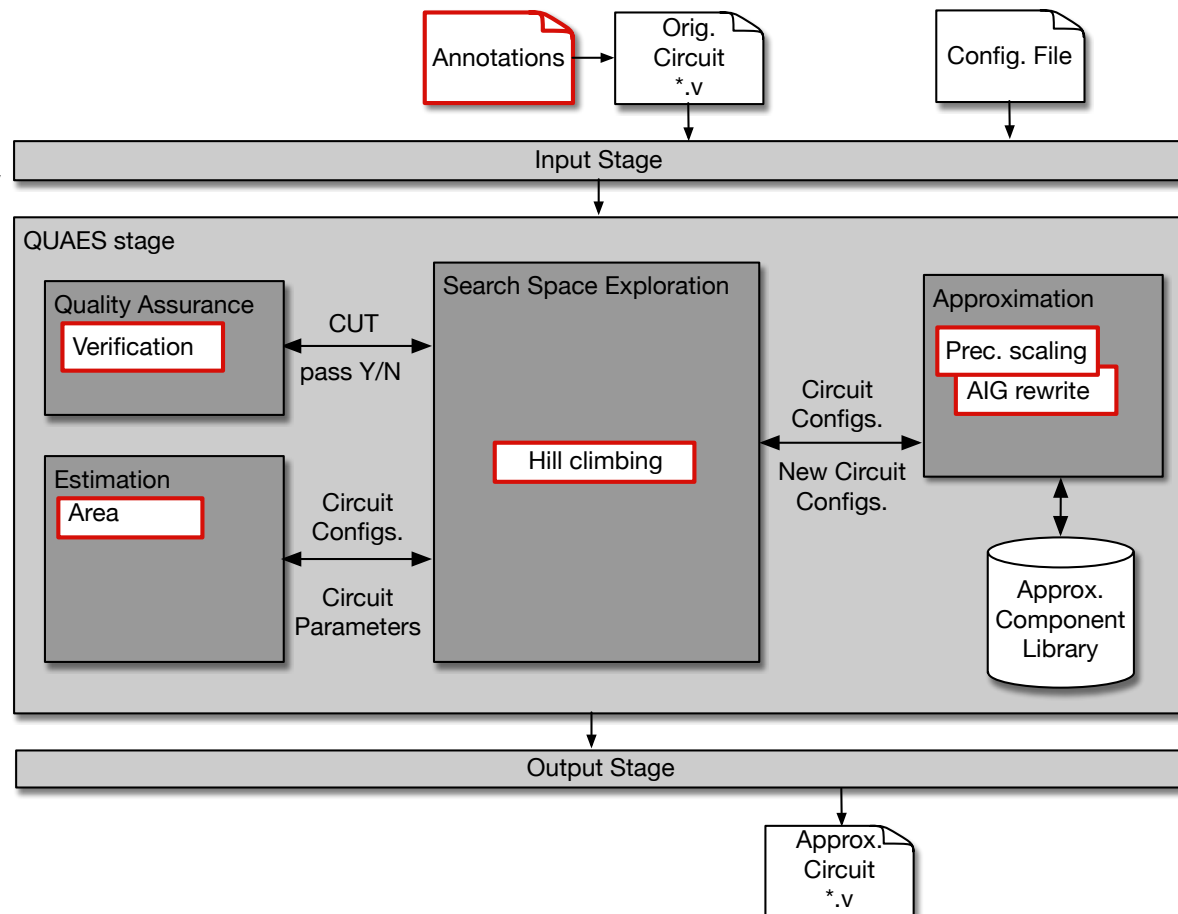
CIRCA: Concept

- Input & Output stage ensure compatibility
- User configures the approximation process
- Independent blocks
 - Modular
 - Extensible
 - General



CIRCA: Current State

- Hill climbing search
 - Heuristic considers hardware area of candidates individually
- Two approximation techniques
 - Precision scaling
 - AIG re-writing
- Formal verification assures quality
 - Inductive solver used from ABC [7]
 - Support for combinational and sequential circuits

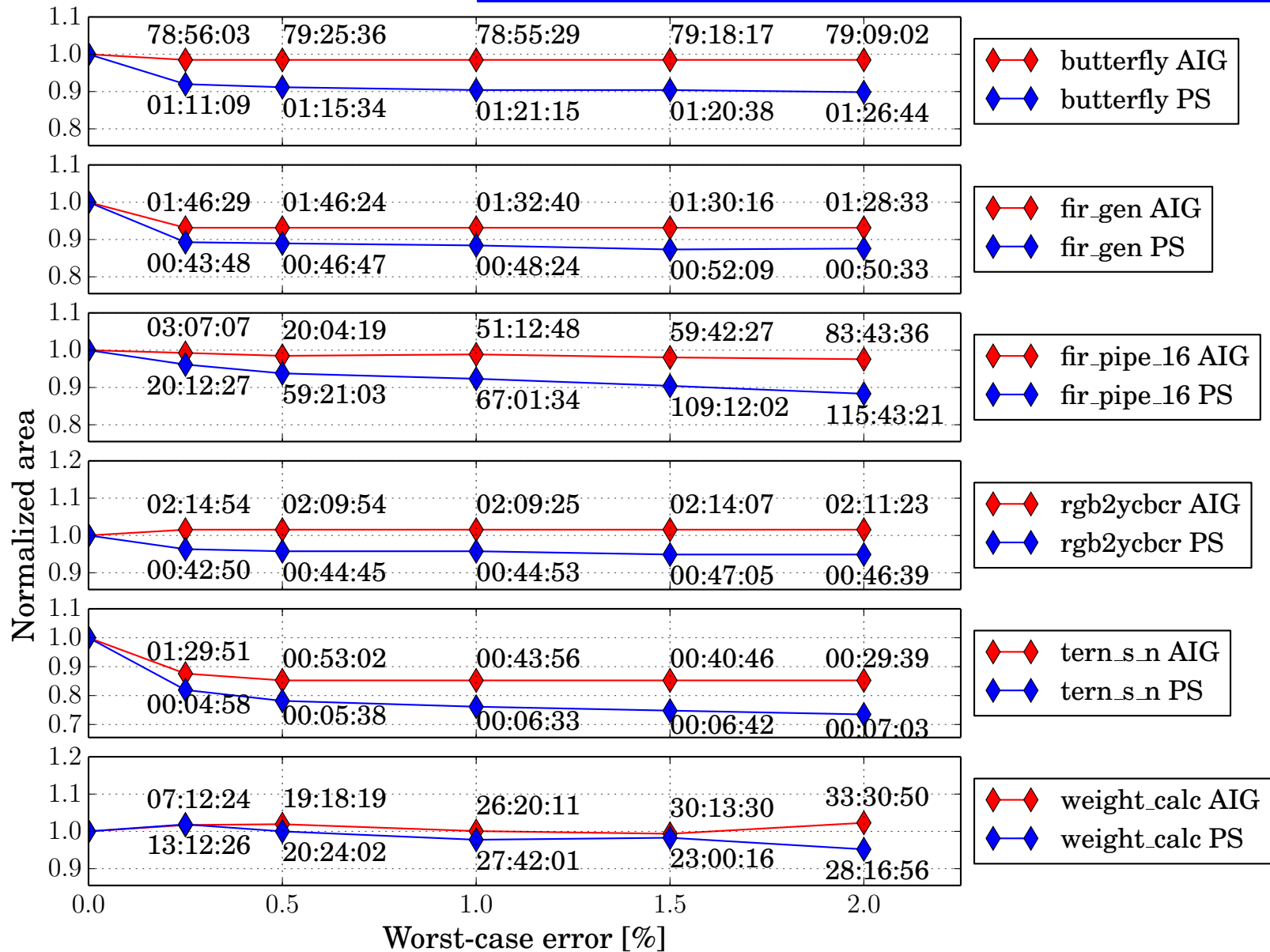


CIRCA: Exemplary Results

Circuit Name	Description	#4-LUTs	#Candidates
butterfly [8]	Operation used in FFT	7221	8
fir_gen [8]	FIR filter 4-tap	5438	7
fir_pipe_16 [9]	FIR filter 16-tap	8768	23
rgb2ycbcr [10]	Color-space transformation	4527	5
ternary_s_n [10]	Adder tree	1483	4
weight_calc	Industrial scale	1872	4

- ABC used to estimate area
- 10 runs per benchmark circuit
 - Varied worst-case error from 0.25% to 2.0%
 - Use precision scaling & AIG RW
 - Report for hardware area & runtime of CIRCA

CIRCA: Exemplary Results



- Analyzed existing frameworks
 - Identified & elaborated on requirements
- Presented concept for CIRCA
 - Modular and extensible framework
 - Showed current state & initial experimental results
- CIRCA enables comparing studies in Approximate Computing
- Continue implementation
 - Investigate other search methods and approximation techniques, e.g., A^* and circuit carving [11]
 - Implement other error metrics, e.g., average case error
 - Connect to back-end synthesis tool, e.g., Synopsys Design Compiler
- Make CIRCA open-source
- Create an AC benchmark circuit set
- Develop front-end to automatically identify candidates

Thank you for your attention!

Questions?

- [1] S. Venkataramani, K. Roy, and A. Raghunathan, "Substitute-and-simplify: A unified design paradigm for approximate and quality configurable circuits," in *Proceedings of the Conference on Design, Automation & Test in Europe*, DATE'13, IEEE, 2013.
- [2] S. Venkataramani, A. Sabne, V. Kozhikkottu, K. Roy, and A. Raghunathan, "SALSA: Systematic logic synthesis of approximate circuits," in *Proceedings of the 49th Annual Design Automation Conference*, DAC'12, ACM, 2012.
- [3] A. Chandrasekharan, M. Soeken, D. Groesse, and R. Drechsler, "Approximation-aware rewriting of aigs for error tolerant applications," in *Proceedings of the 35th International Conference on Computer-Aided Design*, ICCAD'16, ACM, 2016.
- [4] K. Nepal, Y. Li, R. I. Bahar, and S. Reda, "ABACUS: A technique for automated behavioral synthesis of approximate computing circuits," in *Proceedings of the Conference on Design, Automation & Test in Europe*, DATE'14, IEEE, 2014.
- [5] G. Liu and Z. Zhang, "Statistically certified approximate logic synthesis.," in *Proceedings of the 36th International Conference on Computer-Aided Design*, ICCAD'17., IEEE, 2017.
- [6] A. Ranjan, A. Raha, S. Venkataramani, K. Roy, and A. Raghunathan, "ASLAN: Synthesis of approximate sequential circuits," in *Proceedings of the Conference on Design, Automation & Test in Europe*, DATE'14, IEEE, 2014.
- [7] R. Brayton and A. Mishchenko, "ABC: An academic industrial-strength verification tool," in *Computer Aided Verification* (T. Touili, B. Cook, and P. Jackson, eds.), pp. 24–40, Springer Berlin Heidelberg, 2010.
- [8] U. Meyer-Baese, *Digital signal processing with field programmable gate arrays*. Springer, 2014.
- [9] J. Luu, J. Goeders, M. Wainberg, A. Somerville, T. Yu, K. Nasartschuk, M. Nasr, S. Wang, T. Liu, N. Ahmed, K. B. Kent, J. Anderson, J. Rose, and V. Betz, "VTR 7.0: Next generation architecture and CAD system for FPGAs," *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, vol. 7, pp. 6:1–6:30, July 2014.
- [10] D. Lundgren, "OpenCores jpegencode." https://github.com/chiggs/oc_jpegencode. Accessed: 2018-05-25.
- [11] [1] I. Scarabottolo, G. Ansaloni, and L. Pozzi, "Circuit carving - A methodology for the design of approximate hardware.," *DATE*, pp. 545–550, 2018.