PhD Position NXP Semiconductors-LIRMM

Loopback for System Testing

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Host Team :
- Institute for System Testing, the Joint Institute ISyTest between the laboratory of informatics, robotics and Microelectronics of Montpellier (LIRMM) and NXP Semiconductors Caen

Location: 25% at LIRMM Montpellier, 75% at NXP Caen

Abstract

Many micro-electronic systems are based on transceiver architecture, as represented in Fig.1. Traditionally, the test methods are core-based, resulting in long test times and introducing some risks of affecting the signal integrity. In the core-based strategy, every block is tested against its own specifications, whereas path-based testing relies on system-level parameters. This new approach has been developed for some years, and represents a first step towards a full built-in-self-test (BIST) solution, the transmitter and the receiver being path-based tested. However, the test configuration still requires RF signal generation and capture, consequently high-performance instruments, contact blocks, probe cards, and test boards. The next step will rely on the so-called loopback technique. Some blocks of the transmitting path are used to generate the stimuli applied to the receiving blocks, which act as a digitizing + processing chain. Although this technique looks very attractive to solve the RF-related issues, still a lot of progress is required before its application to commercial products.
The technical challenges may be considered twofold:

1. How to discriminate the errors generated by each block individually?

2. How to connect the transmitter to the receiver elements? In other terms, what are the (design-for-test) DfT solutions to be implemented without disturbing the application signals?

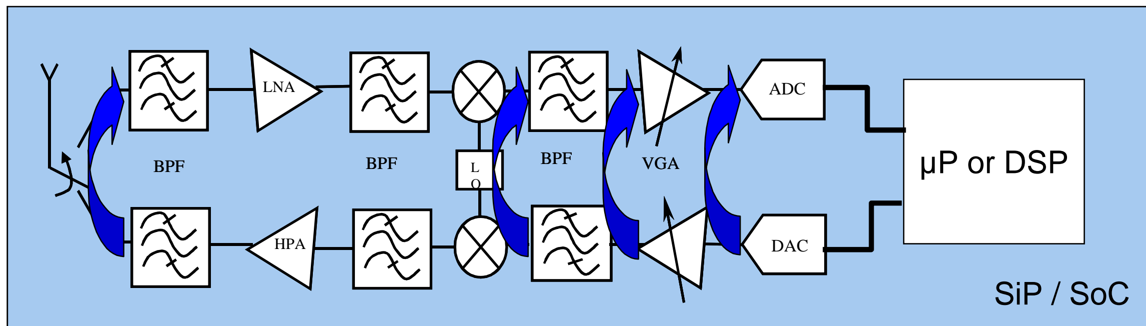

Fig.1: Loopback for system test

The objective of this PhD position is to study the loopback technique and to propose solutions of signal processing to discriminate the influence of each core on the final response. The PhD student could use the results obtained during a former PhD work on loopback at the converter (Analogue-to-Digital and Digital-to-Analogue) level. In this previous work, an original configuration (Fig. 2), so-called "Analogue Network for Converters" (ANC), was developed in combination with mathematics and signal processing, resulting in a successful discrimination of the harmonic distortion of each converter by using only digital test resources [1]. This technique received the Best Paper Award at the European Test Symposium 2006, and is validated on a lab bench.

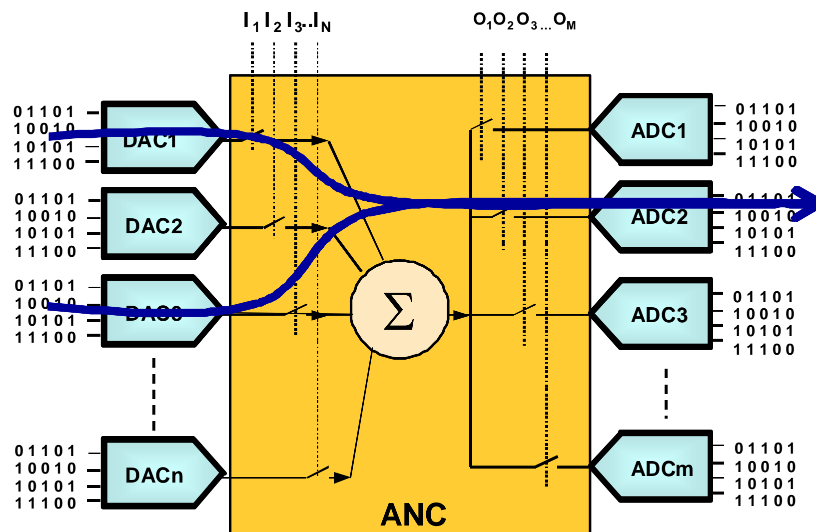

Fig. 2 : Analogue Network of Converters Principle

It was demonstrated that the embedded converters can be re-used as instruments to test the whole path, and to locate the failing cores.

In this PhD position, several solutions will be studied to test the RF and analogue blocks using embedded converters as instruments. In a first step, generic blocks, such as amplifiers, filters, mixers, etc, will be modeled as mathematical elements, then as components. The models will be validated by fault injection and detection, using the traditional test techniques. A loop-back will subsequently be inserted at different nodes of the system, following some concepts and guidelines coming from former papers, such as [2], [3], [4], or developing novel solutions. Finally, the test of a full path will be studied, including the data converters.

Skills:
The candidate should have a good knowledge of signal processing. Knowledge of MS and RF testing is a plus.

References:

[1] V. Kerzérho, P. Cauvet, S. Bernard, F. Azais, M. Comte, and M. Renovell, Analog network of converters: a DFT technique to test a complete set of ADCs and DACs embedded in a complex SIP or SoC*, Proc. IEEE European Test Symp.,* 159–164, May 2006.

[2] J. Dabrowski, and J.G. Bayon, Mixed loopback BIST for RF digital transceivers, *IEEE Int. Symp. on Defect and Fault Tolerance in VLSI Systems*, pp. 220 – 228, Oct. 2004.

[3] D. Lupea, U. Pursche, and H-J. Jentschel, RF BIST: Loopback spectral signature analysis, *Proc. IEEE Design, Automation, and Test in Europe*, pp. 478- 483, Feb. 2003.

[4] J. S. Yoon, and W. R. Eisenstadt, Embedded loopback test for RF, *IEEE Trans. on Instrumentation and Measurement*, Vol. 54, No. 5, pp 1715-1720, Oct. 2005.

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