Fully-Efficient ADC Test Technique for ATE with Low Resolution Arbitrary Wave Generators

V. Kerzérho[1 2], P. Cauvet[2], S. Bernard[1], F. Azaïs[1], M. Renovell[1] and M. Comte[1]
[1]*LIRMM, University of Montpellier / CNRS – 161 rue Ada, 34392 Montpellier, France*
[2]*NXP Semiconductors, 2 esplanade Anton Philips, Campus EffiScience BP20000 14906 Caen Cedex9, France*
{vincent.kerzerho, philippe.cauvet}@nxp.com; {bernard, azais, comte, renovell}@lirmm.fr

***Abstract* - This paper presents a technique allowing the test of ADC harmonic distortions with only low-cost ATE. Contrary to a classical DSP-based test that requires an arbitrary wave generator (AWG) on the ATE with a resolution at least 2 bit higher than the ADC under test, the proposed solution permits to test ADCs using same resolution AWG. The method involves an initial learning phase in which the characteristics of the AWG are extracted. These characteristics are then used during production test to discriminate the harmonic distortions induced by the ADC under test from the ones induced by the generator. Hardware experimentations are presented to validate the proposed approach.**

I INTRODUCTION

Analogue-to-digital (ADC) converters are nowadays part of complex systems developed for diverse domains such as medical applications, telecommunications, and consumer applications. The increasing performances of such systems induce the need of developing high-speed and high-resolution ADCs. More difficult than developing high-resolution ADCs, a relevant challenge is to have test instrument performances higher than ADC under test performances.

Indeed the common way to test ADCs in production is the DSP-based method [1]. In order to achieve such a test, there is a need of an analogue waveform generator or AWG, and a capture memory, combined with a processing unit in the tester. The accuracy of such a test depends on the test instrument performances. The most critical instrument is the analogue generator. As a rule of thumb, the signal delivered by the generator must be 10dB better than the specification limits of the ADC, to ensure acceptable test conditions. Consequently, it is commonly admitted that the generator resolution should be 2-bit higher than the tested ADC resolution.

In this context, it is clear that there is a great interest in developing new test solutions that relax the constraints on the test instrument performances.

Digital-to-Analogue Converters (DACs) are the main components of AWGs. [2][3][4][5] propose solutions for compensation of DACs non-linearity. These solutions are based on hardware modifications. Unfortunately, in our context, the DACs are already embedded in test instruments. Without any hardware modification, a digital processing technique has been proposed in [6] to compensate DACs nonlinearity. This technique could be suitable for compensation of AWGs, but the technique needs high performance instruments to implement the calibration routine.

The objective of this paper is to propose a method to test ADC harmonic distortions with only a low-cost ATE. This method relies on an initial learning phase, in which the AWG characteristics are estimated. These AWG characteristics are subsequently used to discriminate the harmonic distortions induced by the ADC under test from the ones induced by the AWG.

The paper is organised as follows. The first section presents the usual ADC test parameters and the instrumental constraints in order to achieve a correct test. The theoretical developments of the proposed method and its application for low-cost mass production test are described in section 3. Several experimental validations are then presented in section 4. Finally, section 5 gives some concluding remarks.

II ADC Test

A Test parameters

Real-life ADCs are affected by errors, usually classified in two types [1] [7] [8]

a) Stochastic errors: noise, aperture uncertainty (jitter), and coupling between analogue and digital part.
b) Deterministic errors: non-linearities, distortion.

Several parameters are defined in order to characterize and test ADCs. The traditional dynamic parameters are Total Harmonic Distortion (THD), Spurious Free Dynamic Range (SFDR), Signal to Noise Ratio (SNR) and Signal to Noise And Distortion ratio (SINAD). The critical static parameter is the Integral Non Linearity (INL). The above set of parameters can be derived [8] [9] [10] or computed [1] from the harmonic values and/or the noise value.

A very common way to evaluate these harmonic and noise values of a given converter relies on spectral analysis, i.e. to apply a single-tone sine wave to the converter input and compute the FFT on the output signal. Figure 1 shows a typical spectrum of a 12-bit ADC driven by a sine wave at frequency F0. All the values of the spectrum bins are normalized to the fundamental one. The converter errors induce harmonics, which enter in the computation of the converter parameters.

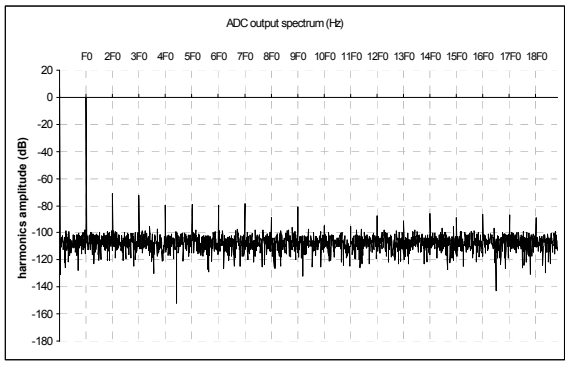

Fig 1: Spectrum of a converter output signal

Afterward, we only focus on harmonic estimation. Indeed, the method developed in [11] can be used to estimate noise features in a similar test configuration to the one proposed in this paper. This method uses one generator to supply the same test signal simultaneously for two ADCs under test. These two ADCs share the same sampling clock. Using the properties of correlated noise sources disturbing both ADCs, by simple post-processing calculations, it is possible to discriminate the noise provided by each ADC under test from the one induced by external sources.

B TEST CONSTRAINTS

1) DSP-based test method

According to the previous section, a crucial purpose of the test programme of an ADC consists in evaluating its parameters. A DSP-based method is usually used in order to measure these parameters. The typical DSP-based test architecture is described in Figure 2. The analogue stimulus is usually generated by an AWG, and the output signal is captured and stored in a logic analyzer.

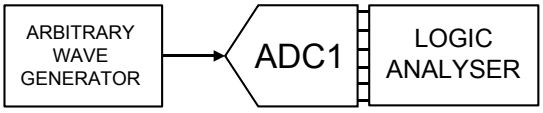

Fig 2: DSP-based test architecture

In order to achieve a correct evaluation of the ADC parameters, there are some constraints concerning the instrument performances and in particular for the AWG. Indeed, an ideal test signal is a pure sine wave, but a real-life signal applied to the converter input is obviously deteriorated by the noise and the harmonics induced by the AWG. Clearly, the noise and the harmonic levels of the test signal should be low enough to be negligible in front of the noise and harmonics induced by the converter under test. The condition for an accurate evaluation of the ADC parameters is therefore the use of an AWG with better performances than the ADC under test. The two following sections detail this condition regarding the noise and the harmonic distortions induced by the AWG.

2) Noise level induced by the AWG

The main critical part of AWG is the embedded DAC that defines AWG performances. The noise level induced by a converter is mainly due to the quantization noise linked to its resolution. Equation 1 gives the ideal SNR of a converter according to its resolution, where Res is the converter resolution:

$$SNRideal=20*Res*\log(2)+10*\log(3/2) \quad (1)$$

The following table gives the ideal SNR of a converter versus its resolution.

Converter Resolution	*Ideal SNR (dB)*
12	74
10	62
8	50

Table1: Ideal SNR vs. converter resolution

Let us consider the ideal case, i.e. a sine wave without any distortion generated by an AWG and converted by an ideal ADC. The digital signal at the output of the ADC is deteriorated by two noise sources: the noise induced by the AWG and the noise induced by the ADC. As a consequence, the SNR measured on the output of the ADC corresponds to the quadratic sum of the noise from the AWG and the noise from the ADC. The following table gives the ideal SNR of the ADC and the SNR measured on the output of the ADC versus the DAC resolution of the AWG.

Test configuration	*true ADC SNR (dB)*	*measured SNR (dB)*
8-bit ADC tested using 8-bit DAC	50.0	47.0
8-bit ADC tested using 10-bit DAC	50.0	49.8
8-bit ADC tested using 12-bit DAC	50.0	50.0

Table 2: SNR measurement, ideal ADC vs. ideal DAC/ADC set-up

This table clearly illustrates that the correct estimation of the ADC SNR is only achieved if the noise induced by the AWG is negligible compared to the noise induced by the ADC. It is obvious that if the AWG has the same resolution than the tested ADC, the measured SNR is not representative of the actual ADC SNR. A resolution at least 2 bit higher is required to have a correct estimation of the ADC noise contribution.

3) Harmonic distortions induced by the AWG

The other important elements used to compute the test parameter are the harmonics. To illustrate the influence of the AWG on harmonics measurements, we only consider the second order harmonic, H2, but similar behaviour could be obtained with other harmonics. Table 3 gives an idea of H2 amplitude that could be induced by converters according to practical experiments and datasheets.

Converter Resolution	*Common H2 (dB)*
12	-88
10	-73
8	-55

Table 3: Common H2 amplitude vs. converter resolution

As previously explained, AWG consists of a DAC with harmonic distortions. Consequently if we consider a sine wave generated by an AWG and converted by an ADC, the digital signal at the output of the ADC is deteriorated by both components. In the worst case, the H2 amplitude induced by both sources can be summed. Table 4 gives the true H2 amplitude of the tested ADC, and the measured H2 amplitude considering the influence of the AWG.

Test configuration	*true H2 (dB)*	*measured H2 (dB)*
8-bit ADC tested using 8-bit DAC	-55.0	-49.0
8-bit ADC tested using 10-bit DAC	-55.0	-54.0
8-bit ADC tested using 12-bit DAC	-55.0	-54.8

Table 4: H2 measurement, ADC vs. DAC/ADC set-up

Once again, it can be seen that the correct estimation of the ADC harmonics requires the use of an AWG with a resolution at least 2 bit higher than the resolution of the ADC under test.

III METHODOLOGY

The previous section demonstrated that there are strong constraints on the test instrument performances to be able to perform classical ADC applying DSP-based method. In particular, the AWG resolution should be, at least, 2 bit higher than the resolution of the ADC under test in order to achieve a correct estimation of the ADC test parameters.

This section presents a test method that allows mass production testing of ADC harmonic distortions using low-cost testers. By low cost testers, we mean testers that contain standard-performance AWGs that would be not efficient enough to apply a classical DSP-based test. The theoretical fundamentals are given in the first part. The next section describes the first step of the method that consists in estimating the AWG harmonic contribution. The last section is dedicated to the production test stage in which ADCs are tested using a post-processing calibration of the AWG.

A Theoretical fundamentals

Let us consider a sine wave applied to an ADC. Using a Fourier series expansion, the output signal can be expressed by Eq. (2). In this equation we distinguish the sampled sine-wave x(n) that would be obtained if the ADC is ideal and the sum of all the harmonic values introduced by static and dynamic non-linearity of the converter [8].

$$s(n) = x(n) + \sum_{k\geq 0} H_k^{converter} \cos(k(\theta_n + \theta_0) + \theta_k) \qquad (2)$$

n is the sample index, θ_0 the initial phase shift, θ_k the phase shift induced by dynamic non-linearity, the amplitude of the k^{th} harmonic, and θ_n is the nominal sampling phase given by:

$$\theta_n = 2\pi\left(\frac{P}{M}\right)n \qquad (3)$$

where P is the number of cycles and M the number of samples in the test record.

In the following of the paper, we will restrict our study to static non-linearity contributions. This context is not valid for all converter architectures but can be verified for architectures using sample-and-hold stage. The problem of dynamic non-linearity will be assessed in further theoretical developments. Eq. (4) is the simplification of Eq. (2) considering only static non-linearities.

$$s(n) = x(n) + \sum_{k\geq 0} H_k^{converter} \cos(k(\theta_n + \theta_0)) \qquad (4)$$

Not considering the dynamic non-linearity could deteriorate the algorithm performances, if the tested ADC is affected by dynamic non-linearity. This condition mainly rests on architectures. Indeed an ADC containing a sample-hold block should not be influence by dynamic non-linearity. This assumption has been verified in further practical experimentations.

Equation (4) may also apply to a DAC and can thus be used to express the signal generated by an AWG.

B Learning AWG harmonic contribution for post-processing calibration

According to [12] and considering a system of two DACs and one ADC connected by a set of switches and a combiner as illustrated in figure 3, it is possible to discriminate the harmonic contribution of the three converters. The idea is to exploit different configurations and test conditions in order to separate the harmonic contribution of each converter.

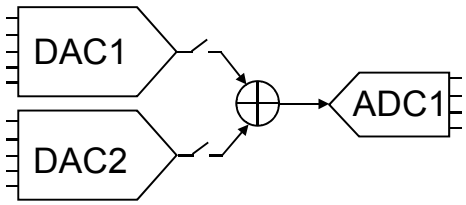

Fig. 3: Hardware set-up for test development

Let us consider a test configuration in which the output of DAC1 is directly connected to the ADC1 input. The spectrum of the output signal can be computed and we can extract the values of the harmonics H_k. Obviously, the output signal is impacted by errors of both converters. In other words, the measured spectrum includes the harmonic contribution of DAC1 as well as the harmonic contribution of

ADC1. According to (4), setting a zero initial phase shift, we can write the following equation:

$$H_k^{measure} = H_k^m = \left(H_k^{DAC1} + H_k^{ADC1}\right) \quad (5)$$

In this equation, we assume that amplitudes of harmonics created by the DAC are negligible with respect to the fundamental amplitude of the signal. In this way, we can consider that the ADC is driven by a single tone signal.

Eq. (5) establishes a relation between the harmonic contributions of the two converters involved in the test configuration. In this equation, the left member is known and corresponds to the amplitude of the k^{th} spectral bin measured at the output of the ADC, while the right member represents the unknowns.

This small example demonstrates the relationship between one configuration and its resulting equation, which leads to the fundamental idea of the new test method. By using different configurations - DAC1/ADC1 or DAC2/ADC1 or DAC1+DAC2/ADC1 - we are able to obtain a set of different equations. So, with an adequate set of configurations (i.e system of five independent equations (6)), we are able to discriminate the harmonic contribution of each converter.

$$\begin{cases} H_k^{m,a} = Hdac1_k^{FS} + Hadc1_k^{FS} \\ H_k^{m,b} = Hdac2_k^{FS} + Hadc1_k^{FS} \\ H_k^{m,c} = Hdac2_k^{FS/2} + Hadc1_k^{FS/2} \\ H_k^{m,d} = Hdac1_k^{FS} + Hdac2_k^{FS/2}\cos(k\pi) + Hadc1_k^{FS/2} \\ H_k^{m,e} = Hdac1_k^{FS} + Hdac2_k^{FS/2}\cos(k\varphi_1) + Hadc1_k^{FS}\cos(k\varphi_2) \end{cases} \quad (6)$$

with $\varphi_1 = \pi - 2\arccos\left(\frac{1}{4}\right)$, $\varphi_2 = \pi - \arccos\left(\frac{1}{4}\right)$.

To develop this method, the combiner influence is neglected. Indeed the combiner used for further experimentations is a full resistive element. As a consequence noise should be the main contribution of this element. This assumption has been verified while practical experimentation. A system of a two-channel AWG has two DACs. If we connect this system to an ADC by set of switches and a combiner we obtain the set-up required for our method. Therefore, it is possible to apply this method to estimate the harmonic contribution of the AWG in the objective to perform a post processing calibration of this AWG to test ADCs.

C Mass production test using post-processing calibration

The method described in the previous section permits to estimate the harmonic contributions of the AWG and the tested ADC. Five test configurations are required to do this estimation.

After one application of the whole method, if we change the ADC and repeat the complete procedure, we will have a new test result for the ADC under test but still the same AWG contribution. In fact once the AWG is characterized, there is only one unknown in equation (5). Solving this equation, it is therefore possible to determine the harmonic contribution of every new ADC using only one test.

In summary, considering mass production test, we need to apply the five required test configurations in order to estimate the AWG harmonic contribution. Once the harmonic contribution of the AWG is known, we only need one additional test per ADC to be tested. We can then accurately estimate the harmonic contribution of the ADC under test, by performing a post-processing calibration of the AWG contribution. As a consequence for mass production test, the test time required to know the AWG contribution with the five test configurations is negligible compared to total testing time. In other words, the test time required to apply our method is completely comparable to the test time required to apply a classical ADC test but with the proposed technique we have no need of higher performances than the ADC under test for the AWGs of the ATE.

IV EXPERIMENTAL VALIDATIONS

Large sets of hardware measurements were performed to validate the proposed approach. The purpose of the experimentation is to evaluate the efficiency of our method to accurately test an ADC using an AWG of same resolution. The experimental set-up is first introduced, then the protocol is described, and finally results are presented. The performance of the proposed test strategy is evaluated by comparing the THD and SFDR results to some reference measurements.

A Experimental set-up

In order to experiment the test strategy, we use a two-channel AWG, a resistive splitter/combiner and a 10-bit ADC, as presented in figure 4.

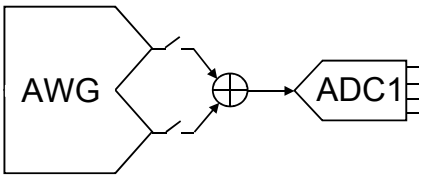

Fig. 4: Experimental test set-up

Moreover, to compare the results of our method to a classical ADC test, some reference measurements were performed using a standard test set-up with high performance analogue generator.

Finally, to demonstrate that the AWG is not efficient enough to accurately characterize the ADC dynamic performances, the classical DSP-based method has been implemented by directly connecting one output of the AWG to the input of the ADC. Table 5 presents the results of this test in comparison with the reference measurements regarding THD and SFDR test parameters.

	THD (dB)	*SFDR (dB)*
Basic AWG/ADC test	-51.6	52.5
Reference test	-68.4	63.5

Table 5: Tests results for the AWG/ADC configuration vs. reference test set-up

An error of more than 16dB is observed on the estimation of the THD, and more than 11dB on the estimation of the SFDR. This clearly demonstrates that the AWG is not efficient enough to set up an accurate DSP-based test.

B Experimental protocol

In order to validate the method, four ADCs of the same batch were tested. These four samples were chosen in order to represent a significant population of converters considering the SDFR and THD variations. Indeed these samples have THD varying from -60.5dB to -68.3dB and SFDR varying from 63.3dB to 70.3dB.

Each one of these four ADC has been tested with a classical ADC test procedure to obtain reference measurement. The test was performed ten times to estimate the repeatability of the technique. The evaluated dynamic parameters are the THD and the SFDR given by:

$$\mathrm{THD(dB)} = 10 * \log_{10}\left(\frac{\sum_{10}^{h=2} a_h^2}{a_1^2}\right) \quad (7)$$

$$\mathrm{SFDR(dB)} = 20 * \log_{10}\left(\frac{a_1}{\max(a_h)}\right) \quad (8)$$

where a_1 is the amplitude of the fundamental and a_h the amplitude of the h^{th} harmonic. Harmonics from the 2^{nd} to the 10^{th} order have been considered for these computations.

Then, the proposed method has been applied considering both the 5-test procedure used in the preliminary learning phase and the 1-test procedure used during production test. As for the classical ADC test, the THD and the SFDR parameters are computed from the estimated value of the harmonic components. Again, the test was performed ten times on each ADC.

C Experimental results

1) Learning phase validation

In order to validate the learning phase that permits to characterize the AWG, the 5-test procedure has been applied for the four samples of ADC. Results are presented in table 6 that gives the estimated value of the harmonic components induced by the AWG for 2^{nd} to the 10^{th} harmonic. The last column gives the standard deviation for each harmonic considering the four estimations using the 5-test procedure with 4 different ADCs.

	ADC #1	*ADC #2*	*ADC #3*	*ADC #4*	σ
H2 (dB)	-59.5	-60.1	-58.7	-58.1	0.9
H3 (dB)	-52.0	-52.1	-52.2	-52.3	0.1
H4 (dB)	-79.7	-77.1	-86.4	-90.6	6.2
H5 (dB)	-84.1	-87.5	-90.7	-94.0	4.2
H6 (dB)	-88.7	-82.9	-84.4	-83.6	2.6
H7 (dB)	-94.5	-108.8	-107.6	-120.9	10.8
H8 (dB)	-93.5	-97.2	-87.9	-85.0	5.5
H9 (dB)	-94.9	-84.3	-91.3	-88.3	4.5
H10 (dB)	-93.7	-105.3	-87.3	-82.7	9.8

Table 6: Estimated value of the AWG harmonic components using the 5-test procedure

Analysing these results, it appears that the amplitude of the most significant harmonic components is well estimated when taking into account the different converters used during the 5-test procedure. More precisely in this experiment, the major contributors to the AWG harmonic distortion are the H2 and H3 components. Similar values are obtained for the amplitude of these components whatever the converter used during the procedure (around -59dB for the H2 harmonic and -52dB for the H3 harmonic, with a standard deviation of less than 1dB). For harmonic components with lower amplitude, results show a more important dispersions depending on the converter used during the procedure. In fact, these harmonics are nearby or below the noise floor and they are not relevant. As a consequence, even a rough estimation of these harmonics will not strongly impact the test procedure efficiency.

In summary, these results demonstrate that the 5-test procedure allows extracting with a good accuracy the amplitude of the most significant harmonic components induced by the AWG, whatever the converter used during the procedure.

2) Production test validation

Using the AWG harmonic distortion estimated during the learning 5-test procedure, we can define a post-processing on the response of the ADC under test. The objective of this section is to validate the effectiveness of this post-processing calibration of AWG in order to accurately test subsequent ADCs with only a 1-test procedure per ADC.

For this, we consider the amplitude of the harmonic components extracted with the 5-test procedure using ADC#1. Then, the 4 samples of ADC are tested using the 1-test procedure, and post-processing calibration on the response of the DUT is performed to take into account the AWG contribution. Results are presented hereafter in comparison with the reference measurements obtained using a classical ADC test setup and a high performance AWG

Table 6 gives the THD measurements for the four ADC samples, using either a classical ADC test (2^{nd} column) or the 1-test procedure with post-processing calibration (3^{rd} column). Each result is the average of five measurements. The last column gives the difference between the two measurements.

	THD reference (dB)	*THD estimation (dB)*	*Measurement difference (dB)*
ADC#1	-66.6	-67.3	0.7
ADC#2	-68.1	-66.7	-1.4
ADC#3	-62.6	-62.4	-0.2
ADC#4	-60.5	-60.6	0.1

Table 7: Average THD measurements reference test vs. 1-test procedure

Table 6 shows that the maximal difference between the proposed method and a classical ADC test is less than 1.5dB. This result is very interesting especially when we consider repeatability of the measurement for the same product on ATE that is around 1dB.

Results for the SFDR estimation are given in table 7. As for the THD measurements, we have good estimations. The estimation uncertainty (1.2dB) is in the same range of the test production scattering (1.3dB) on the SFDR measurement for the same ADC.

	SFDR reference (dB)	*SFDR estimation (dB)*	*Measurement difference (dB)*
ADC#1	68.7	67.9	0.8
ADC#2	70.1	70.0	0.1
ADC#3	67.0	66.7	0.3
ADC#4	63.3	62.1	1.2

Table 8: Average SFDR measurements reference test vs. 1-test procedure

All these results demonstrate that once the harmonic contribution of the AWG has been extracted in the initial learning phase, it is possible to accurately test the ADC dynamic parameters (SFDR and THD) using the 1-test procedure and post-processing calibration.

V CONCLUSION

In this paper, we propose an ADC test solution based on the estimation of ADC harmonics and a post-processing calibration on the test response. The method relies on a preliminary learning phase in which the AWG harmonic contribution is estimated. The AWG characteristics are then used during production test with a post-processing calibration of the test data in order to take into account the AWG contribution.

Thanks to the proposed method, it is possible to accurately measure ADC harmonics using an ATE with standard-performance AWG, whereas a classical DSP-based test requires an AWG with a resolution at least 2 bit higher than the ADC under test. This method can be associated to the 2-ADC method [11], that is suited to noise measurements in a similar test set-up as the one required to apply the novel method. Indeed using these two methods we can test all the ADC dynamic test parameters. As a consequence, one of the main benefits of the method is that it allows testing a wide range of converters with the same standard test equipment, and without the need of customising the test board for every new product. Moreover, after the learning phase, there is no additional test time compared with a classical ADC test procedure.

The theoretical developments have been made under the assumptions that the combiner has no distortion influence and the ADC is not influenced by dynamic non-linearity. The combiner influence has been verified during practical experimentations. The ADC used for practical experimentations was not influenced by dynamic non-linearity. Further theoretical developments would be done in order to take into account ADC architectures that not stop dynamic non-linearity.

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