Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier

LIRMM

PHILIPS

"Analogue Network of Converters": a DFT Technique to Test a Complete Set of ADCs and DACs Embedded in a Complex SiP or SoC

V. Kerzérho[1 2], P. Cauvet[2], S. Bernard[1], F. Azaïs[1], M. Comte[1] and M. Renovell[1]

[1]LIRMM, University of Montpellier / CNRS, France

[2]Philips France Semiconducteurs, France

UNIVERSITÉ MONTPELLIER 2 SCIENCES ET TECHNIQUES

ETS'06 – Southampton – May 2006

CNRS

Motivation

Complex SoC or SiP

- One Chip Set-top Box: 2 ADC, 6 DAC…
- Video decoder: 12 ADC, 2 DAC, …

Motivation

Testing Complex SoC or SiP

- Context:
  - ✓ Expensive ATE
    - With mixed-signal option
    - Up-to-date performances
  - ✓ Time consuming
    - Test mixed-signal circuits (converters)
    - Limited number of mixed-signal resources => no concurrent test

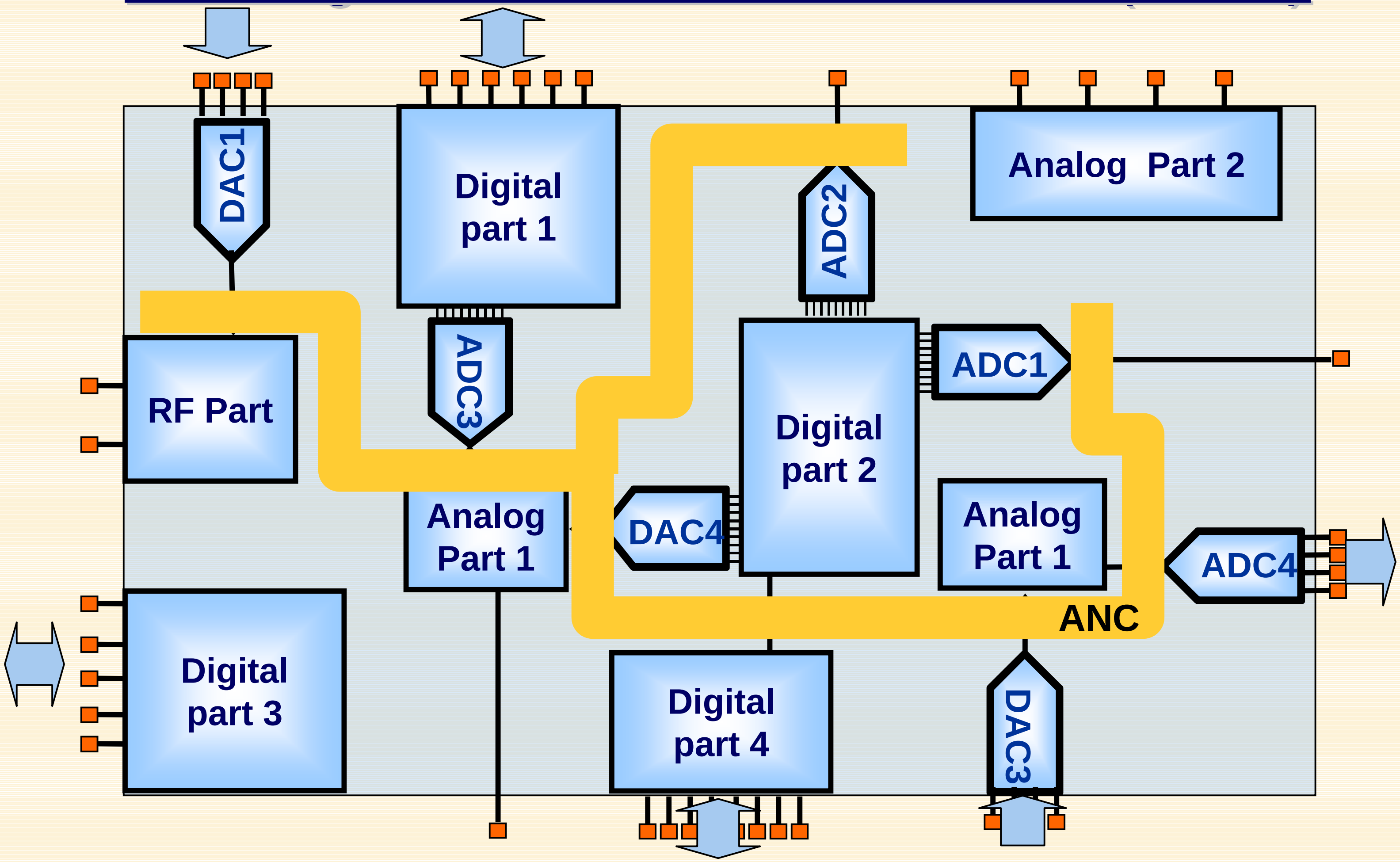
- Objective:
  - ✓ Test of converters
  - ✓ Use Low-cost ATE
  - ✓ Reduce the Testing Time
  - ✓ Guarantee Test Quality

Outline

- ANC Principle
- Test Method
- Didactic Example
- Generalization
- Results
- Conclusion

ANC Principle

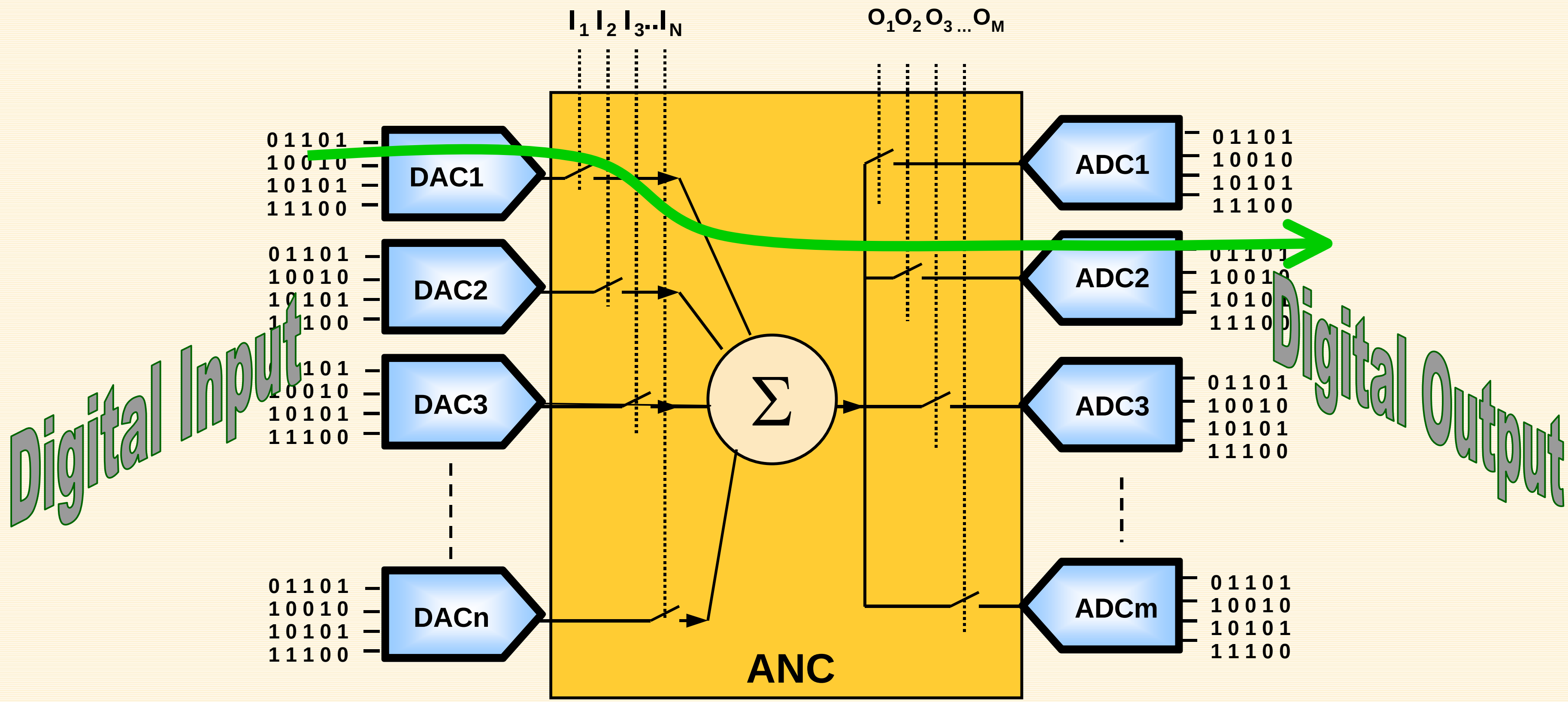
Analog Network of Converters (ANC)



Fully Digital Test of Converters

ANC Principle

Analog Network of Converter Principle

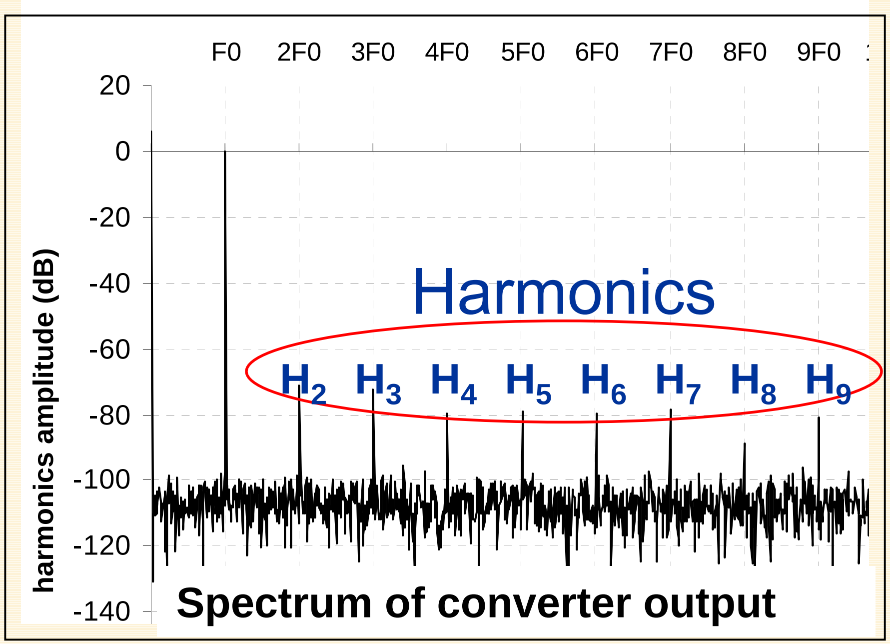


Multi-configuration ➔ Test of every converter

Outline

- ANC Principle
- **Test Method**
- Didactic Example
- Generalization
- Results
- Conclusion

Converter Parameters



- Dynamic Parameters
  - ✓ THD
  - ✓ SINAD
  - ✓ SFDR
  - ✓ ENOB

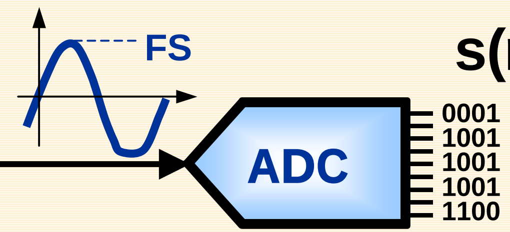
  } **Directly defined by Harmonics**
- Static Parameters
  - ✓ INL } **Direct correlation***

Harmonics => Converter Parameters

* "Comparison Between Spectral-Based Methods for INL Estimation and Feasibility of Their Implantation", V. Kerzerho, S. Bernard, J.M. Janik, P. Cauvet, Proc. IEEE International Mixed-Signal Testing Workshop, pp. 270-275, 2005.

Test Method

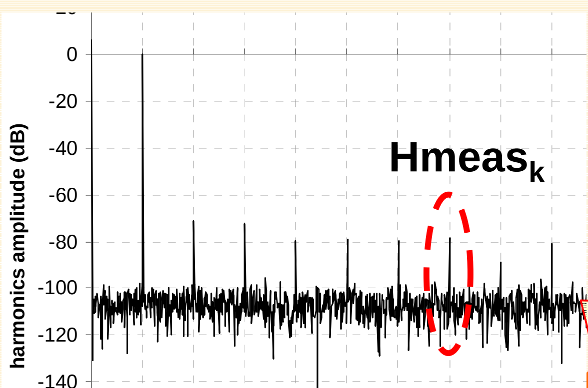
$$x(t) = FS.\cos(2\pi.f_{in}.t + \varphi_0)$$



s(n)

Hypothesis:

- Linear Phase



x(n) + quantification noise

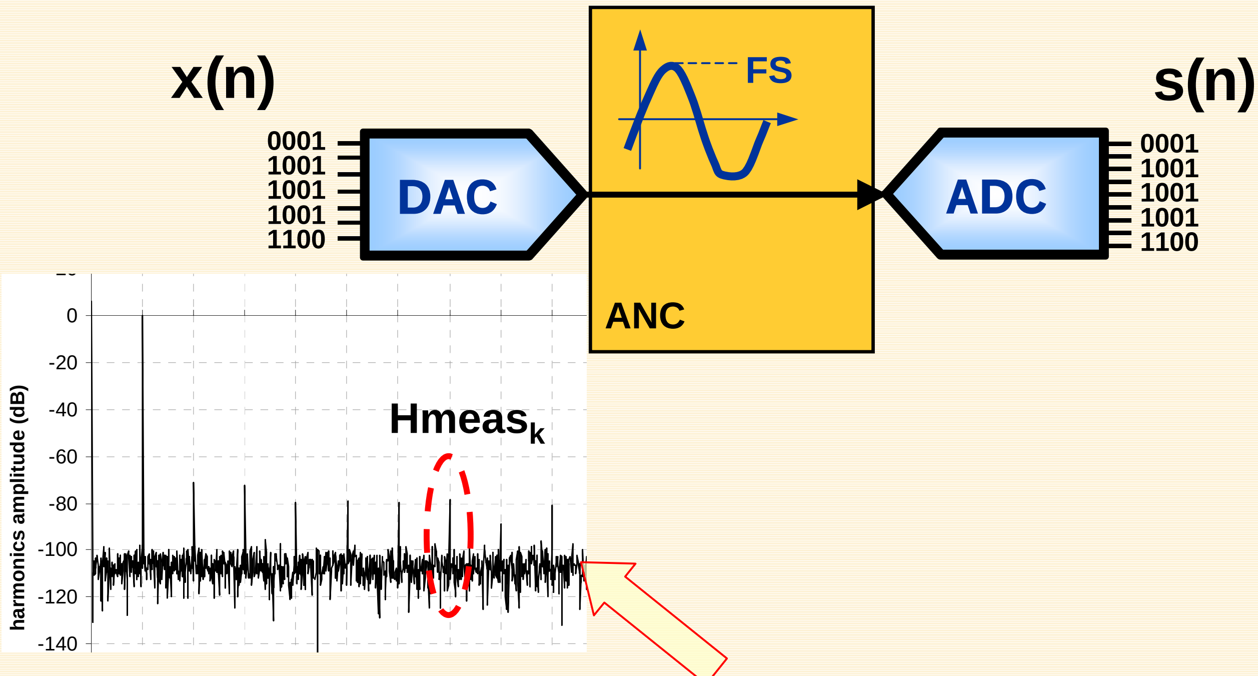
$$s(n) = x_1(n) + \sum_{k\geq 2} Hadc_k^{FS} \cos\left[k.\left(\frac{2\pi.f_{in}}{f_s} n + \varphi_0\right)\right]$$

kth harmonics of the converter

l at FS

$$Hmeas_k = Hadc_k^{FS} \quad \forall k \geq 2$$

Test Method



Hypothesis:

- Linear Phase
- Same Full Scale
- Single Tone (Hdac$_k$ << Fund)

$$s(n) = x_1(n) + \sum_{k \geq 2} \left(Hdac_k^{FS} + Hadc_k^{FS} \right) \cos\left[k.\left(\frac{2\pi.f_{in}}{f_s}.n + \varphi_0 \right) \right]$$

$$Hmeas_k = Hdac_k^{FS} + Hadc_k^{FS} \quad \forall k \geq 2$$

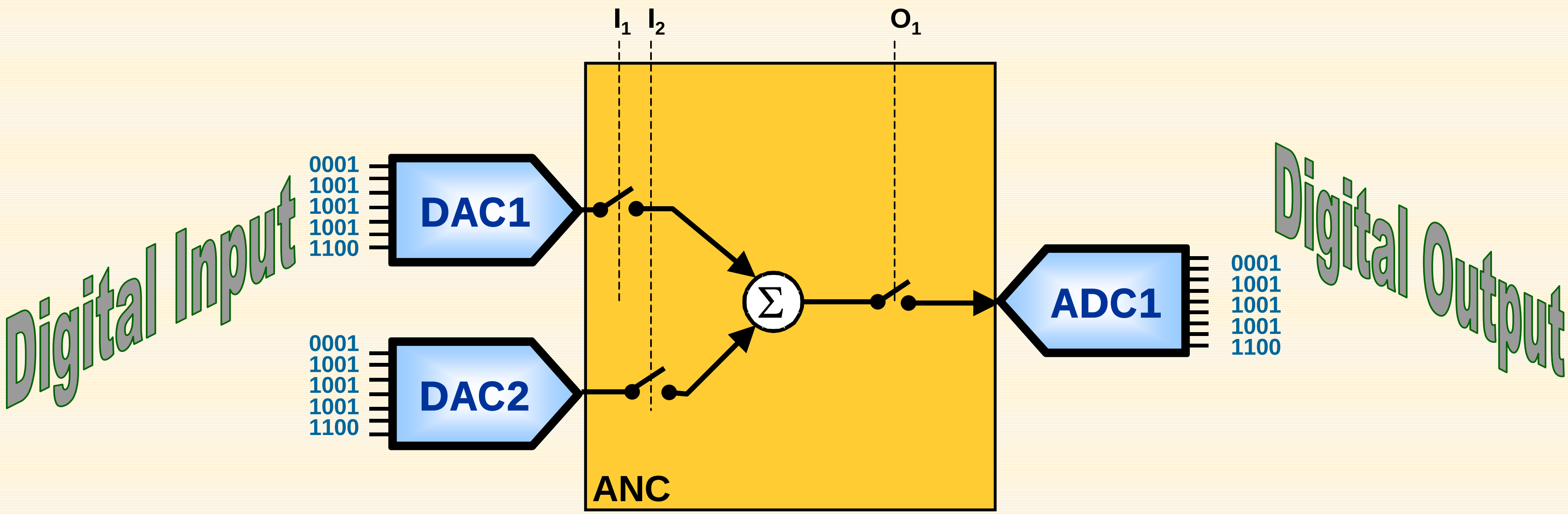
One equation but two unknowns

Outline

- ANC Principle
- Test Method
- Didactic Example
- Generalization
- Results
- Conclusion

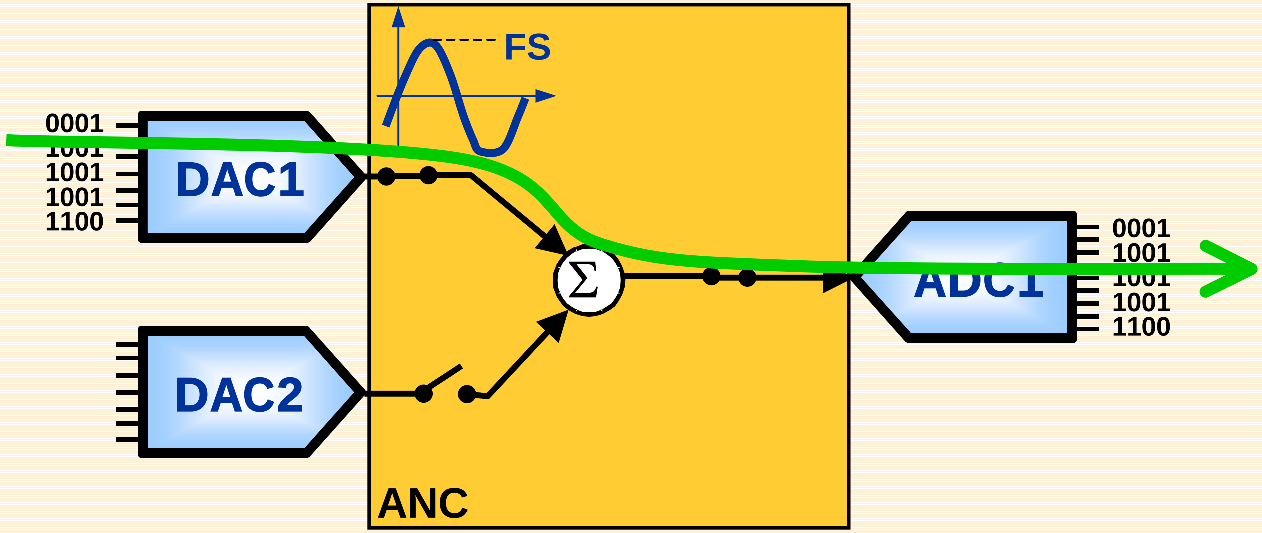
Didactic Example

Context



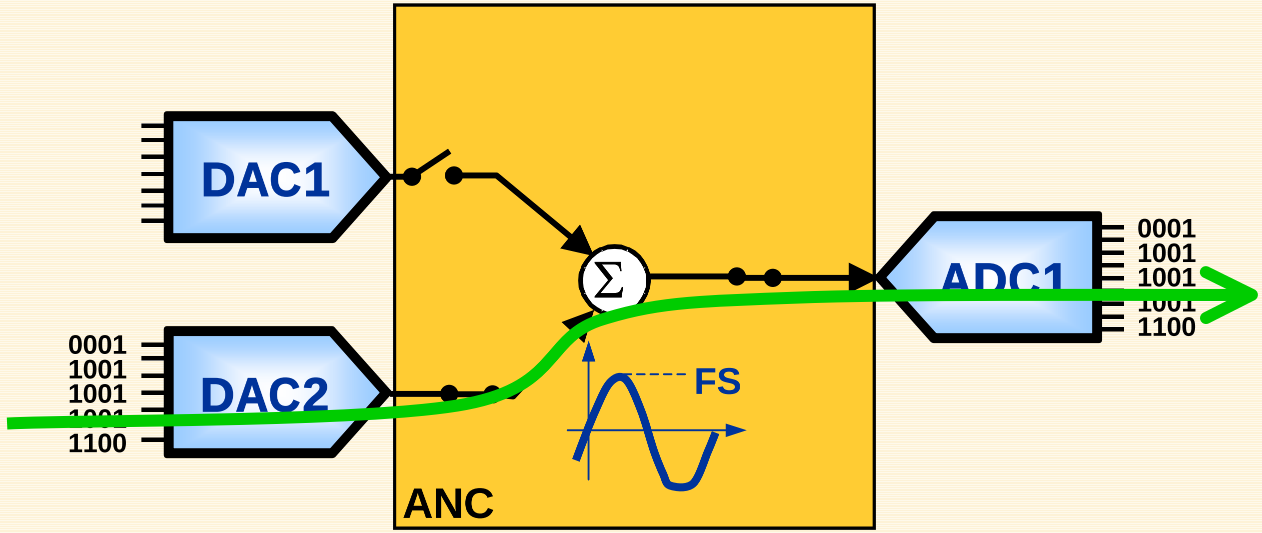
Three sets of parameters to be evaluated: $Hdac1_k^{FS}, Hdac2_k^{FS}, Hadc1_k^{FS}$

Configuration C(1,1): First equation



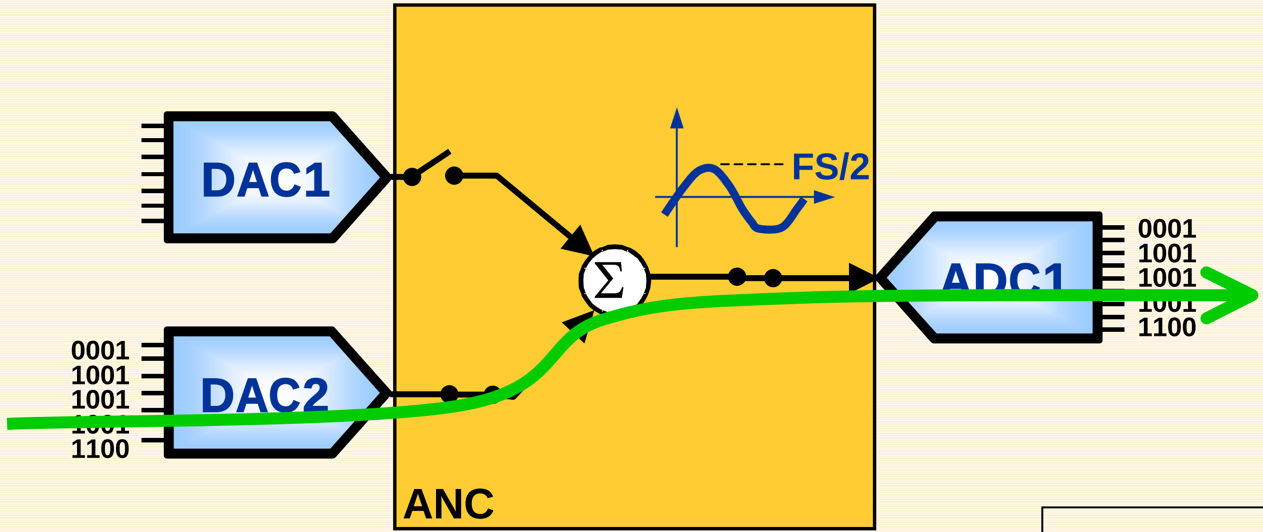
$$Hmeas1_k = Hdac1_k^{FS} + Hadc1_k^{FS}$$

Configuration C(1,1): Second equation



$$\begin{cases} Hmeas1_k = Hdac1_k^{FS} + Hadc1_k^{FS} \\ Hmeas2_k = Hdac2_k^{FS} + Hadc1_k^{FS} \end{cases}$$

Configuration C(1,1): Third equation



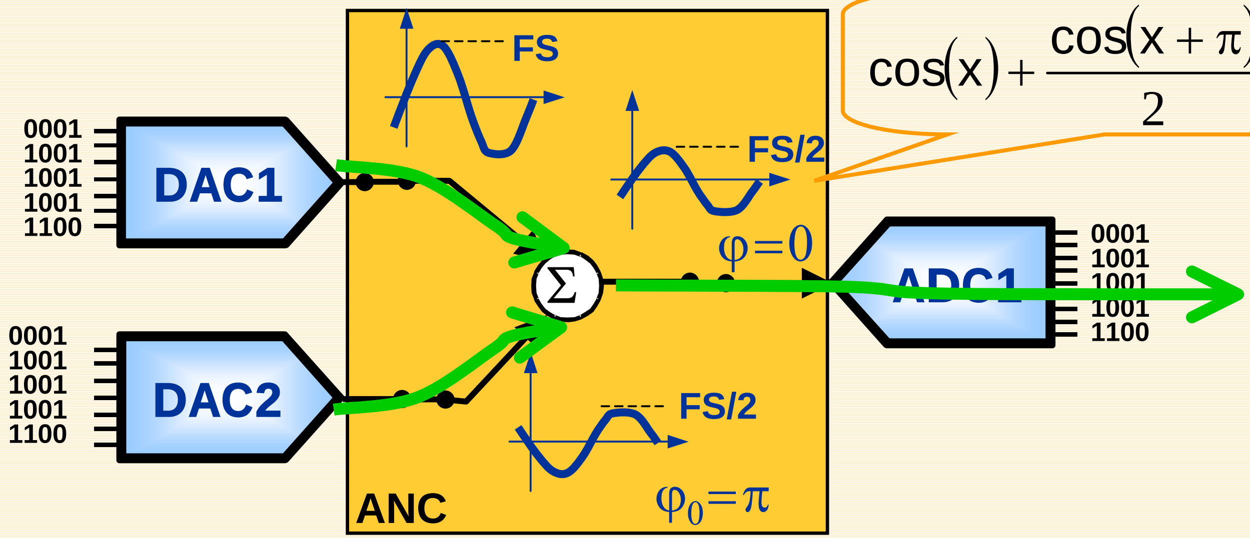
$$\mathrm{Hconv}_k^{FS} \neq \mathrm{Hconv}_k^{FS/2}$$

$$\begin{cases} \mathrm{Hmeas1}_k = \mathrm{Hdac1}_k^{FS} + \mathrm{Hadc1}_k^{FS} \\ \mathrm{Hmeas2}_k = \mathrm{Hdac2}_k^{FS} + \mathrm{Hadc1}_k^{FS} \\ \mathrm{Hmeas3}_k = \mathrm{Hdac2}_k^{FS/2} + \mathrm{Hadc1}_k^{FS/2} \end{cases}$$

New equation but two new unknowns

Didactic Example

Configuration C(2,1): Fourth equation

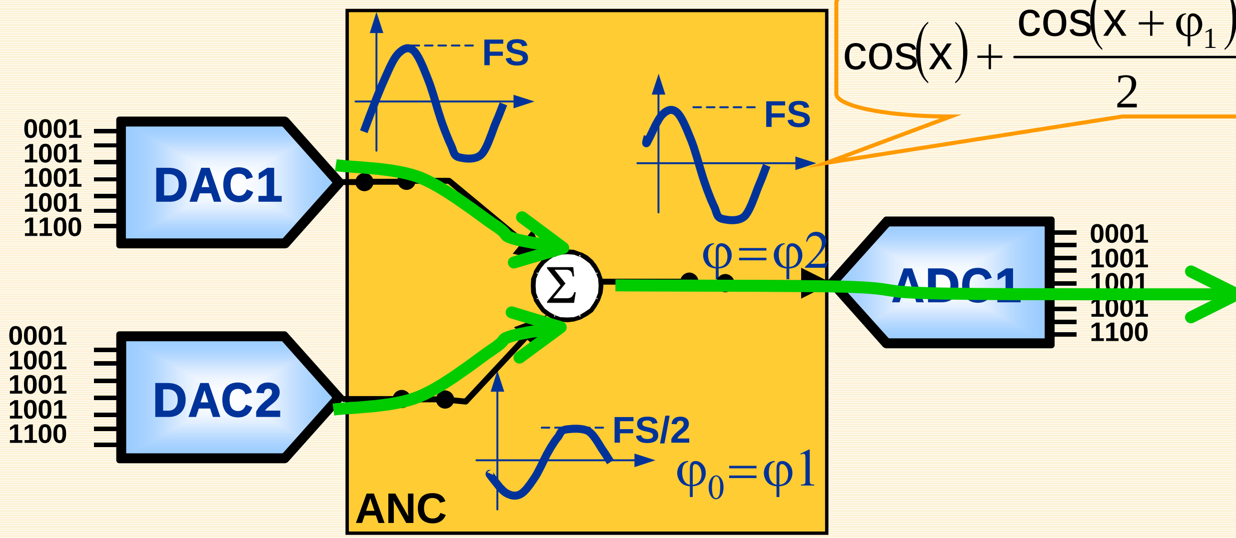


$$\cos(x) + \frac{\cos(x+\pi)}{2} = \frac{\cos(x)}{2}$$

$$\begin{cases} Hmeas1_k = Hdac1_k^{FS} + Hadc1_k^{FS} \\ Hmeas2_k = Hdac2_k^{FS} + Hadc1_k^{FS} \\ Hmeas3_k = Hdac2_k^{FS/2} + Hadc1_k^{FS/2} \\ Hmeas4_k = Hdac1_k^{FS} + Hdac2_k^{FS/2}\cos(k.\pi) + Hadc1_k^{FS/2} \end{cases}$$

Configuration C(2,1): fifth equation

$$\cos(x) + \frac{\cos(x+\varphi_1)}{2} = \cos(x+\varphi_2)$$



$$\begin{cases} Hmeas1_k = Hdac1_k^{FS} + Hadc1_k^{FS} \\ Hmeas2_k = Hdac2_k^{FS} + Hadc1_k^{FS} \\ Hmeas3_k = Hdac2_k^{FS/2} + Hadc1_k^{FS/2} \\ Hmeas4_k = Hdac1_k^{FS} + Hdac2_k^{FS/2}\cos(k.\pi) + Hadc1_k^{FS/2} \\ Hmeas5_k = Hdac1_k^{FS} + Hdac2_k^{FS/2}\cos(k.\varphi_1) + Hadc1_k^{FS}\cos(k.\varphi_2) \end{cases}$$

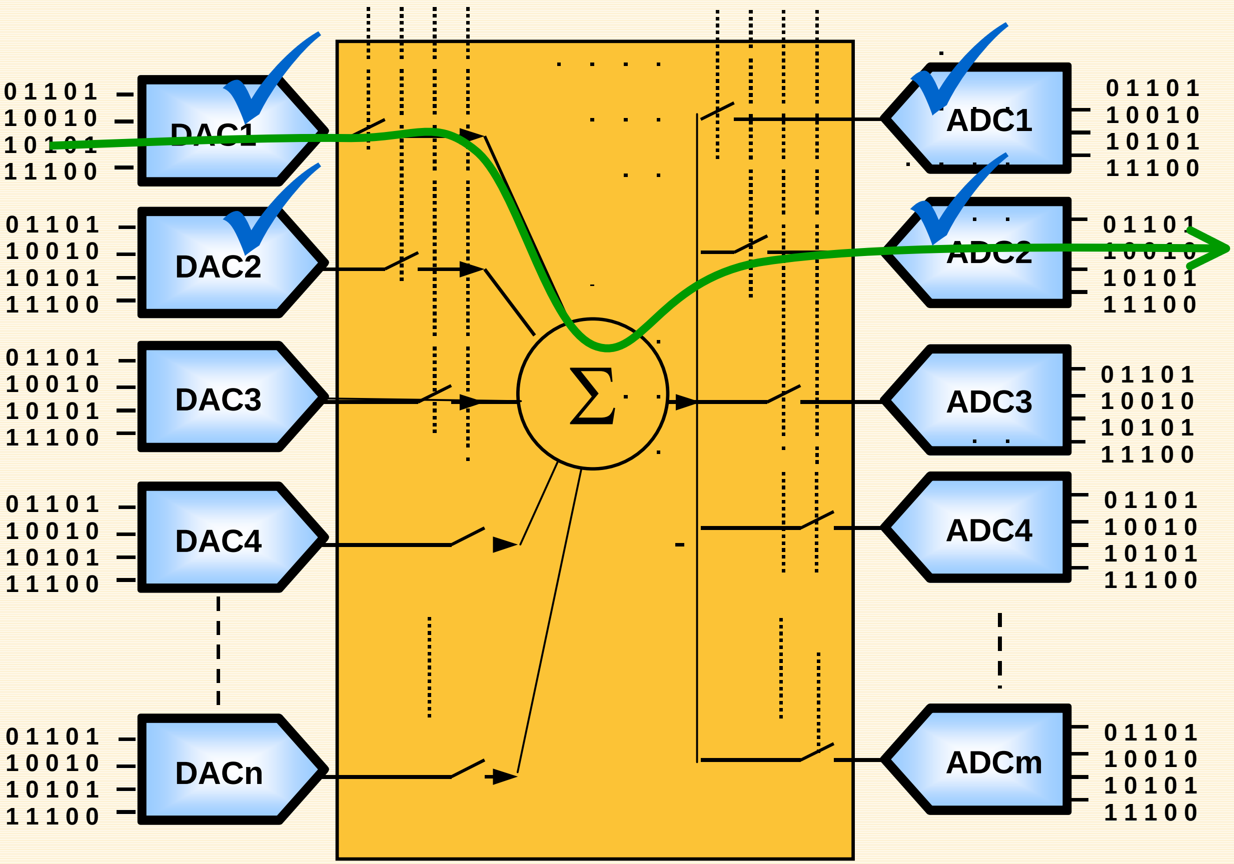
$$\begin{cases} \varphi_1 = \pi - 2.\arccos(1/4) \\ \varphi_2 = \pi - \arccos(1/4) \end{cases}$$

Outline

- ANC Principle
- Test Method
- Didactic Example
- Generalization
- Results
- Conclusion

Generalization

Test Procedure

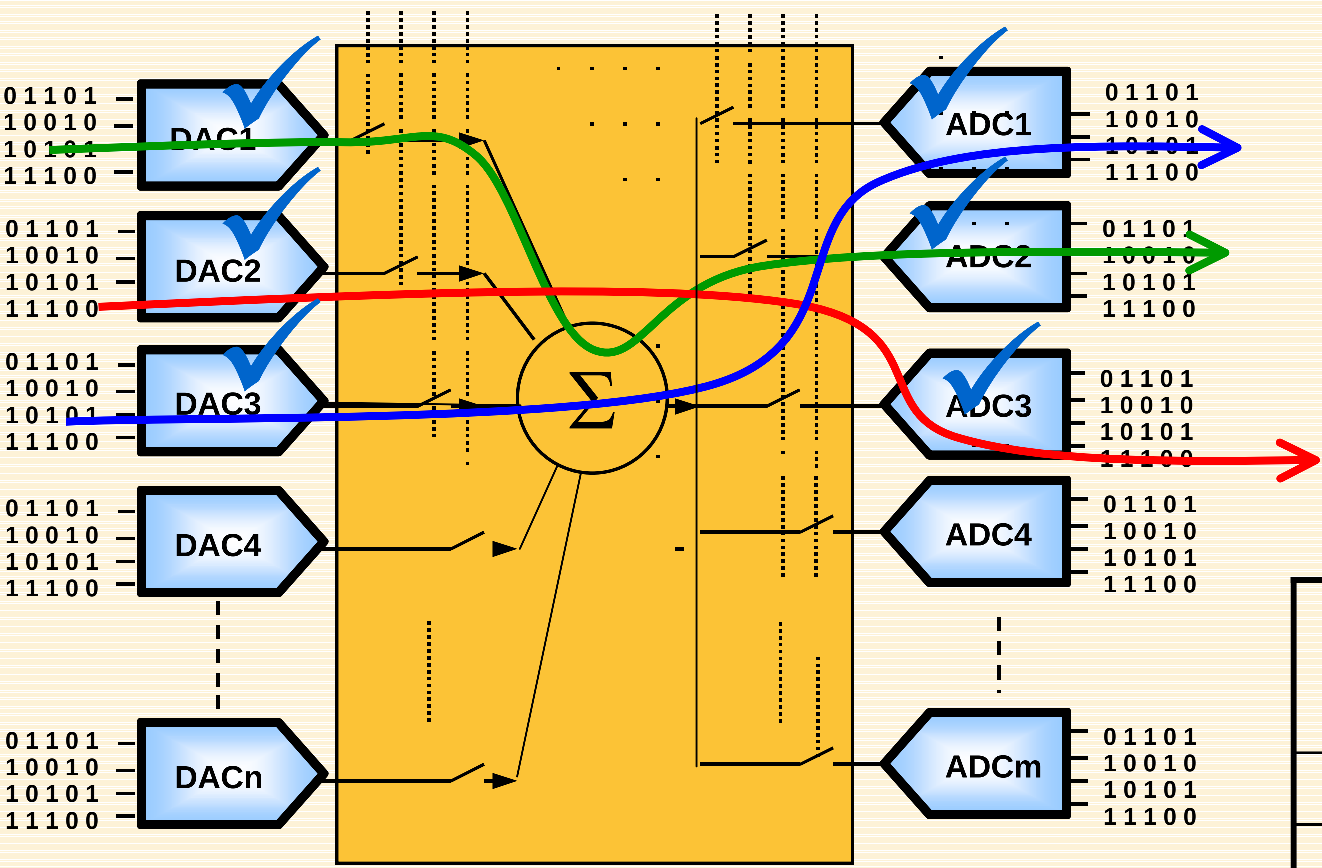


$$Hmeas_k = Hdac_k^{FS} + Hadc_k^{FS}$$

Step	# Tested convert.	Equi. test time
#1	3	5

Generalization

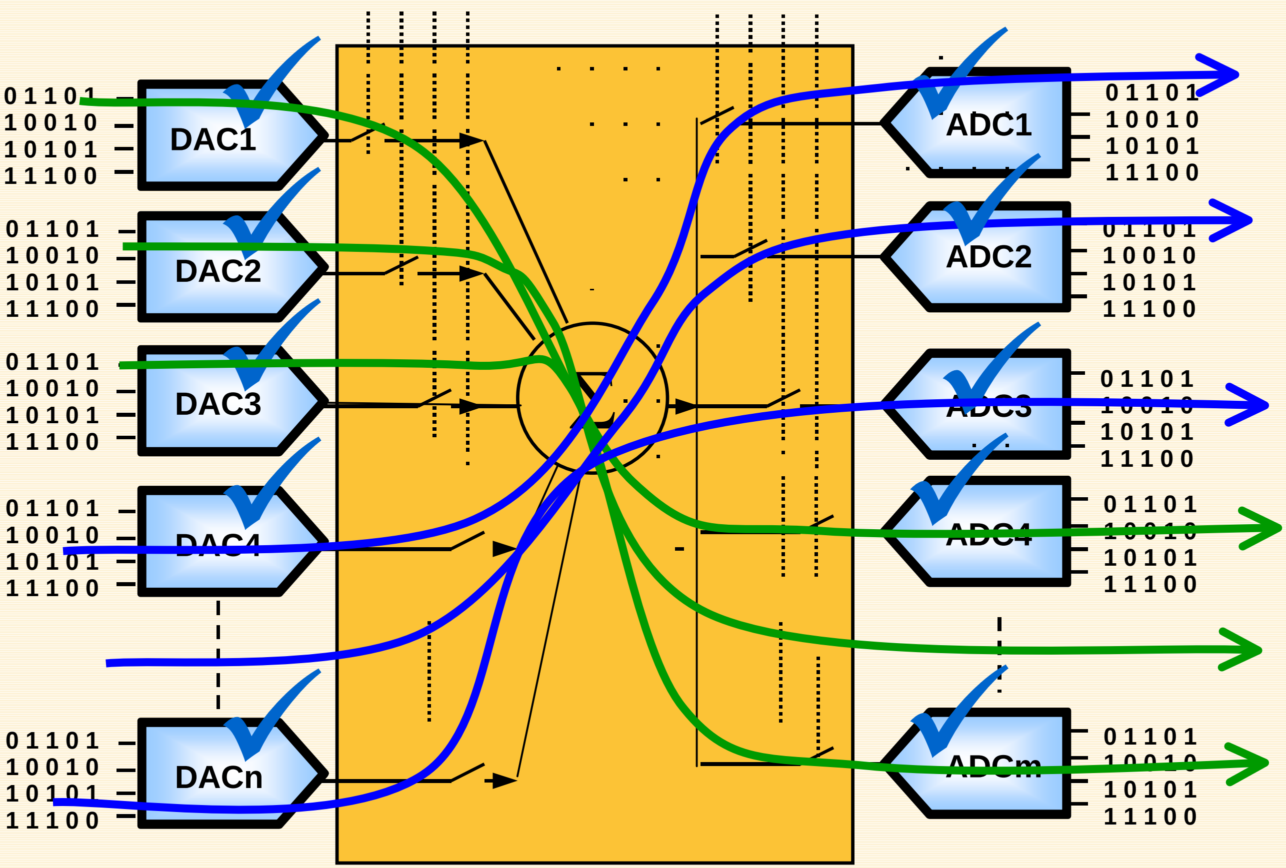
Test Procedure



Step	# Tested convert.	Equi. test time
#1	3	5
#2	3	1

Generalization

Test Procedure



Dynamic Process

Step	# Tested convert.	Equi. test time
#1	3	5
#2	3	1
#3	6	1
#4	12	1

Summary

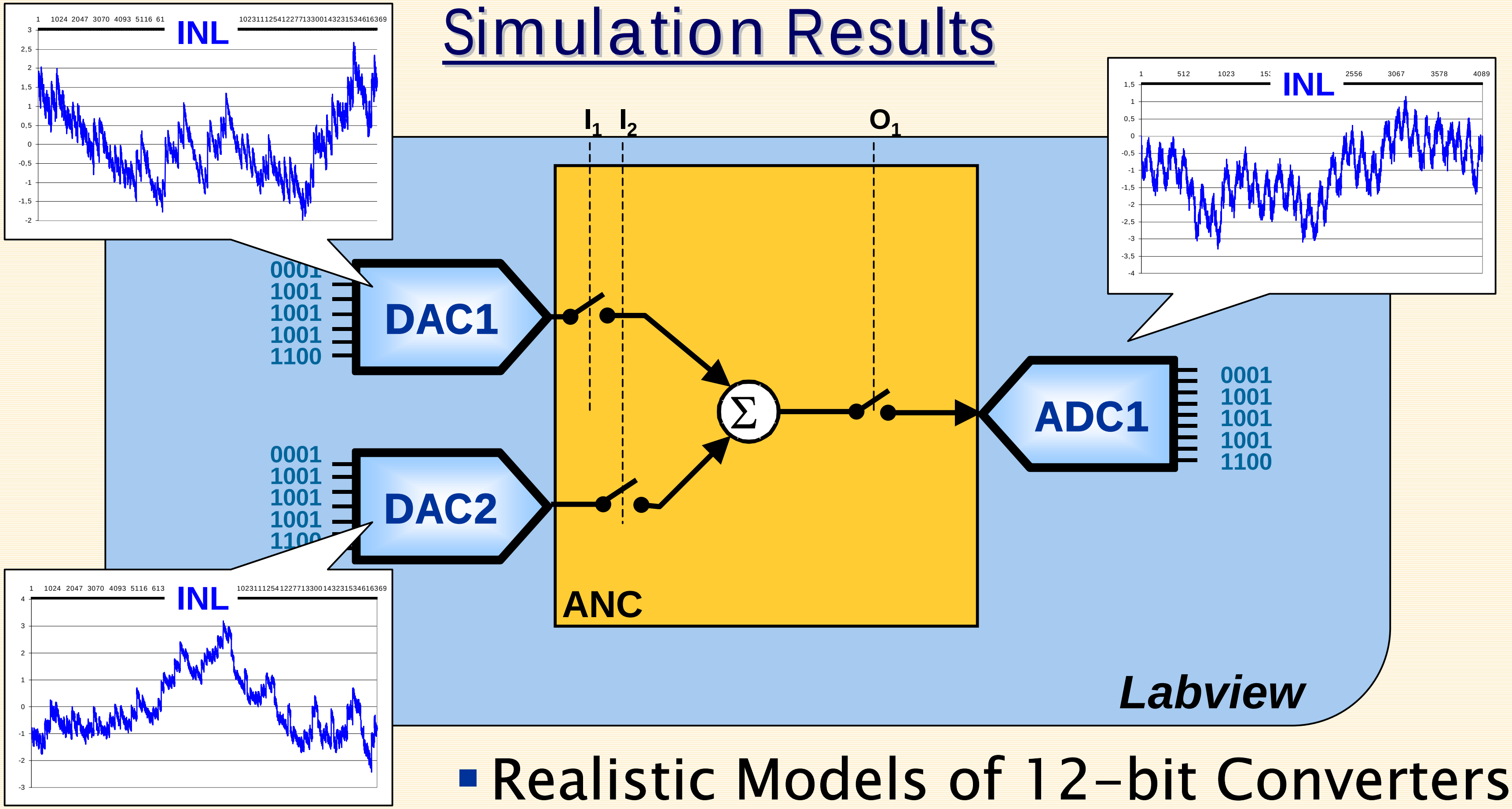
- Significant Parameters of Each Converter
  - ✓ SFDR, THD, INL…
- Low-cost ATE
  - ✓ Fully Digital Testing
- Testing Time
  - ✓ Dynamic Process + Digital resources ⇨ Concurrent testing

Outline

- ANC Principle
- Test Method
- Didactic Example
- Generalization
- Results
- Conclusion

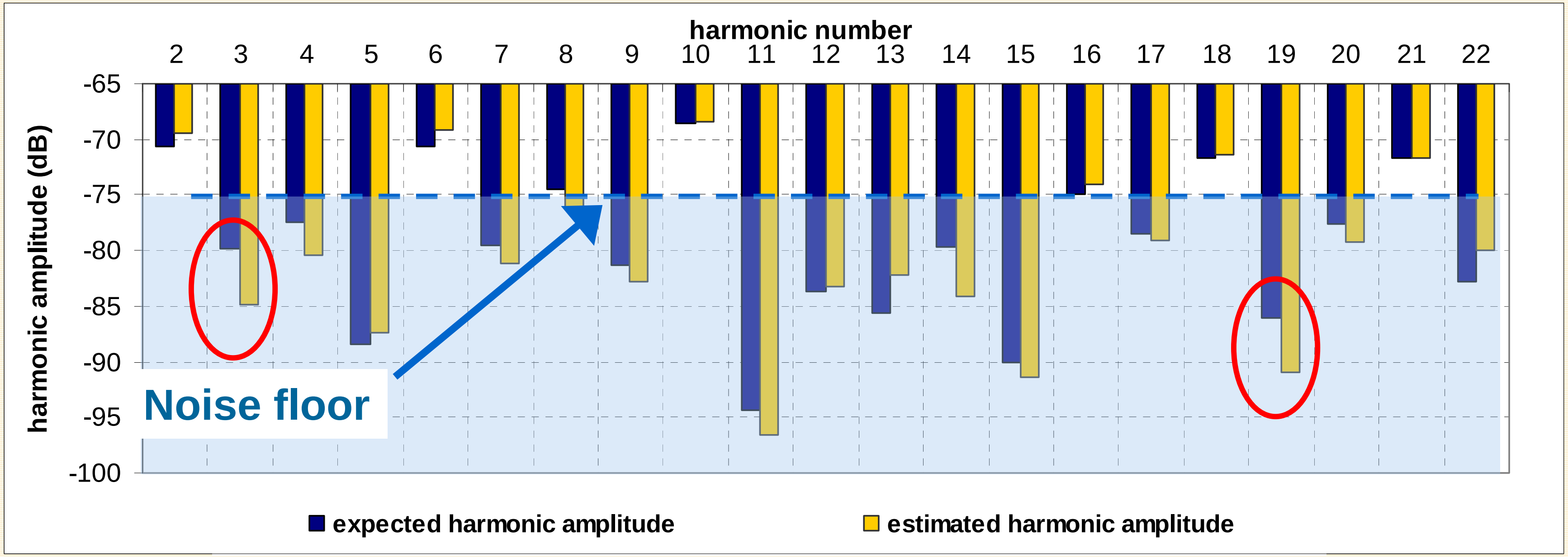
Results

Simulation Results



- Realistic Models of 12-bit Converters
  - ✓ INL from measurement on real converter
  - ✓ Jitter
  - ✓ White noise

Simulation Results: Harmonic Estimation



- On 15 different converters
  - ✓ for H_k>noise floor => max. estimation error =3.5dB

Results

Simulation Results: Parameter Estimation

Converter Number	*Wanted THD (dB)*	*THD estimation (dB)*	*THD error (dB)*	*Wanted SFDR (dB)*	*SFDR Estimation (dB)*	*SFDR error (dB)*
#1	-59.1	-59.0	-0.1	68.8	69.3	-0.5
#2	-58.0	-57.9	-0.1	69.3	69.9	-0.6
#3	-58.2	-58.2	0	67.9	67.5	0.4
#4	-64.3	-63.9	-0.4	69.4	68.9	0.5
#5	-66.7	-66.9	0.2	70.9	71.1	-0.2
#6	-61.7	-58.8	-2.9	63.4	64.2	-0.8
#7	-48.1	-48.1	0	67.1	66.3	0.8
#8	-62.7	-62.2	-0.5	65.4	64.7	0.7
#9	-60.7	-60.9	0.2	64.9	65.5	-0.6
#10	-59.7	-59.7	0	62.2	62.2	0
#11	-61.5	-61.8	0.3	64.0	65.1	-1.1
#12	-61.6	-61.4	-0.2	62.8	62.8	0
#13	-70.4	-69.6	-0.8	71.1	67.4	3.7
#14	-55.5	-55.6	0.1	65.0	65.0	0
#15	-64.0	-63.6	-0.4	68.6	68.4	0.2

Results

Simulation Results: Parameter Estimation

Converter Number	Wanted THD (dB)	THD estimation (dB)	THD error (dB)	Wanted SFDR (dB)	SFDR Estimation (dB)	SFDR error (dB)
#1	-59.1	-59.0	-0.1	68.8	69.3	-0.5
#2	-58.0	-57.9	-0.1	69.3	69.9	-0.6
#3	-58.2	-58.2	0	67.9	67.5	0.4
#4	-64.3	-63.9	-0.4	69.4	68.9	0.5
#5	-66.7	-66.9	0.2	70.9	71.1	-0.2
#6	-61.7	-58.8	-2.9	63.4	64.2	-0.8
#7	-48.1	-48.1	0	67.1	66.3	0.8
#8	-62.7	-62.2	-0.5	65.4	64.7	0.7
#9	-60.7	-60.9	0.2	64.9	65.5	-0.6
#10	-59.7	-59.7	0	62.2	62.2	0
#11	-61.5	-61.8	0.3	64.0	65.1	-1.1
#12	-61.6	-61.4	-0.2	62.8	62.8	0
#13	-70.4	-69.6	-0.8	71.1	67.4	3.7
#14	-55.5	-55.6	0.1	65.0	65.0	0
#15	-64.0	-63.6	-0.4	68.6	68.4	0.2

Experimental Results (real circuits)

12-bit ADC: TDA9910

ADC	Expected THD (dB)	Estimated THD (dB)	Estimat. Error (dB)	Expected SFDR (dB)	Estimated SFDR (dB)	Estima. Error (dB)
#1	66.4	66.0	0.4	−66.9	−66.9	0.0
#2	64.8	65.9	−1.1	−67.2	−65.6	−1.6
#3	70.4	69.4	1.0	−70.7	−72.1	1.4
#4	63.2	63.6	−0.4	−67.8	−65.3	−2.5

Conclusion

Analog Network of Converters (ANC)

- Test the Complete Set of Embedded Converters
- Low-cost ATE
  - ✓ Digital testing
  - ✓ BIST possibilities
- Reduce the Testing Time
  - ✓ Concurrent test
- Preserve Test Quality
  - ✓ Embedded resources

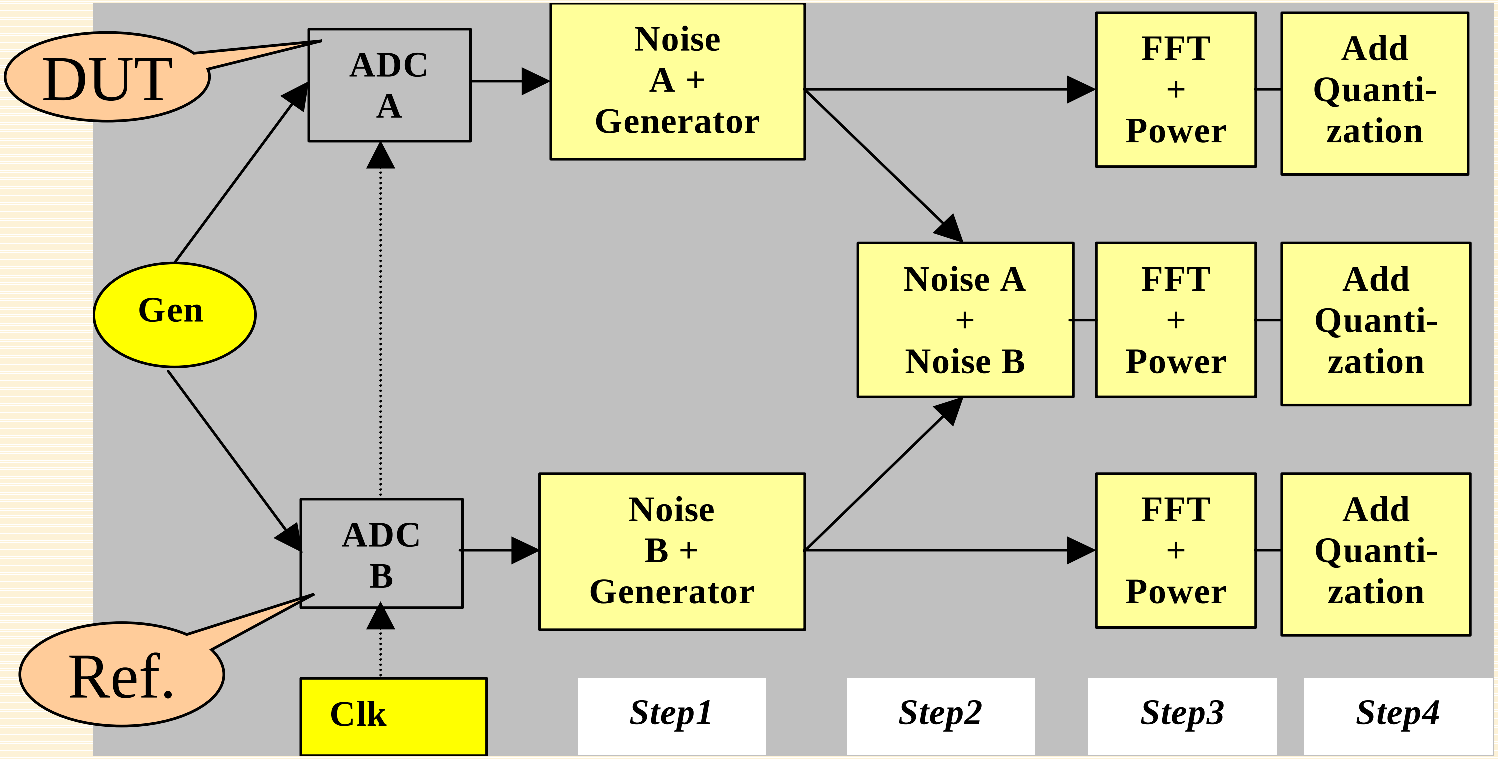
Future Projects

- DFT Implementation
- Extend the application field
- Linear Phase Requirement

Thank You
for your Attention

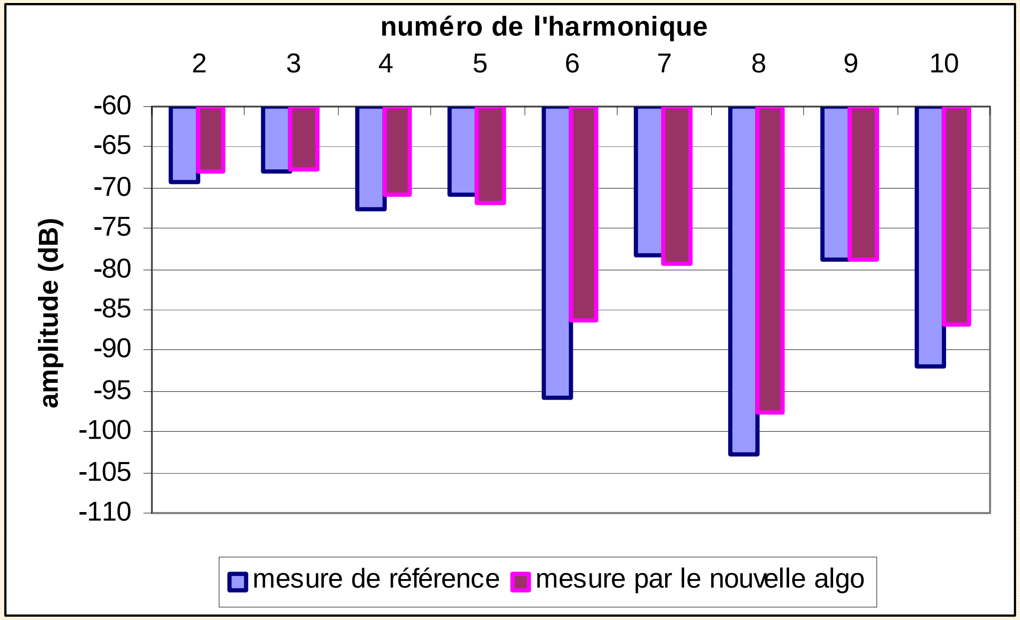
Jitter + noise compensation

- Noise is considered as a random variable
  Correlated and uncorrelated values are discriminated and processed



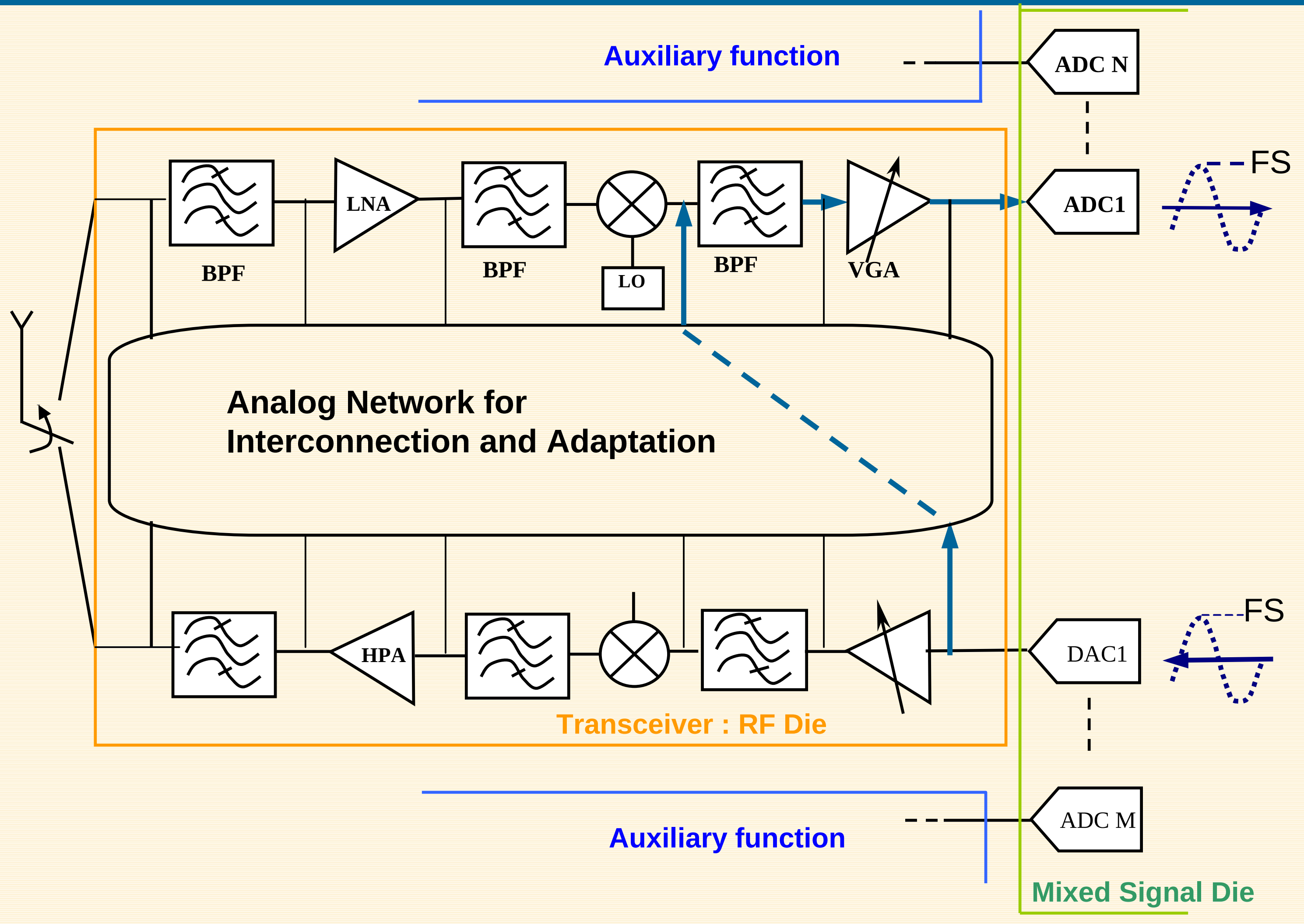
Ref: "Improving the dynamic measurement of ADC's using the 2 ADC method", P Cauvet, Teradyne Users Group 2001

Experimental Results



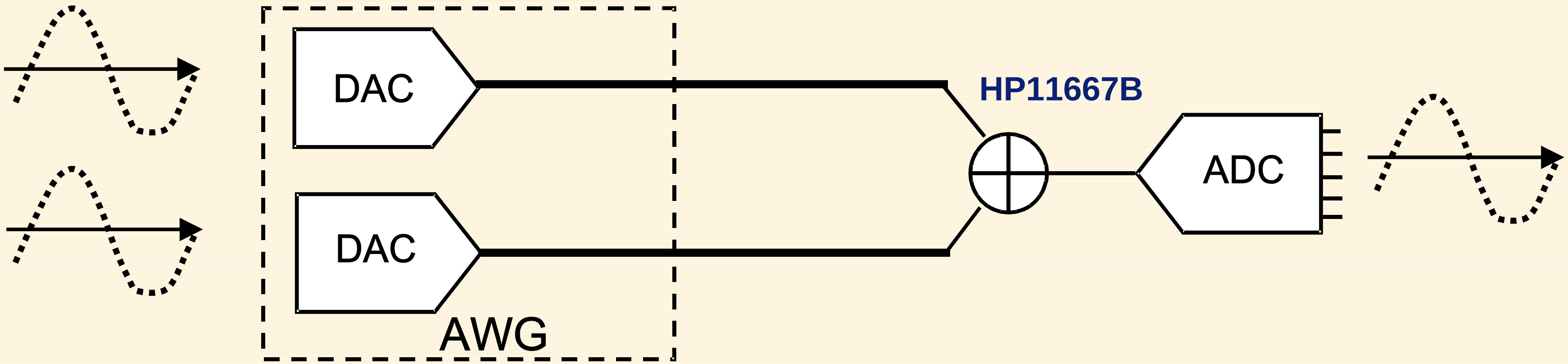
Harmonic number	*Reference values (dB)*	*Method results (dB)*	*Measurement difference (dB)*
2	-69.2	-68.1	-1.1
3	-67.9	-67.8	0.1
4	-72.5	-70.8	-1.7
5	-70.8	-71.8	1.0
6	-95.7	-86.2	-9.5
7	-78.2	-79.4	1.2
8	-102.9	-97.6	-5.2
9	-78.7	-78.9	0.2
10	-92.0	-86.7	-5.3

Loop-back technique



[ref]

Experimental Setup

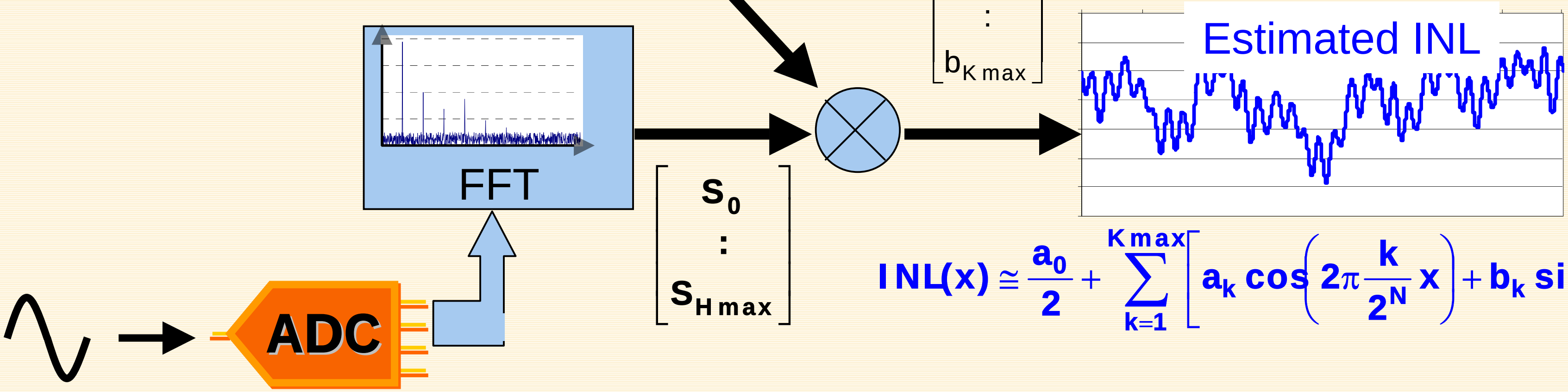


AWG: DACs emulation

Splitter/Combiner (resistive splitter)

INL from FFT

$$T_{K\,max}^{-1} = \begin{bmatrix} \beta_{1,1} & \cdots & \beta_{1,2K\,max} \\ \vdots & & \vdots \\ \beta_{H\,max,1} & \cdots & \beta_{H\,max,2K\,max} \end{bmatrix}$$



$$\begin{bmatrix} S_0 \\ \vdots \\ S_{H\,max} \end{bmatrix}$$

$$\begin{bmatrix} a_0 \\ a_1 \\ \vdots \\ a_{K\,max} \\ b1 \\ \vdots \\ b_{K\,max} \end{bmatrix}$$

$$INL(x) \cong \frac{a_0}{2} + \sum_{k=1}^{K\,max} \left[a_k \cos\left(2\pi \frac{k}{2^N} x\right) + b_k \sin\left(2\pi \frac{k}{2^N} x\right) \right]$$