Institute for System Testing
ISyTest

Fully-Efficient ADC Test Technique for ATE with Low Resolution Arbitrary Waveform Generator

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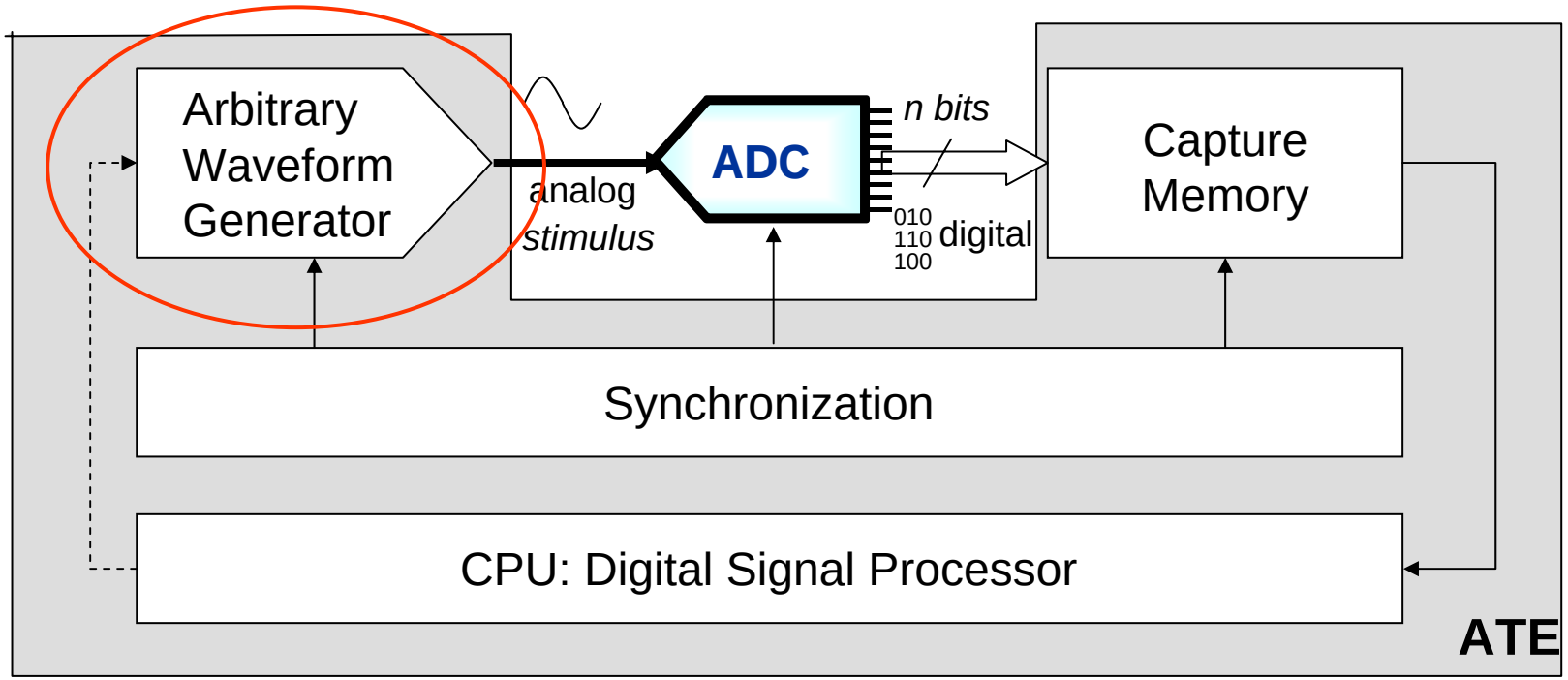
Context



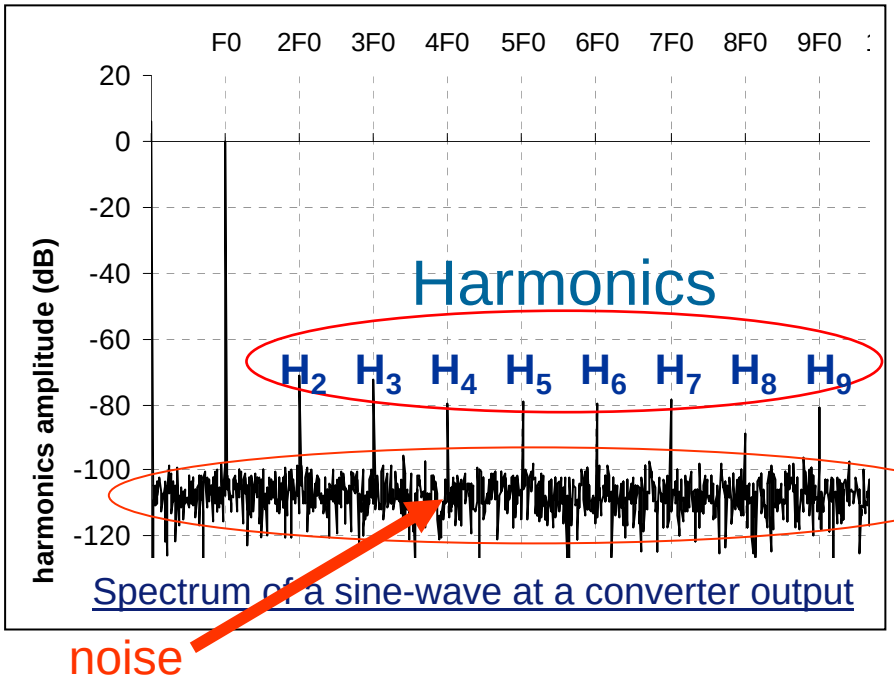
- Better performances than the DUT
  - ✓ Speed
  - ✓ Resolution
  - ✓ Distortion
  - ✓ ...

Outline

- Introduction
- Test Method
- Learning Phase
- Mass Production Test
- Results
- Conclusion

Introduction

Converter Parameters



- Dynamic Parameters
  - ✓ THD
  - ✓ SFDR

  Directly defined by Harmonics
  - ✓ SINAD
  - ✓ ENOB

  Directly defined by Harmonics and noise*
- Static Parameters
  - ✓ INL

  Direct correlation from Harmonics**

Harmonics + Noise ⇒ Converter Parameters

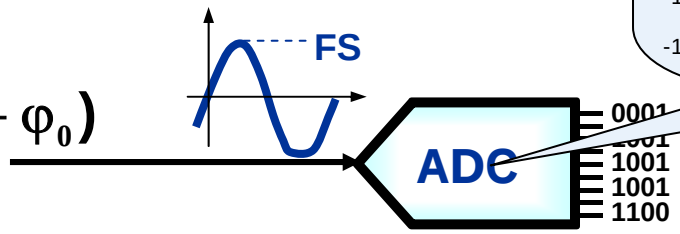
* "Improving the dynamic measurements of ADCs using the 2-ADC method", Philippe Cauvet, Journal of Computer standard and interfaces, 2001, vol.22 issue 4, pp281-286

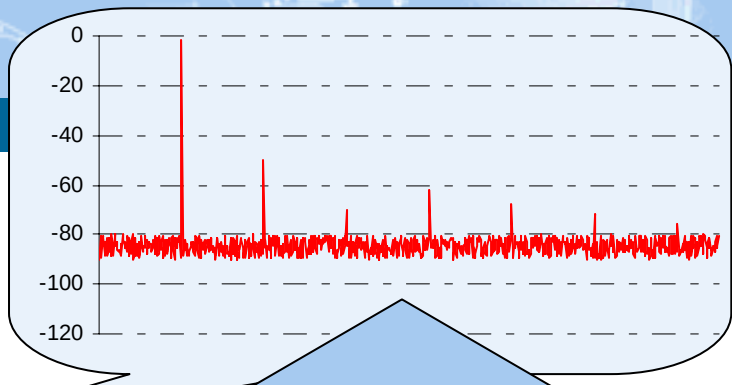
** "Comparison Between Spectral-Based Methods for INL Estimation and Feasibility of Their Implantation", V. Kerzerho, S. Bernard, J.M. Janik, P. Cauvet, Proc. IEEE International Mixed-Signal Testing Workshop, pp. 270-275, 2005.

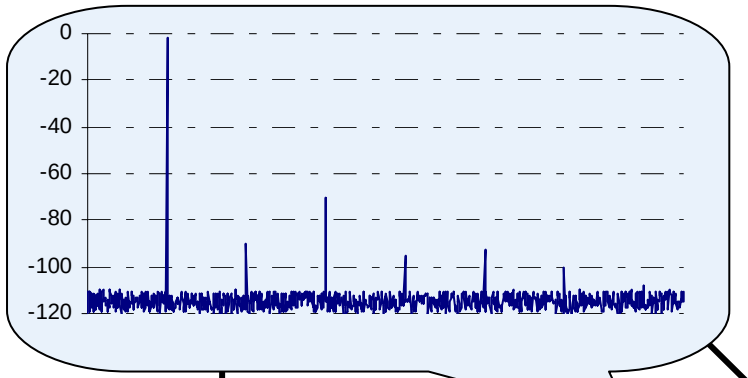
Introduction

ADC Testing

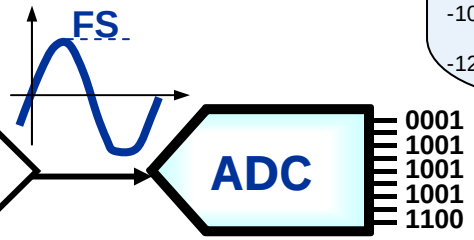
$$x(t) = FS.\cos(2\pi.f_{in}.t + \varphi_0)$$

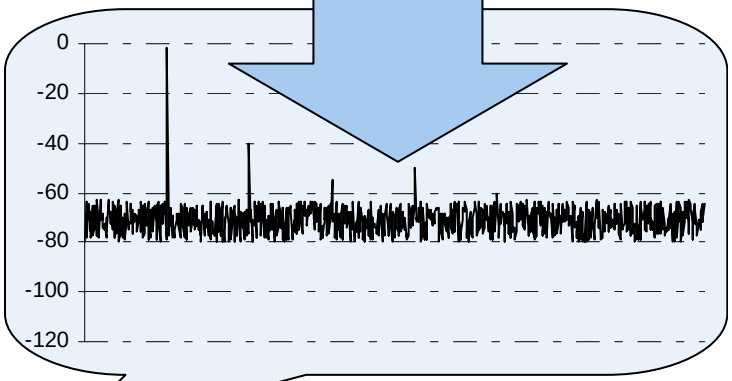






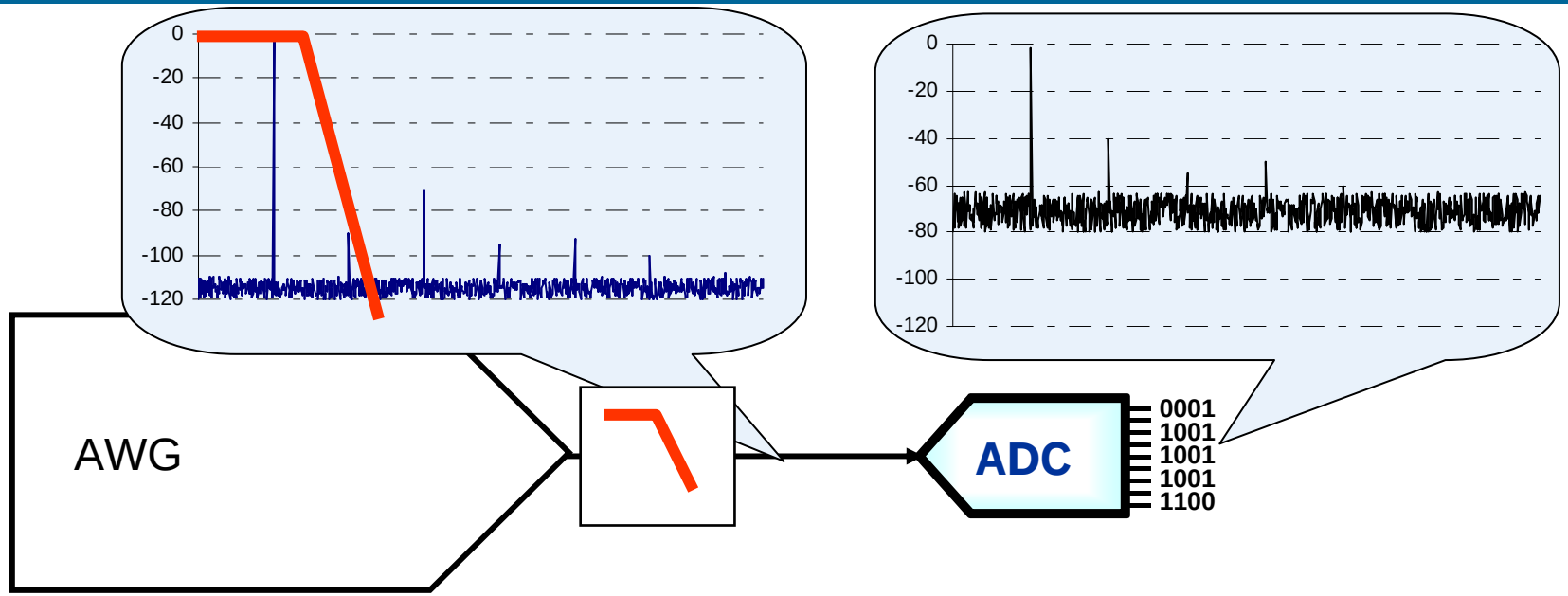
Arbitrary Waweform Generator





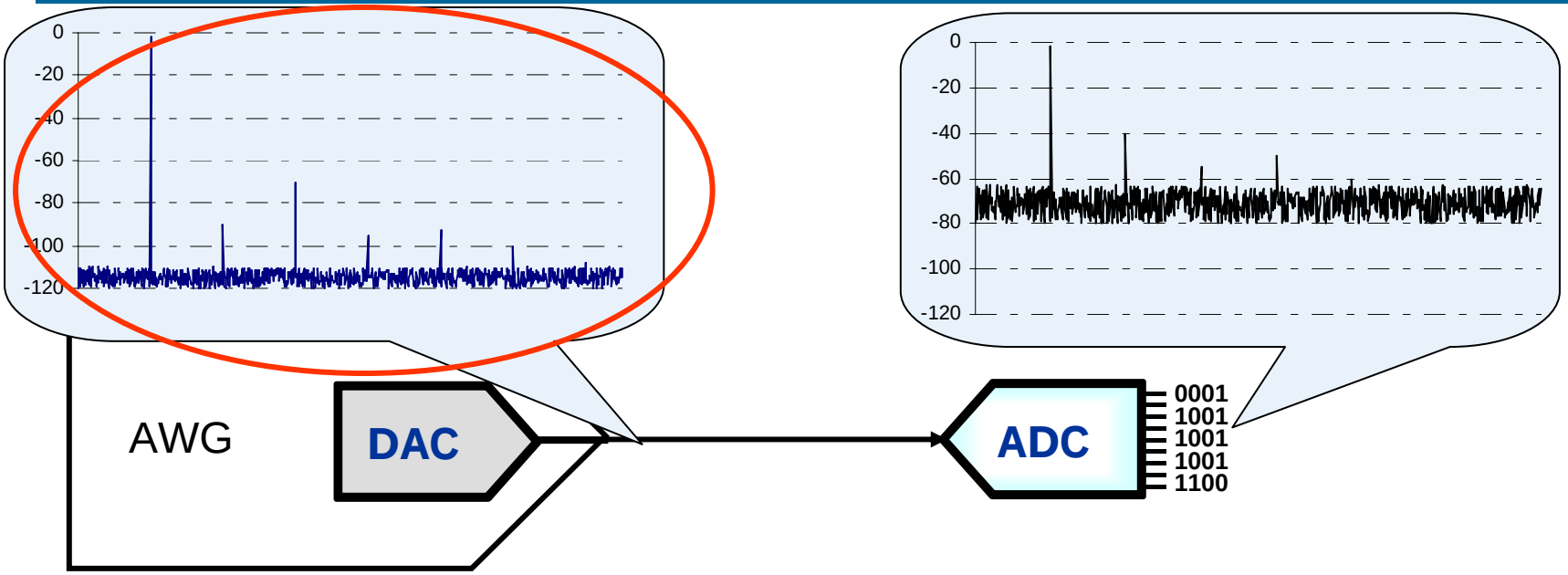
Measurement

Introduction



- **Selective Filter**
  - ✓ One filter per test frequency
  - ✓ No noise reduction in the band
- **Wobbling, dithering** [Janssen and al. 99]
  - ✓ Need several test procedures
  - ✓ Number of samples and complex post-processing
- **Stimulus Error Identification and Removal (SEIR)** [Jin and al. 07]
  - ✓ For static parameters and static test

Introduction



$$\underline{\mathrm{Hmeas}_k} = \underline{\mathrm{Hdac}_k^{FS}} + \underline{\mathrm{Hadc}_k^{FS}}$$

$$\Rightarrow \begin{cases} \mathrm{Re}(\underline{\mathrm{Hmeas}_k}) = \mathrm{Re}(\underline{\mathrm{Hdac}_k^{FS}}) + \mathrm{Re}(\underline{\mathrm{Hadc}_k^{FS}}) \\ \mathrm{Im}(\underline{\mathrm{Hmeas}_k}) = \mathrm{Im}(\underline{\mathrm{Hdac}_k^{FS}}) + \mathrm{Im}(\underline{\mathrm{Hadc}_k^{FS}}) \end{cases}$$

Two equations but Four unknowns $\forall k \geq 2$

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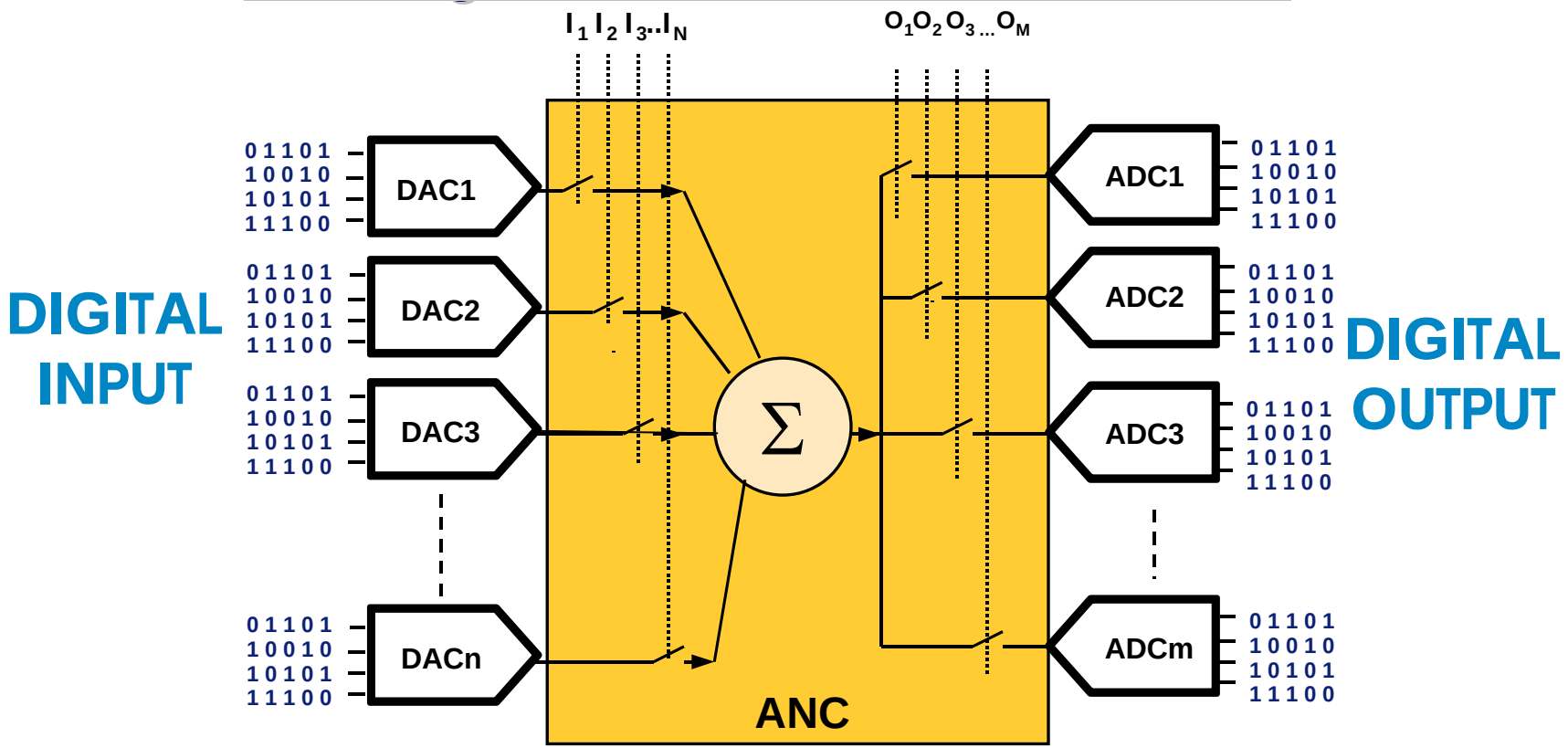
Analog Network of Converters *

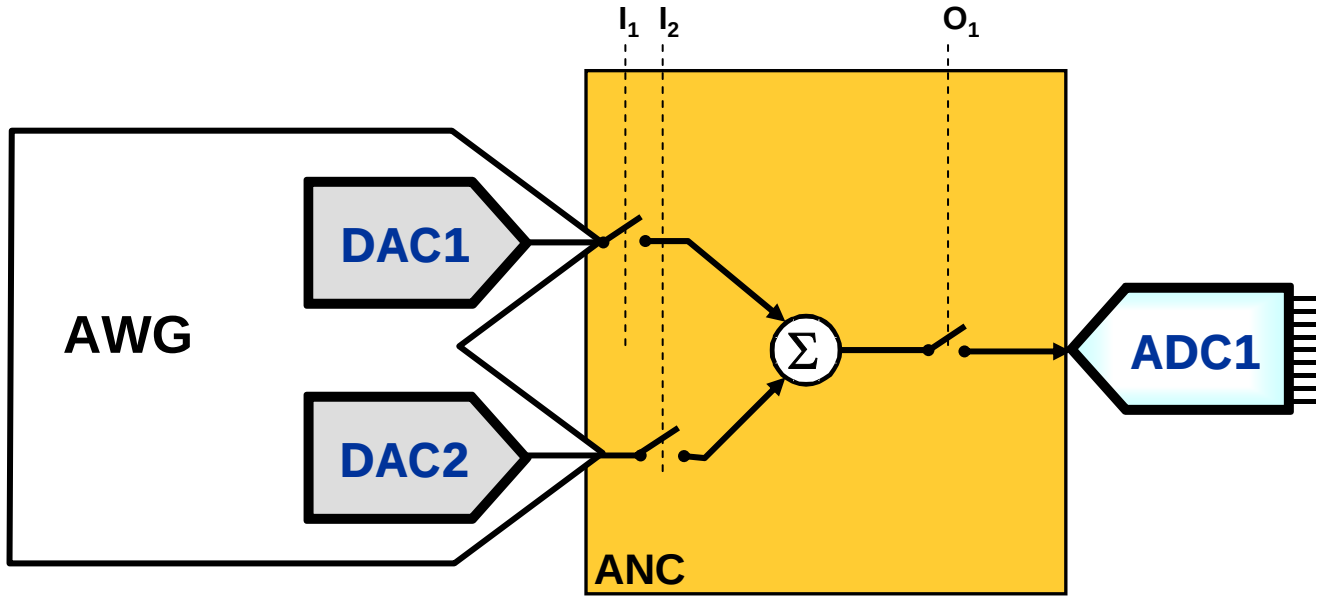


Multi-configuration → Test of every converter

* ETS'06: V. Kerzérho, P. Cauvet, S. Bernard, F. Azaïs, M. Comte and M. Renovell "Analogue Network of Converters": a DFT Technique to Test a Complete Set of ADCs and DACs Embedded in a Complex SiP or SOC

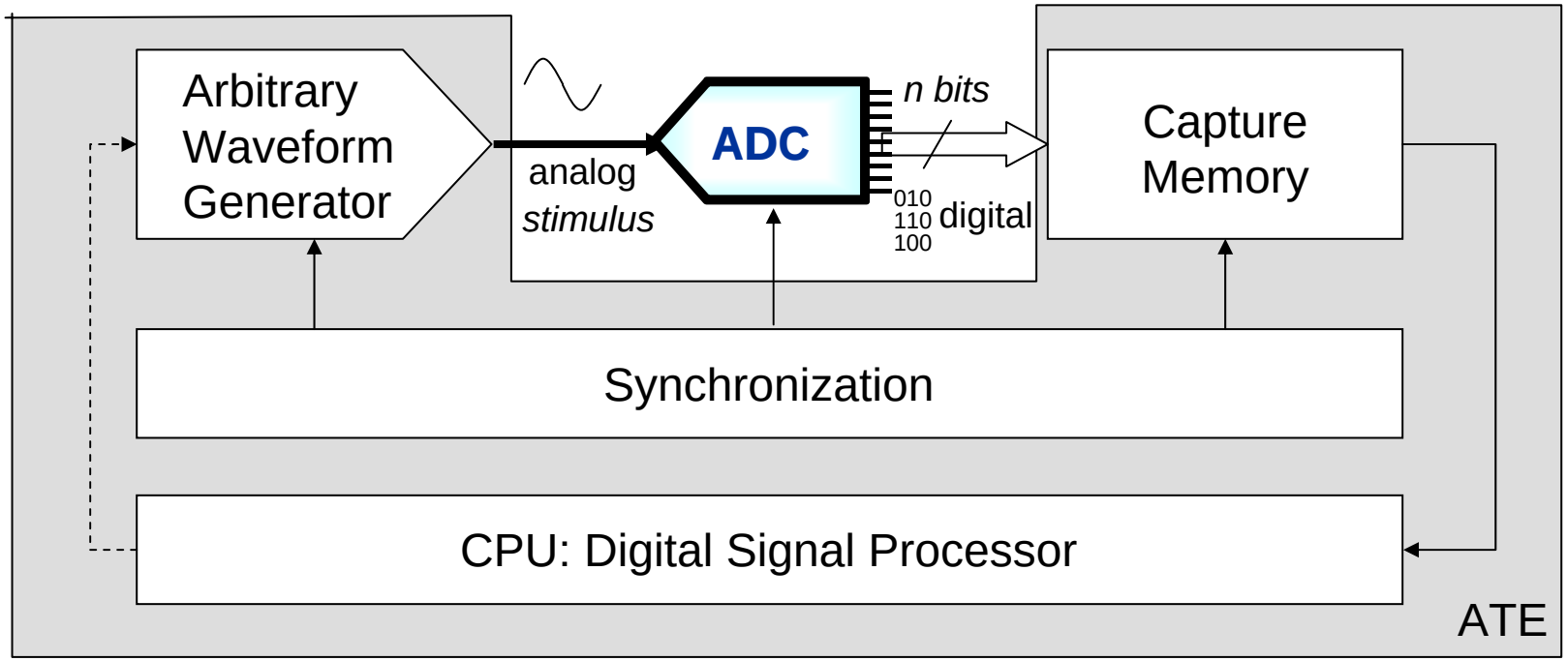
Test Method

Hardware Set-up



- Concerning the method
  - ✓ Nonlinear phase shift
- Concerning the hardware requirements
  - ✓ We need two AWG Channels

Test Method



- Learning Phase
  - ✓ Estimate Harmonics created by the AWG
- Mass Production Testing
  - ✓ Test ADC in removing AWG error by post-processing

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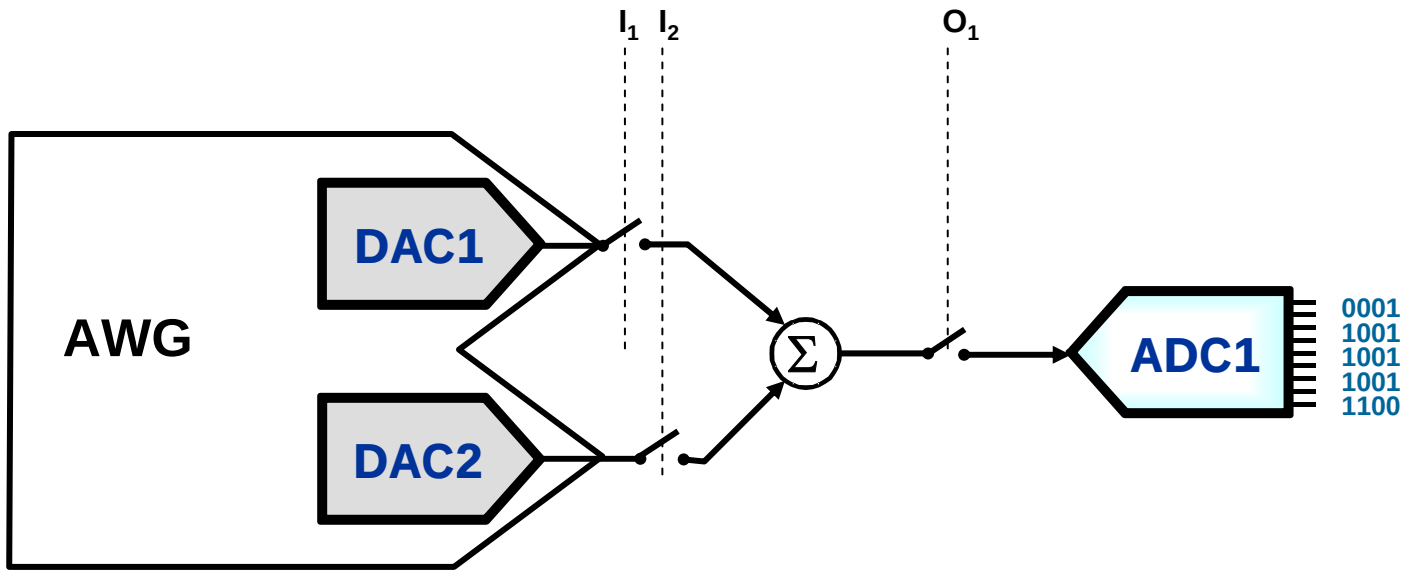
Learning Phase

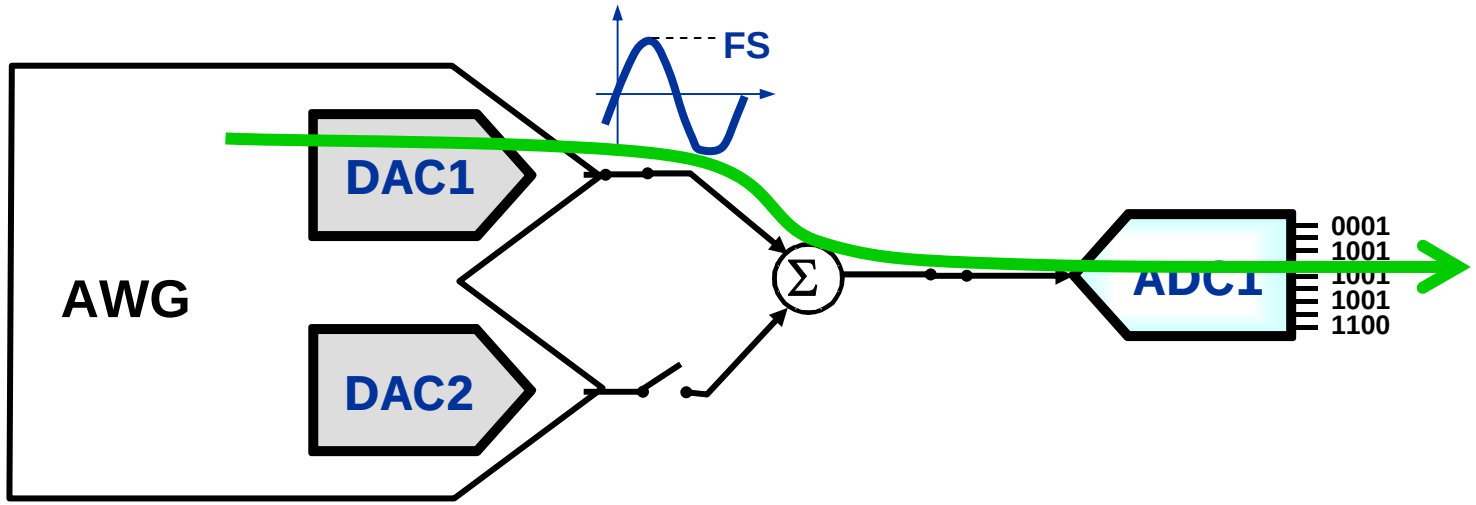
Context



Three sets of parameters to be evaluated: $\mathbf{Hdac1_k^{FS}}$, $\mathbf{Hdac2_k^{FS}}$, $\mathbf{Hadc1_k^{FS}}$

Learning Phase

Configuration C(1,1): the First two equations

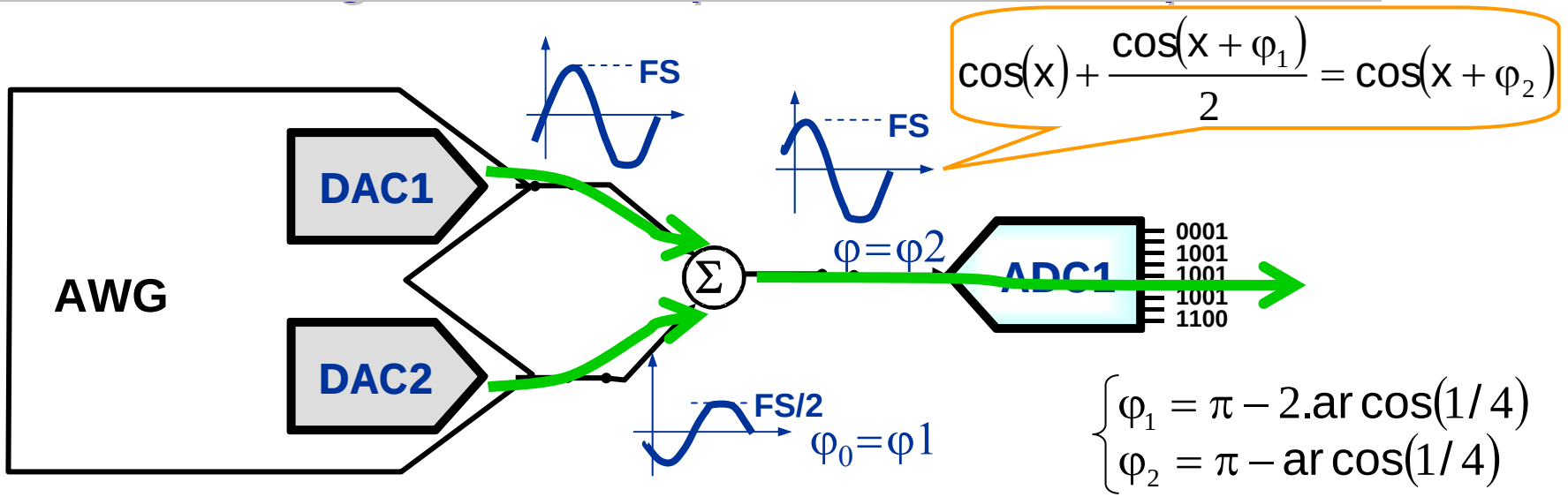


$$Hmeas1_k = Hdac1_k^{FS} + Hadc1_k^{FS}$$

$$\Rightarrow \begin{cases} Re(Hmeas1_k) = Re(Hdac1_k^{FS}) + Re(Hadc1_k^{FS}) \\ Im(Hmeas1_k) = Im(Hdac1_k^{FS}) + Im(Hadc1_k^{FS}) \end{cases}$$

Learning Phase

New Configuration & phase and amplitude

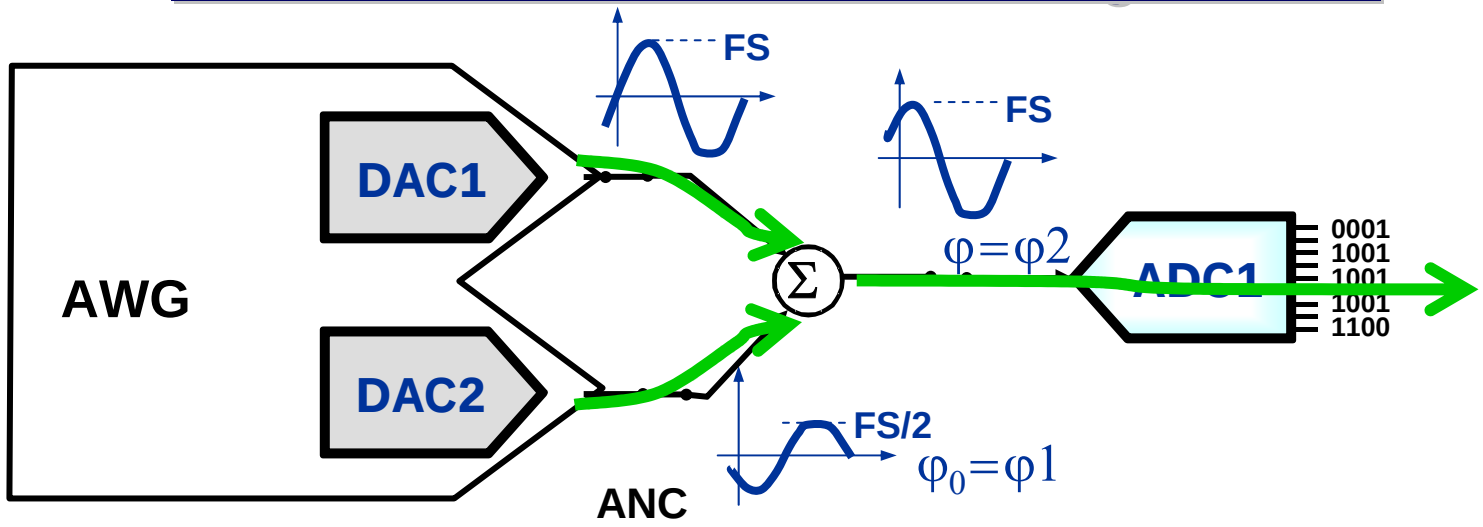


$$Hmeas5_k = Hdac1_k^{FS} + Hdac2_k^{FS/2}.e^{-jk\varphi_1} + Hadc1_k^{FS}.e^{-jk\varphi_2}$$

Two more linear equations

Learning Phase

Conclusion of the Learning Phase



- Test configuration (AWG1/ADC AWG2/ADC AWG1&2/ADC)
- Relative phase shift variation
- Different amplitudes of the test signal (FS, FS/2)

5 Tests → Linear System → Estimation of AWG harmonics

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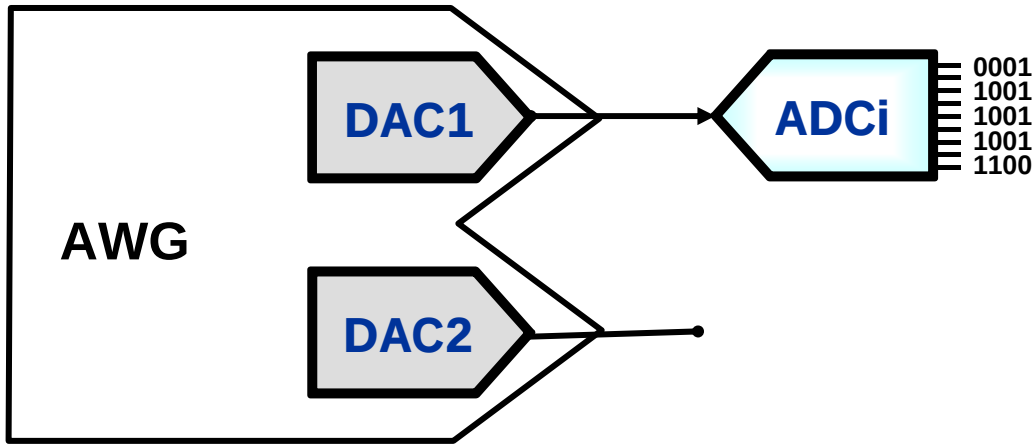
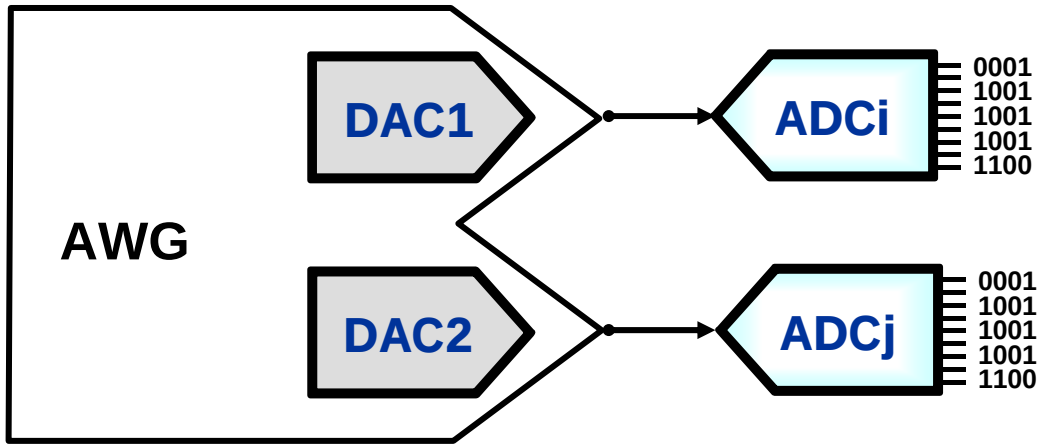
ADC Testing



$$\underline{Hmeasi_k} = \underline{Hdac1_k^{FS}} + \underline{Hadci_k^{FS}}$$

Post-Processing calibration ➡ 1 Test procedure per ADC

Parallel Testing



$$Hmeasi_k = Hdac1_k^{FS} + Hadci_k^{FS}$$

$$Hmeasj_k = Hdac2_k^{FS} + Hadcj_k^{FS}$$

Post-Processing calibration ➡ 1 Test procedure per 2ADC

Summary

- Learning Phase
  - ✓ Two channels of LOW PERFORMANCE AWG
  - ✓ One ADC under test (no gold device)
  - ✓ 5 measurements for the estimation of AWG features
- Production test
  - ✓ One test per ADC under test
  - ✓ Parallel testing is available with the two AWG channels

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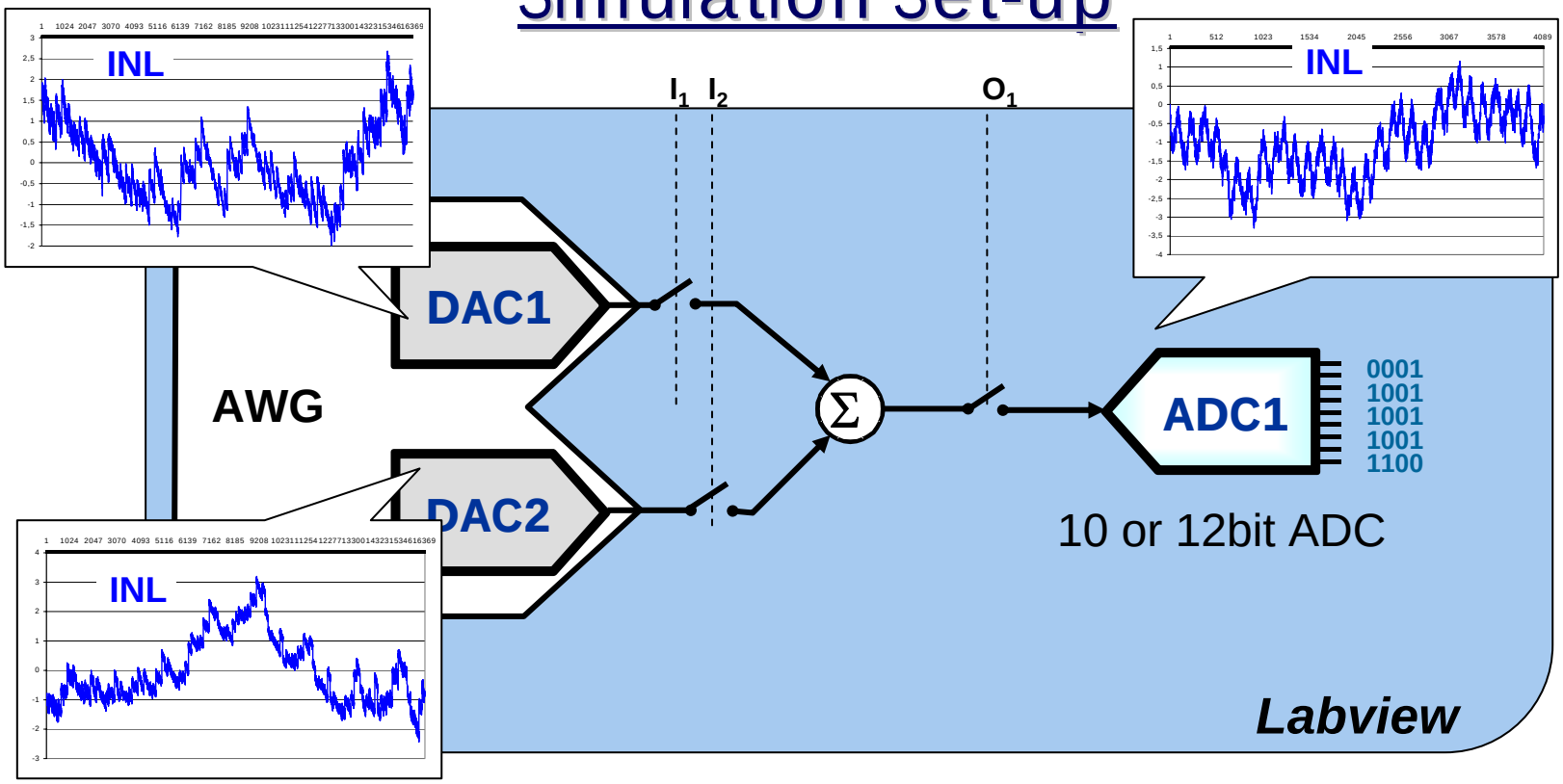
Results: Simulations

Simulation Set-up

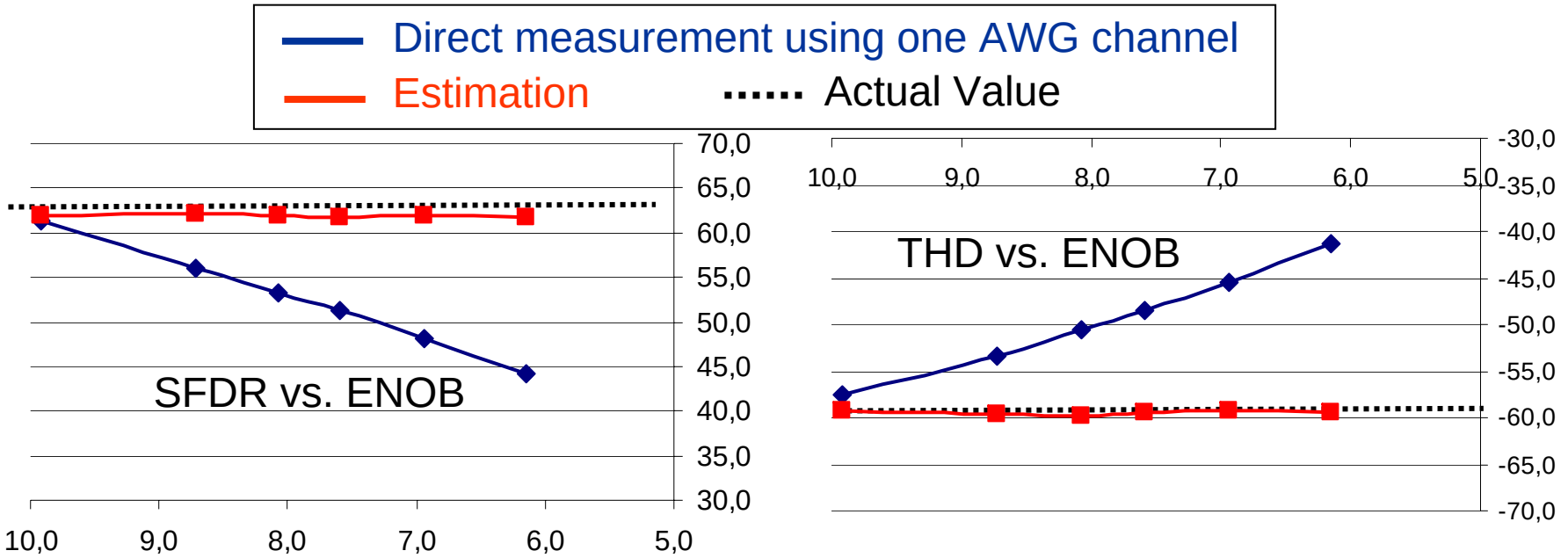


- Realistic Models of Converters
  - ✓ INL from measurement on real converter
  - ✓ Jitter
  - ✓ White noise

ENOB variation

Results: Simulations

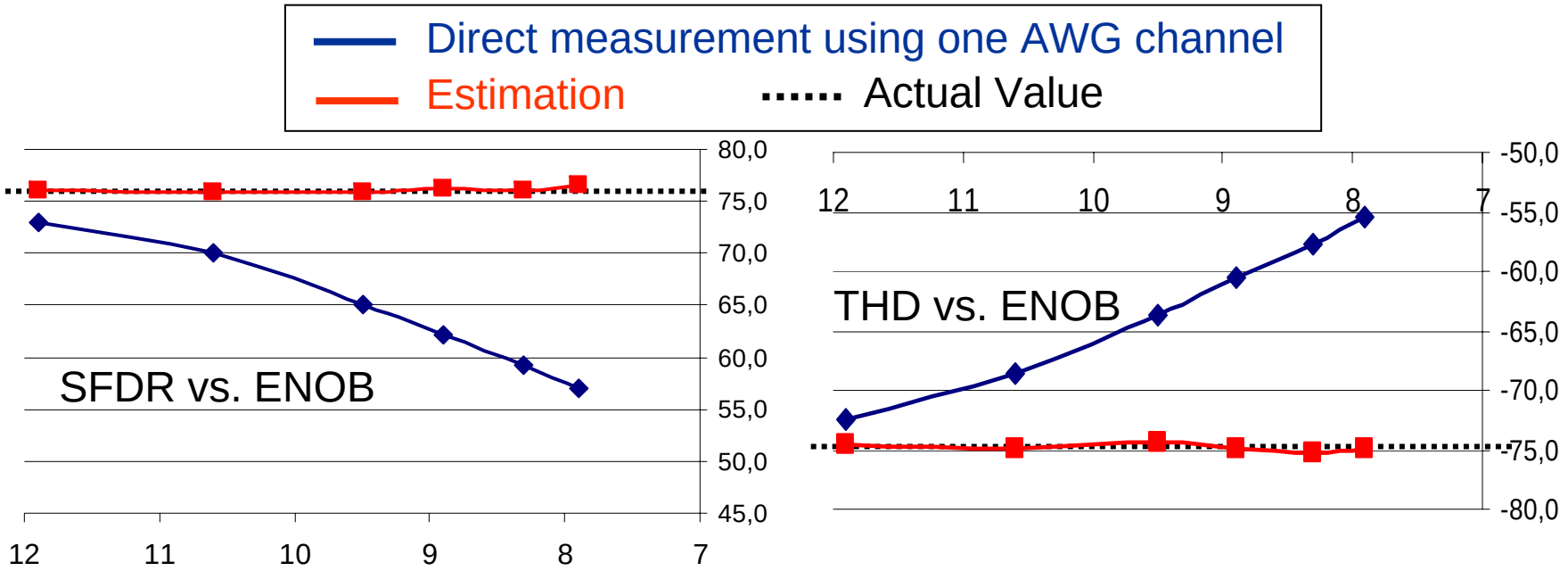
Simulation Results for a 10bit ADC



Harmonic Estimation of 10bit ADC with 6bit (ENOB) AWG

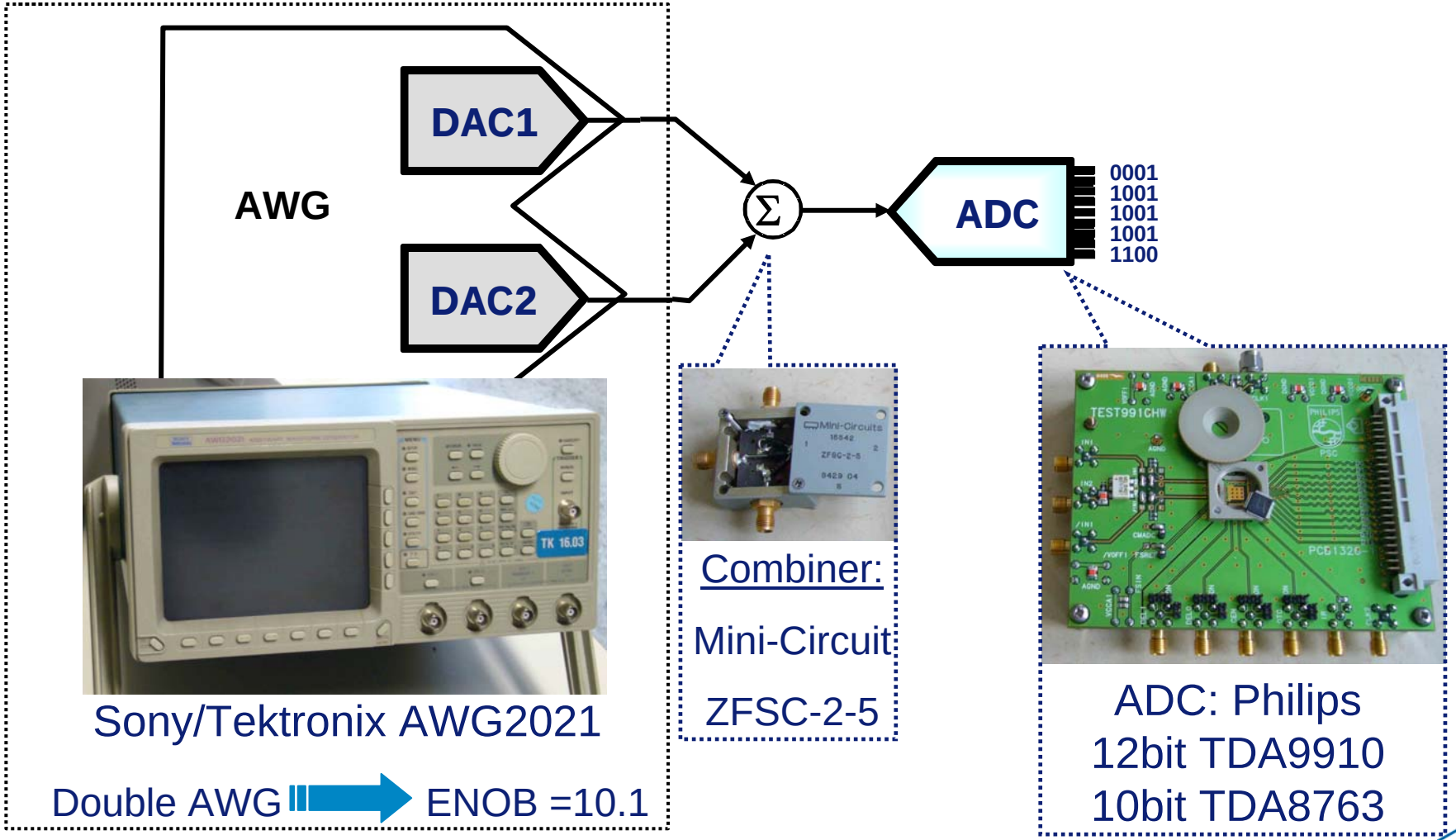
Results: Simulations

Simulation Results for a 12bit ADC



Harmonic Estimation of 12bit ADC with 8bit (ENOB) AWG

Results: Hardware Experiments



Results: Hardware Experiments

Experimental Results (real circuits)

10-bit ADC: TDA8763

ADC	Expected THD (dB)	Estimated THD (dB)	Estimat. Error (dB)	Expected SFDR (dB)	Estimated SFDR (dB)	Estima. Error (dB)
#1	- 66.6	- 67.3	0.7	68.7	67.9	0.8
#2	- 68.1	- 66.7	-1.4	70.1	70.0	0.1
#3	- 62.6	- 62.4	0.2	67.0	66.7	0.3
#4	- 60.5	- 60.6	0.1	63.3	62.1	1.2

Results: Hardware Experiments

Experimental Results (real circuits)

12-bit ADC: TDA9910

ADC	Expected THD (dB)	Estimated THD (dB)	Estimat. Error (dB)	Expected SFDR (dB)	Estimated SFDR (dB)	Estima. Error (dB)
#1	- 66.4	- 66.0	- 0.4	66.9	66.9	0.0
#2	- 64.8	- 65.9	1.1	67.2	65.6	1.6
#3	- 63.2	- 63.6	0.4	67.8	65.3	2.5
#4	- 70.4	- 69.4	- 1.0	70.7	72.1	-1.4

Conclusion

ADC Test with LOW PERFORMANCE AWG

- Learning Phase
  - ✓ We need two AWG channels
  - ✓ 5 test procedures for the estimation of the AWG harmonics
- Production test
  - ✓ 1 test procedure per ADC under test
  - ✓ Parallel testing is available with the two AWG channels
- Validation
  - ✓ Simulation: AWG with 4bits less than the ADC under test
  - ✓ Hardware experiments: validation on 10 and 12bit ADCs

Conclusion

ADC Test with LOW PERFORMANCE AWG

- Learning Phase
- Production test
- Validation
  - ✓ Simulation: AWG with 4bits less than the ADC under test
  - ✓ Hardware experiments: validation on 10 and 12bit ADCs

Future Works

- Extended validations
- INL extraction from the harmonic estimation
- Noise measurement

Thank You
for your Attention