2A702: NanoTEST

Test Technology for Nano CMOS Processes

Goal

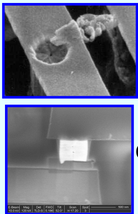
- NanoTEST will create breakthroughs in manufacturing test
  - **Low cost**, **better quality** and **short time-to-market**
- Development of flows, tools and standards
- Commercial success of European microelectronics industry

Approach

WP 1: Technology

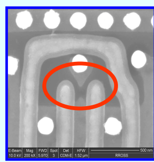
New defects will appear in **new process nodes** that drive the need for **new test methods**.

Old process | New process



Bridge

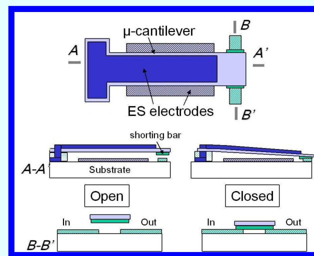
Open



Optical Proximity Correction (OPC)

WP 2: Design-for-Test (DfT)

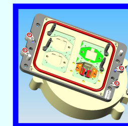
DfT offers powerful techniques to reduce **test cost** and **test complexity**



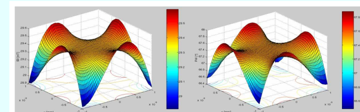
RF MEMS Switch

WP 3: Tester

Develop new methods to enhance **tester throughput** and reduce **tester resources**



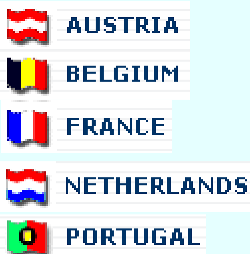
GMR Sensor Hardware | Hexapole



Field magnitude & direction

Cooperation (11 Partners)

5 Countries



Large firms | Institutes | Small firms

Manpower: 404.5
Duration: 2005-2008

NXP Semiconductors
Research – Design Methods & Solutions
High Tech Campus 48 (WA p1.60)
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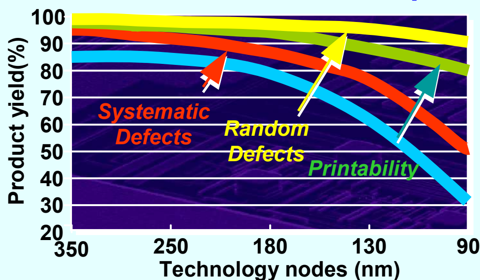
WP 1: Technology Perspective - Challenges

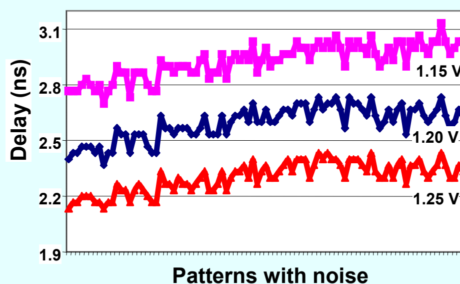
- Testing and detection of new defect types in 65nm/45nm technology nodes
- Influence of process variation is increasing
- Finding adequate fault models
- Improving diagnosis method to increase resolution both inter- and intra-gate
- Faster yield ramp-up support by means of test data analysis
- New methods for testing of embedded SRAM and non-volatile memories

Defect-based Test & Diagnosis Strategies

Defect-based test techniques



Shift in dominating yield loss mechanisms

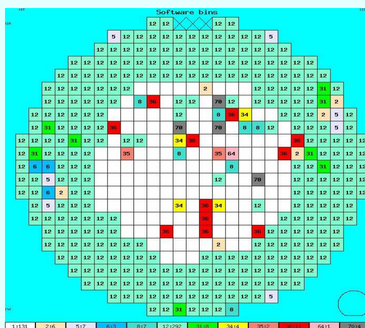


- Advanced delay fault testing
- IR drop/noise impacts on performance (>15%)
- Current measurements of AMS blocks
- Defect based test methods for MS blocks

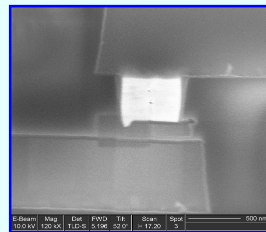
Electrical fault diagnosis

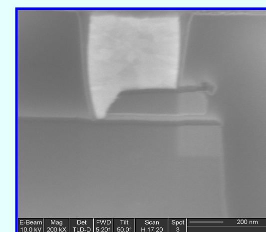
Open via : scan chain fail
Timing marginalities (hold problems)

Resistive via : logic fail
Interconnect problems



Volume diagnostics
Statistical analysis
Linked to YMS/DDB

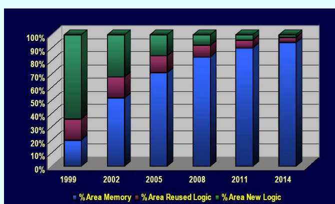


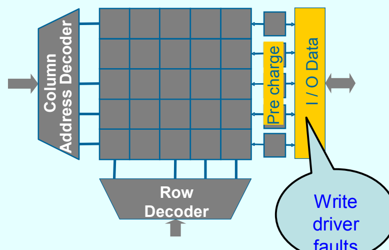


Centre-border effect

- Intra-gate bridge/open diagnosis method
- Volume diagnosis for yield improvement (30% → 90% in 3 weeks
- Multiple fault diagnosis (SA, Delay, Bridge, Intra-gate)

Memory test





C90-Dual Port SRAM: New test algorithms

C65-Single Port SRAM: Address gap Leads to low FC

- New test algorithms for Dual/Single port SRAMs and FIFO
- New fault models
- Appropriate stress conditions (V,T,Temp)

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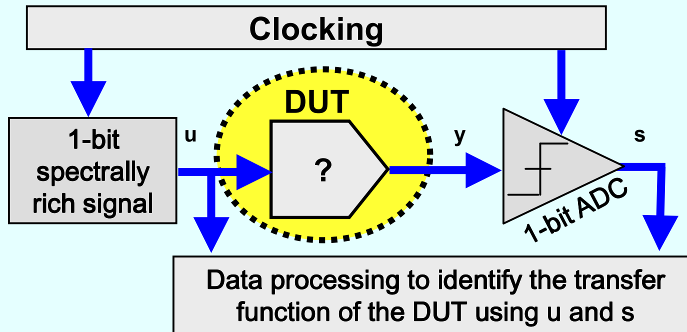
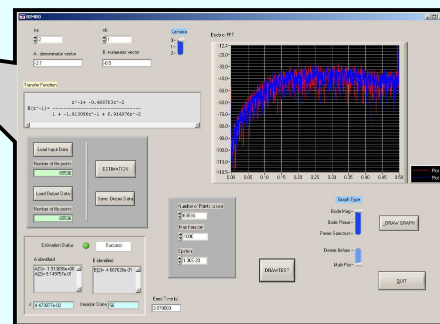
WP2: A Basic Identification Method using Binary Observations

Practical implementation



Principle

- Generate a spectrally rich signal *u* (white noise).
- Measure DUT's output *y*, using a 1-bit ADC.
- Compute the estimated time response *y* and *s* using a parametric model of the DUT
- Adjust the parametric model of the DUT so that a correct estimation of *y* and *s* is produced



Software tools

For further information contact: CEA-LETI
Email: *eric.colinet@cea.fr*

Benefits

- Use a simple 1 bit ADC (triggered comparator)
- Open loop excitation
- Measures can be done very closed to the DUT
  =>low measurement noise

Future plan

Implementation of this methodology including the identification algorithm into silicon

WP2: AT-speed BIST for Data Converters

In cooperation with

Challenges:

DfT for test cost and complexity reduction

Principle

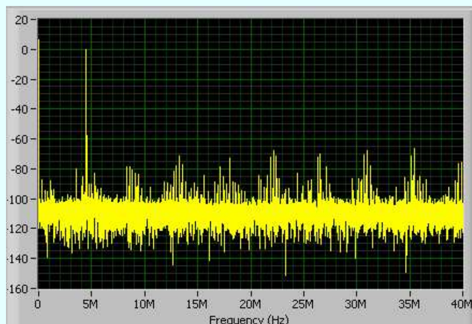
BIST & BISR with:

-Back end digital processing and INL embedded compensation

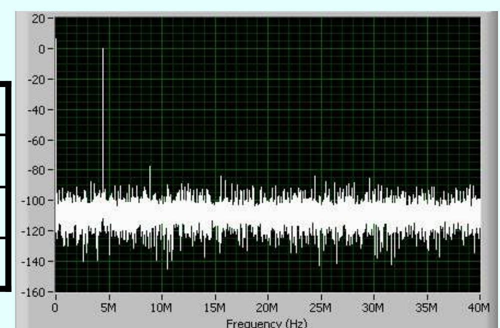
-Reduce set of samples for estimating compensation (2k vs. 200k for Histogram method)

Benefits

Improve the converter performances



	Before	After
SFDR	66.44	81.04
THD	-64.83	-79.40
ENOB	9.37	10.69



Acronyms

BIST : Built-in Self Test
BISR : Built-in Self Repair
INL : Integral Non Linearities
SFDR : Spurious Free Dynamic Range
THD : Total Harmonic Distortion
ENOB : Effective Number of Bits

Future plan

Optimize back end processing method

Demo-2

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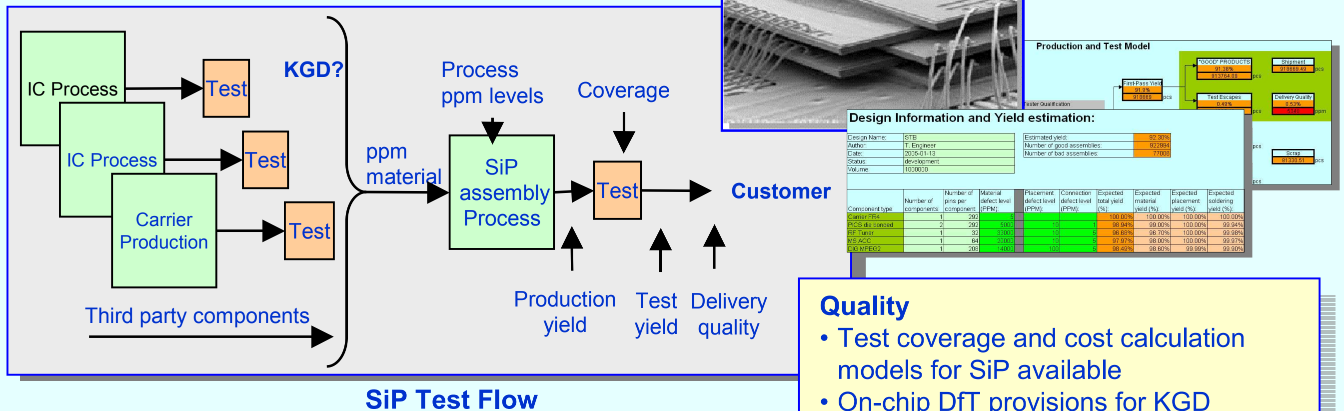
WP 3: Tester Perspective - Challenges

- Increased circuit complexity, test data volume, and signal speed.
- System-in-Package (SiP) testing based on a known-good-die approach (KGD)
- Advanced test automation tools for SoC and SiP.
- Cutting production test cost by one order of magnitude
- Enhanced test cell throughput by multi-site testing for digital, analogue, RF, sensors.
- Low-cost test cells considering integral costs of testers, handlers, probers, and silicon

Test Strategies / Test Automation / Test Cells

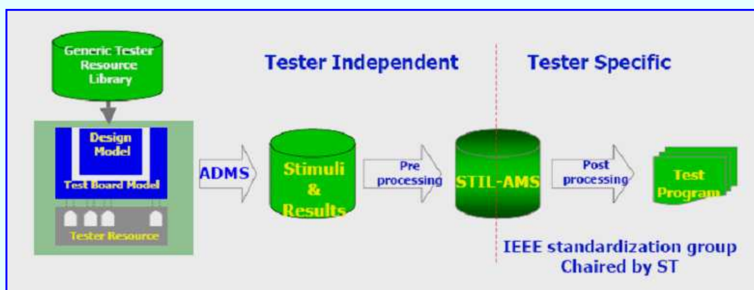
Test Strategies for SiP



SiP Test Flow

Quality
- Test coverage and cost calculation models for SiP available
- On-chip DfT provisions for KGD (e.g. LVDS BIST, using ADC/DAC as instruments)

Test Automation Tools



AMS Test Development Flow

Time-to-Market
- AMS Test development flow saves up to 50% of engineering efforts
- Test-Simulated tests up and running within 1- 2 days rather than week(s)

Low-cost Test Cells

GMR Sensor Test Hardware

Structural DfT Tester

Test Cost:
- 4x parallel test of integrated GMR sensor products is industry benchmark
- Low-cost Structural DfT tester is in 10k€ range rather than 1M€
- Structural test program for DAC cuts test time by factor 15

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