Low Power SRAM Design for Mobile Phones Products

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Outline

• Introduction – Mobile Phone chip market
• Technology status
  – CMOS technology roadmap
  – Process/Bit Cell choice
• SRAM Low Power design
  – Challenges
  – Power Modes
  – SRAM Bit Cell challenges
  – SRAM Bit Cell Assists
  – Dual-Rail approach
• Conclusion
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Introduction

Mobile Phone chip market:

• A few numbers (Gartner’s 2011 forecast):
  – Semiconductor market: $314 billion (+4.6%)
  – Mobile market: $55.4 billion (+13.6%)

• Main types of chip for mobile phones
  – ABB: Analogue Baseband
  – DBB: Digital Baseband
  – Cellular RF transceiver
  – PMU
  – APP: Application Processor
  – Communications: BT, FMR, WIFI, GNSS (satellite navigation), ...

• Main mobile chipmakers companies
  – Qualcomm, Broadcom, TI, IMC, STE, MediaTek, Nvidia, Xilinx, Marvell, ...

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Introduction

Mobile Phone chip market:
Each mobile phone chipmaker propose different SoC solutions with different granularity.
SoC is often a good solution towards cost and power reductions

- Example of high integration in low segment (entry phone):
  Intel® X-GOLD™ 110:
  65nm SoC includes GSM/GPRS Baseband, RF transceiver, Mixed Signal, Power Management, SRAM and RDS FM Radio in a Single-Chip

- Example of high integration in high segment (smart phone):
  Qualcomm Snapdragon S4 SoC announced for next year
  28nm Soc Modem 3G/LTE + Multi-Core APP + Multi-Media
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CMOS technology roadmap

- Scaling is given by gate pitch
- Conditions for attractive power gain
  - Scale down VDD
  - Static power: try to keep leakage current constant
  - Dynamic power: Transistor/BE capacitances must scale as well
=> Technology challenges
Process/Bit Cell choice

Several process flavours are proposed at each technology node
=> Very broad panel of chips can be manufactured

Example of process foundry offering

In each family, several Vt flavors available for logic device (e.g. HVT, RVT, LVT)
Several 6T bit cell flavours are proposed in each process version.

Definition of $V_{\text{min}}$: functional minimum voltage without yield loss … in production.

Example of bit cell foundry offering.

SRAM $V_{\text{min}}$ critical towards DVS concept.
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SRAM design challenges

Low power SRAM still dominant in the mobile chips like DBB and AP IPs (DRAM and Flash memories still external)

😊 What R&D people like in SRAM?
- Fast access (cycle time in a range of 50 Mhz to 1 Ghz according to the application running in the phone)
- High density (e.g. 2 to 3 Mbits/mm2 in 40nm)
- Fast integration in a design
- No cost adder (or minor cost) at process level

😊 What R&D people do not like in SRAM?
- Area (can be more than 50% of chip area)
- Static power (>> DRAM)
- One of the main yield detractor
  - Hard fails (always failing)
  - But also Soft Fails (sometimes failing, depending of process, voltage, temp.)
- Test time and Test escape rate (bit cells not caught in production test)
- Narrow voltage window \([V_{min}, V_{max}]\) -> impact on voltage scaling
What is an SRAM macro?

- Array size: from a few Kbits to 1Mbits
- In general compiler based (automated generation)
- Column multiplexor option to extend the number of word, e.g.

A macro of 256Kb with 512 Wordlines:
- in mux 4b: 2k word x 128 bit
- in mux 8b: 4k word x 64 bit
- in mux 16b: 8k word x 32 bit

### Single-Port SRAM floorplan

<table>
<thead>
<tr>
<th>Array</th>
<th>Row Decoders</th>
<th>WL row</th>
<th>BL column</th>
</tr>
</thead>
<tbody>
<tr>
<td>Column mux</td>
<td>Address Pre-decoder, Control, Timing generator</td>
<td>Column mux</td>
<td></td>
</tr>
<tr>
<td>R/W circuit + IO interface</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Column mux</td>
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<td></td>
<td></td>
</tr>
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<td>Row Decoders</td>
<td>Array</td>
<td></td>
</tr>
</tbody>
</table>

### 6T cell schematic

3 types of devices
- PU Pull-Up (Pfet)
- PD Pull Down (Nfet)
- PG Pass-Gate (Nfet)
Standard Low Power measures in SRAM

At bit cell level
• “low power” flavor (low leakage cell)

At periphery level
• Selection of the appropriate Vt flavor for logic device of the periphery (in some cases mixed-Vt are done)
• Maximum input signals gating to minimize the internal activity when memory is not accessed (e.g. Clock gating, Memory Enable gating, ...) -> impact on timings
• Bitline segmentation to reduce dynamic power and access time
  -> impact on area due to periphery overhead
• Power modes with additional control pins (driven by PMU)
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Power modes in SRAM

**Goal:** reduce/remove the static power
- with minimum penalty in area and speed

4 modes embedded within the SRAM macros:
- light sleep  no latency before operation
- sleep or retention
- deep sleep  latency before operation
- power off

Usual circuit solution: PFET VDD switch
Power modes in SRAM (cont’d)

- **light sleep**
  - VDD Rail
  - VDD
  - Array
  - Row Decoders
  - IO periphery/control
  - VDD

- **sleep**
  - VDD Rail
  - VDD
  - Array
  - Row Decoders
  - IO periphery/control
  - VDD

- **deep sleep**
  - VDD Rail
  - VDD
  - Array
  - Row Decoders
  - IO periphery/control
  - VDD

- **power off**
  - VDD Rail
  - VDD
  - Array
  - Row Decoders
  - IO periphery/control
  - VDD
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SRAM cell challenges

Main cell criteria

- cell Read current ⇒ performance, yield
- cell area ⇒ chip size ⇒ dies per wafer ⇒ chip costs
- cell leakage ⇒ chip power consumption
- Cell Vmin (and Vmax) ⇒ degree of voltage scaling ⇒ chip power
- manufacturability ⇒ yield
- cell Read margin (stability margin) ⇒ Stability during access (read/write), yield
- cell Write margin ⇒ yield, performance

Trade-off difficult: all criteria need to be carefully assessed
SRAM cell challenges

Biggest SRAM cell limitation is “Within die variation”

- **global variations:**
  ACLV, ACWV, tox, Vt
  - chip to chip
  - wafer to wafer
  - lot to lot

- **local variations:** statistical distribution of dopants

![Diagram](image)

Local mismatch becoming the major part at 90nm downwards
SRAM cell challenges

2 big aspects to take into consideration:

- SRAM has narrow devices (gate area very small)
  - $\sigma_{Vt_{SRAM}} >> \sigma_{Vt_{standard\ cell}} >> \sigma_{Vt_{analog\ cell}}$

- Each die has several Mbits of SRAM
  - About 6 sigma distribution must considered
    Mismatches, especially Vt mismatches, are exacerbated in SRAM bit cell
    - Severe impact on margins and then on Vmin
    - Create new type of fail: Soft Fail

Operating at low voltage needs new solutions to address these issues:

- **Bit cell Assist** circuits: to improve the cell margins
- **Dual Rail** concept: to keep the cell at the optimum voltage
SRAM cell challenges

Examples of margin degradations:

**Stability margin**

- Measured internal voltage levels on 0.57 μm² SRAM cell

**Write margin**

Outlyers: non functional cells !!
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SRAM Bit Cell Assist Principle

Goal: improve cell margins to get better yield and/or lower \( V_{min} \)

2 main families
- Read assist (or stability assist)
- Write assist

Principle: apply different biasing from standard (VDD/VSS voltage) to certain pin(s) of the bit cell to modify the strength of one type of device

It can be:
- WL wordline
- BL/BLB bitlines
- VDD & VSS source supplies
- VDD & VSS bulk supplies
SRAM Read Assists

The most usual technique: **lower the wordline voltage below VDD to weaken the PG**

Drawbacks:
- $I_{\text{read}}$ decreased (slower read)
- Write margin decreased

**Version 1**

**Version 2**
SRAM Write Assists

2 main techniques
• VDD collapse
• Negative Bitline boost

**VDD collapse**

VDD of selected columns is lowered

**Negative BL boost**

Diagram showing the voltage levels over time.
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Dual Rail concept

Goal: decouples logic VDD from SRAM bit cell constraints
⇒ Allows DVS concept
  ⇒ VDDM (bit cell array) always biased at high constant voltage
  ⇒ VDDL (logic) can be scaled according to performance needs
⇒ Second Voltage supply necessary (e.g. LDO)

Different versions of Dual Rail:
Advanced version expected to consume less power than basic version but periphery complexity is higher

„basic“ version

„advanced“ version

Array
Row Decoders
IO periphery/control
VDDM (memory)
VDDL (logic)

Array
Row Decoders
IO periphery/control

Only WL buffer @VDDM

Level shifters in IO part
## Dual Rail concept (cont’d)

Comparison between basic and advanced Dual Rail

<table>
<thead>
<tr>
<th>Criteria</th>
<th>Basic DR</th>
<th>Advanced DR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Impact on bit cell margin</td>
<td>No</td>
<td>Yes (stability)</td>
</tr>
<tr>
<td>Complexity increase in periphery</td>
<td>Min (LS)</td>
<td>Max (timer, signals interlocking, LS,...)</td>
</tr>
<tr>
<td>Power gain (at macro level)</td>
<td>None</td>
<td>Max</td>
</tr>
<tr>
<td>LDO current sizing</td>
<td>100% of $I_{mem}$</td>
<td>&lt;5% of $I_{mem}$</td>
</tr>
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Conclusion: what should we put within a Low Power SRAM in advanced nodes?

More and more features!…
Most likely all the features shown in this figure will be integrated together in advanced nodes, still with some significant gains!

Power Scaling still possible in new technology nodes
Thank you!