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FIRST CALL FOR PAPERS

VARI 2010

European Workshop on CMOS Variability

May 26-27, 2010, Montpellier, France

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VARI 2010 is the first European workshops on CMOS Variability. The Vari meeting answer to the need to have an European event on variability , where industry and academia meet to discuss. VARI 2010 is organized by *LIRMM.*

Montpellier has for centuries been a city where different cultures meet. Today, it is a dynamic economy in which art and science go hand in hand with advanced technology and the superb Mediterranean style-life. Part of the great European Medieval City tradition, open to the world, linked as much to the Mediterranean as to northern Europe, it is forever welcoming and assimilating new ideas, a melting pot of all that is best in today's civilisation. Montpellier is both a city dedicated to building a new Europe, and one of the southern Europe's main metropolies. There has been a university in Montpellier since the middle age. The medical faculty was founded in 1222, followed by humanities and law. The Montpellier science faculty was set up in 1808.
By plane: 10km from the Montpellier Méditerranée Airport with about 10 flights/day with Paris airports.
By car: about 2 hours from Nice Sophia/Antipolis, or Grenoble or Toulouse.

The VARI objective is to provide a forum to discuss and investigate the CMOS variability problems in methodologies and tools for the design of upcoming generations of integrated circuits and systems. The technical program will focus on timing, performance and power consumption as well as architectural aspects with particular emphasis on modelling, design, characterization, analysis and optimization of variability. The emphasis of the workshop is on, but not limited to, the following topics:

- **Variability modelisation and consideration in tools**
  - o Local variability : inductive stess, OPCs, …
  - o Uncertain phenomenom : doping
  - o Environmental variations (Vdd,T)
  - o Global process variations
- **Conception tools and methodologies for variability**
  - o Statistical approaches
  - o Multi-Corners approaches
  - o Tools for variability consideration at design and layout levels
  - o Layout post-treatment tools,
- **Measurements and sensors**
  - o Timing slacks and faults
  - o Process, Temperature, Vdd
  - o Power and Energy

- **Actuators**
  - o Vdd, VBB scaling (global & local)
  - o Frequence scaling
  - o Delay Tuning
- **Compensation at circuit Level**
  - o Asynchronous, desynchronised tehniques
  - o Operationg point tracking
  - o Clock tree resynchronisation
- **Compensation at layout Level**
  - o Regular layout
  - o Restrictive design rules
  - o OPC
  - o DFM
- **Compensation at architectural Level**
  - o Tasks remapping according to hardware possibilities
  - o Global or distributed, static or dynamic optimisation

Contributions are invited for regular presentations and discussion sessions. Perspective authors are invited to submit their complete paper, no later than February 1st, 2010, including a 100-word abstract and illustrations, in A4 camera-ready format, not exceeding 6 pages or 5000 words. Electronic submission is required and should follow the IEEE style for the final publication. Submitted papers will be reviewed formally and anonymously by several reviewers.

Selected papers will be included in special issues of Journals.

Proposals for panel sessions and special sessions are encouraged and must be received no later than February 1st, 2010.

More information can be found on the VARI 2010 website: http://www.lirmm.fr/vari10/