Comparison of Open and Resistive-Open Defect Test Conditions in SRAM Address Decoders *

Luigi Dilillo Patrick Girard Serge Pravossoudovitch Arnaud Virazel

Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier
Université de Montpellier II / CNRS
161, rue Ada – 34392 Montpellier Cedex 5, France

Email: <lastname>@lirmm.fr
URL: http://www.lirmm.fr/~w3mic

Simone Borri

Infineon Technologies France
2600, Route des Crêtes – 06560 Sophia-Antipolis, France

Email: simone.borri@infineon.com
URL: http://www.infineon.com

Abstract

This paper presents a comparative analysis of open (ADOF: Address Decoder Open Fault) and resistive open defects in address decoders of embedded-SRAMs. Such defects are the primary target of this study because they are notoriously hard-to-detect faults. In particular, we consider dynamic defects which may appear in the transistor parallel plane of address decoders. From this study, we show that test conditions required for ADOFs testing (sensitization and observation) can be partially used also for resistive open defect testing.

1. Introduction

The growing needs of performance, processing power, energy consumption and production cost has brought some new design concepts such as the Systems-on-Chip (SOC) revolution. With the SOC concept, many functionalities can be addressed by a single system instead of a complex and expensive system on board. In order to reach the various SOC challenges, the area employed for SRAM blocks is constantly growing. This is confirmed by the SIA Roadmap which forecasts a memory density nearby 80 % of the chip area in the next few years [1]. Thus, memory test solutions for new class of defects need to be developed.

Generally, memory test algorithms such as March tests [2, 3] are employed to determine the presence of defects in a memory. March algorithms are the most used because of their linear complexity. Test algorithms, like MATS++ and March C- [2, 4] are the most common March tests used in industry.

However, March tests are constructed essentially for static defects. In recent memory designs, a new class of defect appears to be more and more problematic from a test point of view. These defects are called dynamic defects. Referring to the classification presented in [5, 6], a fault is considered dynamic when the sequence of operations needed to sensitize it consists of more than one operation.

Among the known dynamic faults, we focus our study on open and resistive open defects which may occur in address decoders. Concerning open defects, we consider the faults which appear at transistor level and especially in the parallel plan of NAND/NOR gates. When such defects appear in an address decoder, two BLs (Bit Line) or WLs (Word Line) may be selected at the same time. This defect class, also called ADOF (Address Decoder Open Fault), has been considered in [7, 8], where it is proposed an algorithmic solution that allows the sensitization and

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observation of all ADOFs. Other works have dealt with this type of defect like [9, 10, 11]. They have proposed March test modifications to detect all the ADOFs. These methods will be briefly described in Section 3.

Recently, the ADOF problem has been considered from another point of view. In VDSM (Very Deep SubMicron) technologies, resistive open defects appear to be more and more common [12]. In the following, we will consider resistive open defects in the parallel plan of transistors, which we name resistive-ADOFs. The presence of a resistive-ADOF produces a delay in the selection and deselection phases of WLs or BLs. The fault effect may occur partially during a write or a read operation.

In this paper, we present a comparative analysis of ADOFs and resistive-ADOFs in address decoders of SRAMs. We show that the required test conditions for resistive-ADOFs in address decoders are almost the same than for ADOFs. The only difference concerns the timing requirements needed for observing defects, which are more stringent for resistive-ADOFs.

The rest of the paper is organized as follows. Section 2 gives details of a classical address decoder implementation. Section 3 presents the ADOF and resistive-ADOF test conditions. Section 4 provides a comparative study between both in terms of sensitization and observation conditions. Concluding remarks and future work are discussed in Section 5.

2. Basics and background

In the whole memory structure, we focus our attention on address decoders. Figure 1 depicts the scheme of a 2-bit WL pre-decoder. It is based on NOR-gates; NAND and NOT gates are present for synchronization and buffering respectively. A similar address decoder is used for BL selection. Such a structure is used in the Infineon 0.13µm synchronous embedded-SRAM architecture.

We consider open and resistive open defects in this address decoder. When one of these defects appears between gates (inter-gate defects), it can be detected by standard March tests. When the defect is located inside the gate (intra-gate defect) and especially in the parallel plan of transistors, it is called dynamic fault due to its sequential behavior. Referring to the NOR-gate of Figure 1, such a defect may be located in the drain, source or gate nodes of transistors TN1 or TN2.

As an example, in Figure 1 we have inserted an open defect in the source node of transistor TN2. This is an ADOF. In this architecture, the fault may produce an irregular behavior of the pull-down of the NOR-gate, thus preventing the correct deselection of the WL. In this case, two WLs can be selected at the same time, so two memory cells are addressed during the same read or write operation.

In presence of a resistive open defect, the NOR-gate pull-down presents a certain delay. In the following, we show that the effects produced by resistive-ADOFs are very close to ADOFs.

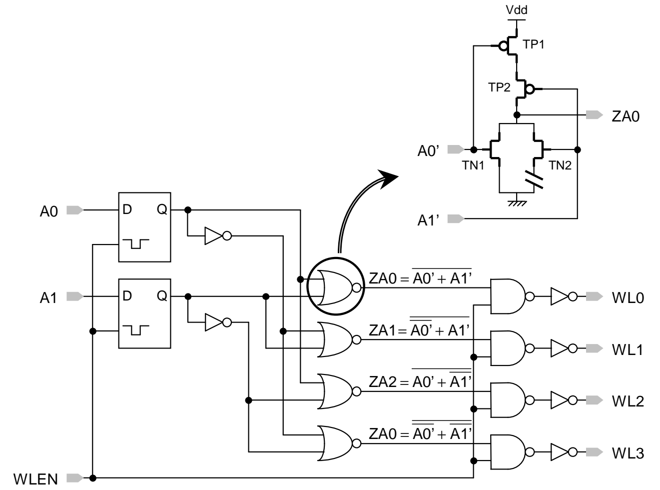

Figure 1: A NOR-based address pre-decoder

In the case of open defects placed in the serial plane of the NOR-gates between the connections of the PMOS transistors (TP1 and TP2 in Figure 1), there is not any pull-up of gate output. This time, the effect produced by the defect is different. When WL0 is addressed its selection does not occur. This particular open fault of address decoder is not sequential. It does not depend from a particular address sequence, but it appears every time the affected WL is addressed. March tests are able to sensitize and detect it. If the previous defect is a resistive open defect there is a delay in the pull-up of NOR-gate output and a consequent delay of WL selection. The test conditions are the same with additional timing constraints.

What stated above for NOR-based address decoders has the same validity for the complementary NAND-based architecture. In this case the parallel plane is placed in the pull-up path and the serial plane in the pull-down path. As for NOR-based architecture, the faults have a sequential behavior.

3. ADOFs and resistive-ADOFs detection

ADOFs and resistive-ADOFs involve sequential behavior due to their dynamic nature. The target of this paper is the comparison of sensitization and observation conditions for both of them.

3.1 ADOFs detection

When it is fault free, the address decoder in Figure 1, driven by signals A0 and A1, activates only one WL at a time. For example:

a. <A0, A1> = <0, 0>
   ⇒ WL0 is selected.

b. rising transition on A1: <A0, A1> = <0, 1>
   ⇒ WL2 is selected and WL0 is de-selected.

Now we describe with some details the sequential behavior of an ADOF taking as reference, as before, the address decoder of Figure 1 with the open defect in TN2, and the corresponding waveform shown in Figure 2. As mentioned before, the presence of an ADOF induces a wrong selection of two WLs:

a. <A0, A1> = <0, 0>
   ⇒ WL0 is selected.

b. rising transition on A1: <A0, A1> = <0, 1>
   ⇒ WL2 is selected and WL0 remains selected.

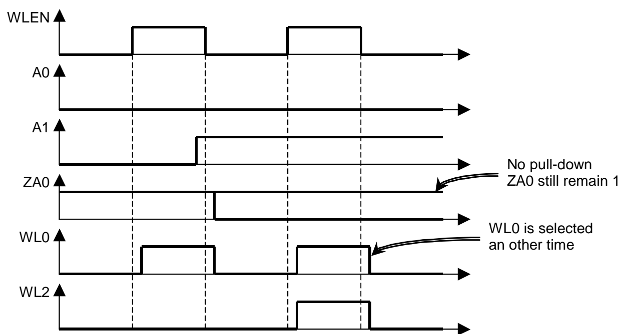

Figure 2: NOR-based address pre-decoder waveforms with an ADOF

In this case, the open defect in TN2 prevents the pull-down of the ZA0 node, that remains at logic level high because of the memory effect. In this example, we have first selected WL0, address <0, 0>, and after WL2, address <0, 1>. Between the two addresses only one-bit changes. This is required to sensitize the fault because a two bits transition from <0, 0> to <1, 1>, would activate both TN1 and TN2, thus discharging the node ZA0. So WL0 is correctly de-selected in presence of the open defect because transistor TN1 is 'on' and masks the faulty behavior of TN2. This shows that, in general, a test condition for this fault is an address sequence with a Hamming distance of 1 (Hd = 1), *i.e.* each address has to present only one bit transition in comparison with the previous one.

For the previous fault, an example of detection sequence is the following one:

1. Write ZERO at address <0, 0> (WL0 is active).
2. Write ONE at address <0, 1> (WL2 is active. WL0 remains active and there is a write operation in two locations when an ADOF is present in TN2).
3. Read address <0, 0> (ZERO is expected).

The phases 1 and 2 are for sensitization and phase 3 is for observation. This strategy has been proposed in [7, 8], where the author proposes an algorithm (Sachdev's algorithm) that produces a similar sequence which sensitizes and detects the ADOFs through the whole memory.

In general, for each WL, Sachdev's algorithm performs the following three phases:

a. '0' is written in a certain cell A.
b. '1' is written in a cell B, whose address has Hd = 1 from cell A.
c. cell A is read; a '0' is expected.

Phase b is iterated *m* times, *i.e.* for all the cells whose address has Hd = 1; *m* is the number of decoder inputs.

In presence of an ADOF, during phase b, '1' is written in cell B, but cell A is selected at same time and '0' stored before is overwritten with its opposite. Phase c allows the fault observation. Sachdev's algorithm is effective for sensitization and observation and its complexity is:

$$(2m+1)\times 2^{m}$$

Another test approach is the use of well-known March tests. This approach allows employing efficient linear tests. In general, March tests target static defects, but by applying their properties, called degrees of freedom [3], we can modify them to detect ADOFs. The condition for a March test to detect ADOFs is the following one:

> *For any open in the parallel path of address decoder gates, all two-pattern sequences with Hd = 1 have to be applied. With this prerequisite, any March test effective to cover non-sequential address decoder open fault (AF-Open) will detect this fault [13].*

There are many common March tests, like March C-, able to detect AF-Open. Applying one of these with the right pattern sequences covers all ADOFs.

In the literature, a few BIST structures have been proposed to generate address sequences with Hd=1 requisite, like the following ones:

- Complete LFSR (Linear Feedback Shift Register) [9].
- LHCA (Linear Hybrid Cellular Automata) [10].

3.2 Resistive-ADOFs detection

Figure 3 shows the path of the first of the four WLs of the address decoder presented in Figure 1. On the left side, the electric circuit of the NOR gate is depicted. We have injected a resistive open defect in TN2, in the three possible locations: on the source node, the drain node and the gate node. Simulations have been performed by varying the value of the resistive open defect in a range between 1 Ω and 2 MΩ, *i.e.* between an irrelevant defect and an almost open circuit.

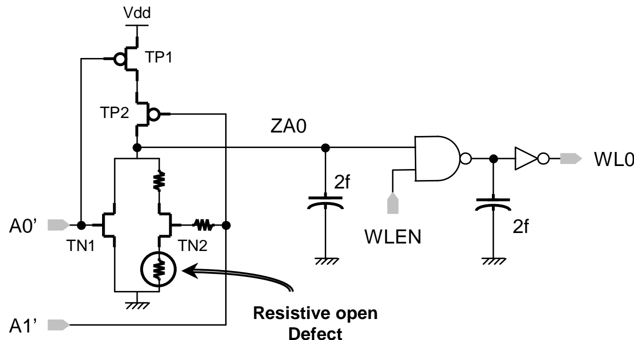

Figure 3: Electric simulation scheme of resistive open defect locations

Figure 4 shows the waveform of the simulations performed with a parametric resistive open defect in the source node of TN2, during the input transition <A0, A1> = <0, 0> → <A0, A1> = <0, 1>. The NOR-gate output presents a transition from the logic value '1' to '0' (pull-down). This transition exhibits a delay that increases linearly with the size of the injected resistance. This delay causes a consequent linear delay of the deselection of WL0. Other simulations have been performed with the injected resistance on gate drain nodes with similar delay effects. Figure 5 shows the results of the three simulations. The delay/resistance ratio is always linear, but the circuit is less sensitive to resistive defects placed on the gate node.

In case of a large resistive open defect, the circuit behaves as in presence of an ADOF. This is deducible from Figure 4. For large resistive open defect the delay in deselection of WL0 is longer than the clock period, thus the two WLs are selected during the whole read or write phases.

The consequences on the entire address decoder structure are observable in Figure 6. After the input transition <A0, A1> = <0, 0> → <A0, A1> = <0, 1>, WL2 is correctly activated, while WL0 remains selected erroneously for a certain time due to the delay of the pull-down operation.

In case of a very little resistive open defect, the delay perturbation introduced in the circuit is irrelevant and not pathological.

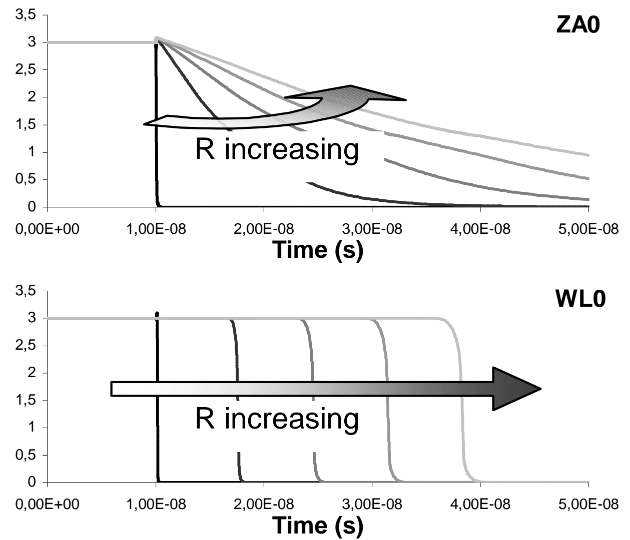

Figure 4: Variable delay in WL0 deselection depending on the resistive open defect value – defect inserted in the source of TN2

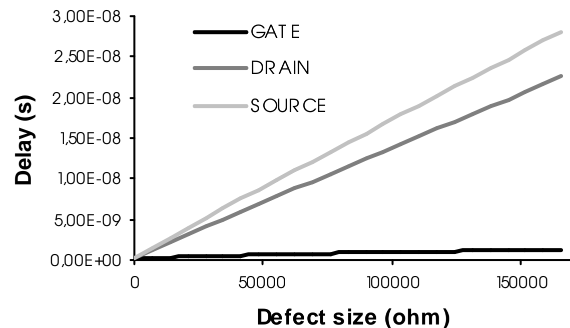

Figure 5: Variable delay in WL0 deselection depending linearly on the resistive open defect value – defect placed in the source, drain and gate of TN2

In case of intermediate resistive open defect, the delay produced during the WL0 deselection is partial. So we have the correct selection of WL2 and for a certain time the concomitant selection of WL0. This time, there is a high probability that a dynamic fault occurs, with the same effects of an ADOF. The same result has been illustrated in [13].

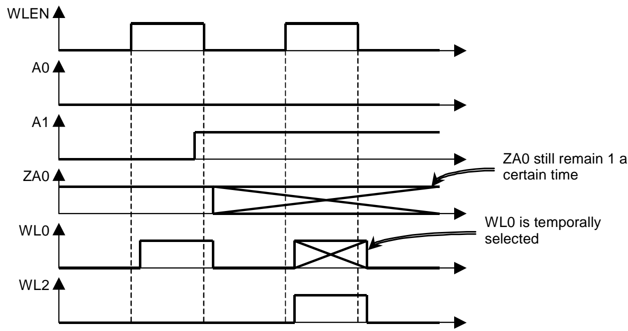

Figure 6: NOR-based address pre-decoder waveforms with a resistive open defect

Sachdev's algorithm is effective for the sensitization of resistive-ADOFs and it is effective for observation if the delay exceeds the sensing phase of the write operation. In fact, with this algorithm the partial double addressing occurs during a write access. The same occurs for modified March tests that are effective for the sensitization. They are effective for observation if the delay exceeds the sensing phase of the operations done during the double addressing.

For resistive-ADOFs another modification of March tests has been proposed in [11]. In this paper, the author presents a parallel March test. It is parallel because during the sensing phase in the memory cells for the write operation, different logic values are written for different bit-lines. During the observation phase in case of defect presence, a read operation occurs for two WLs at the same time, while all possible logic combination are produced on different bit-lines, allowing the detection independently from the predominant logic state.

4. ADOFs vs. resistive-ADOFs

The previous section shows essentially that ADOFs and resistive-ADOFs can be treated with the same test strategy. In particular, we can assume that ADOFs are a sub-class of resistive-ADOFs. Hence, we can formulate the following statements:

- **Sensitization:** For ADOFs and resistive-ADOFs, defect sensitization requires the same condition.

For any open and resistive open defect in the parallel plane of the address decoder gates, all two-pattern sequences with Hamming distance Hd=1 have to be applied.

In presence of ADOFs or resistive-ADOFs, a double simultaneous addressing is produced only if this condition is satisfied.

- **Observation:** Between ADOFs and resistive-ADOFs, the main difference is the observation phase after the sensitization.

Figure 7 is referred to a resistive-ADOF injection in the address decoder of Figure 1. In these waveforms we define *Ts* as the latch setup time, *T* as the sum between *Th* (latch hold time) and *Tgate* (delay of address decoder logic gates) and δ as the resistive open defect size which we consider fixed for the three simulations.

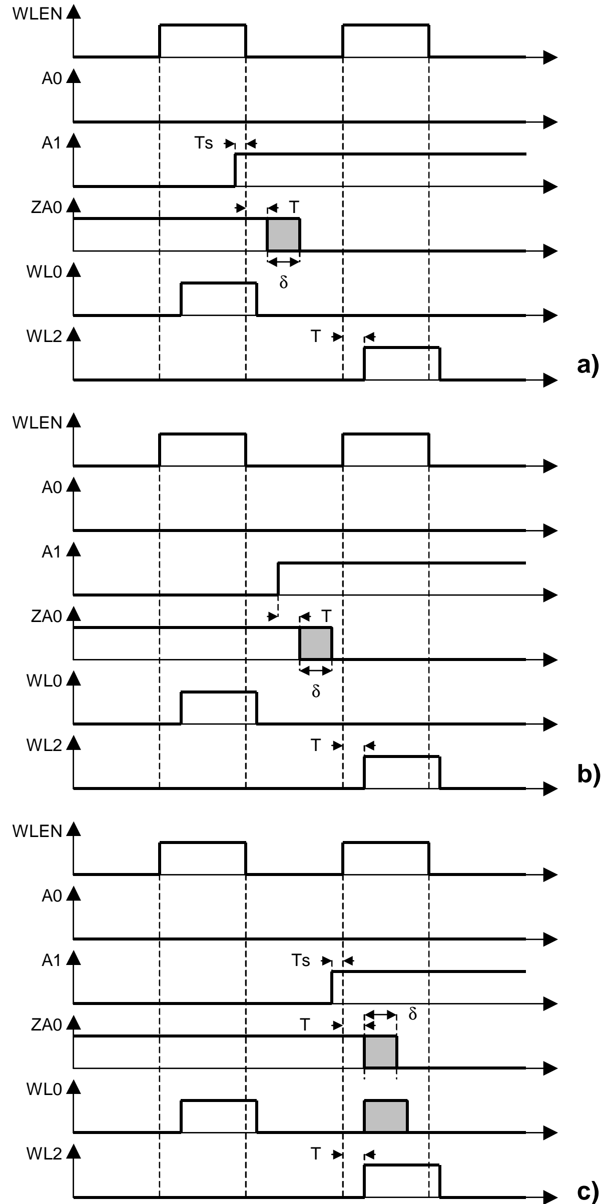

Figure 7: NOR-based address pre-decoder waveforms with a fixed resistive open defect and various address transition location

In Figure 7.a, A1 commutes when WLEN is not active (state logic 1). This involves a falling transition on ZA0 with a delay $T+\delta$. In this case, they are not malfunctions because there is enough time for the ZA0 pull-down.

In the second case (Figure 7.b), the address transition occurs during the active state of WLEN. As previously, there is enough time for the ZA0 pull-down and so, any malfunction does not appear.

Finally, in Figure 7.c, the address transition occurs exactly Ts before the WLEN deactivation. This time, WL0 is erroneously selected for a certain time. The third case is the best test condition to observe resistive-ADOFs. In fact, this way the littlest resistive open defect size is detectable independently of the clock frequency. If this condition (address transition close to WLEN deactivation) is not warranted then at-speed test allows to increase the resistive-ADOFs coverage.

Consequently to these remarks, the required observation conditions for ADOFs and resistive-ADOFs are the following ones:

1. *In presence of ADOFs, the faulty behavior of the circuit induces a double addressing for the whole sensing phase of operations. The fault is observable.*
2. *In presence of intermediate resistive-ADOFs the incorrect dual WL or BL selection persists for a portion of the sensing phase of operations. The presence of malfunctions is strictly related to the occurrence of the address transition. The best test condition is obtained for address transition close to WLEN deactivation. At-speed test is the best compromise in absence of this condition.*

As said in Section 2, the above statements are valid for NOR-based address decoders and NAND-based complementary architectures. In both cases the faults show a sequential behavior. For NAND-based architecture, the parallel plane is placed in the pull-up path and the serial plane in the pull-down path.

5. Concluding remarks and future work

The present study has focused on dynamic defects that may occur in address decoders. In particular, we have considered ADOFs and their generalization, resistive-ADOFs.

The comparison between ADOFs and resistive-ADOFs test conditions (sensitization and observation) has shown that ADOFs are a sub-class of resistive-ADOFs. In other words, the same test conditions can be used for both of them, but in the case of resistive-ADOFs, there are more stringent temporal constraints that require address transition close to WLEN deactivation. At-speed test is the best compromise in absence of the previous condition. In fact, in this case, the time between two consecutive WLEN selections is shorter and thus the address transition occurs closer to the *WLEN deactivation.*

We intend to continue this study of resistive-ADOFs by analyzing more carefully their effects on the memory array and on the input-output circuitry.

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