Polytech' Montpellier
ERII 4

Design of Analog ICs
Chapitre IV
Advanced Analog Design Techniques
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Outline
- Analog IC Design Flow
- Advanced specifications
- Advanced design techniques

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Offset considerations
- Definition: "input offset" of a differential amplifier is the differential input voltage that leads to a zero output voltage

Symmetrical Power Supplies !!!
Offset considerations

- Offset is a random phenomenon due to:
  - Technology spreading → low “frequency” variations (die to die; wafer to wafer; run to run)
  - Mismatches → high “frequency” variations (device to device)
  - Variability → hot topic covering both previous origins
    - affecting technology parameters and dimensions
    - generally following a Gaussian distribution.

- Propagation to circuit behavior
  - Example: incertitude on saturation current
    - \( \mu_{C_{ov}}, W/L \) and \( V_t \) are affected
  - \( \sigma_{I_{sat}} = \frac{2}{W/L} \left( V_{t1} - V_{t2} \right) \)

- Gaussian distribution basics
  - For a large number of identical devices the distribution of actual \( V_t \) (\( \mu_{C_{ov}}, W/L \)) follows a Gaussian distribution
  - 0.5% of the values are more than ±3\( \sigma \) away from the average value
  - 6\( \sigma \) designs are then the standard in industry
  - Run to run \( \sigma \) (technology spreading) is much higher than device to device \( \sigma \) (mismatches)
  - MC simulations

- Random offset in a current mirror
  - \( I_s = I_{sat} = \frac{\mu_{C_{ov}}}{2} \left( \frac{W}{L} \right) \left( V_{t1} - V_{t2} \right) \)

- Design tips
  - Large area and \( V_{eff} \), long
  - \( W=100\mu m \); \( L=1\mu m \); \( V_{eff}=0,1V \)
  - \( W=10\mu m \); \( L=10\mu m \); \( V_{eff}=1V \)

\[ \sigma_{V_t} = \frac{1.2mV}{600mV} = 0.2\% \quad \sigma_{\mu_{C_{ov}}} = 0.00056 = 0.056\% \quad \sigma_{W/L} = 2\% \]
- 50% more for a PMOS
- 10 times less for MOST on the same die (mismatches)
We've already studied...

Some variability parameters (wafer to wafer)

- Advanced specifications and variability
  - Uncertainties translate in a \( I_{\text{trans}} \) standard deviation
    \[
    \sigma_{I_{\text{trans}}} = \frac{I_{\text{trans}}}{V_L} \sigma_{V_L} + \frac{V_L}{I_{\text{trans}}} \sigma_{I_{\text{trans}}} + \ldots
    \]
  - Random offset in a simple current mirror...
    - Large transistors and large \( V_{\text{eff}} \)

Offset considerations

- Random offset in a differential pair with resistive load and symmetrical supply voltages
  \[
  V_{\text{off}} = \frac{R_1}{2} \frac{I_0}{V_{\text{eff}}} (\sigma_{V_{\text{trans}}} + \Delta V_{\text{sat}})
  \]
- Spreading in load resistors
  \[
  V_{\text{off}} = \frac{R_1}{2} \frac{I_0}{V_{\text{eff}}} \quad \Rightarrow \quad V_{\text{off}} = \frac{V_{\text{eff}}}{2} \frac{\Delta V_{\text{sat}}}{\mu C_{\text{ox}}} + \frac{\Delta W L}{W L}
  \]
- Other spreading
  \[
  V_{\text{off}} = R_1 \Delta I_{\text{sat}} + \frac{V_{\text{off}}}{2} \frac{\Delta V_{\text{sat}}}{\mu C_{\text{ox}}}
  \]

Common Mode Rejection Ratio, CMRR

- Definition: CMRR characterizes the ability of a differential amplifier to reject the common mode
  \[
  \text{CMRR} = \frac{A_{\text{MC}}}{A_{\text{MC,0}}} = A_{\text{MC,0}} - A_{\text{MC,0}} = 20 \log \left( \frac{A_{\text{MC}}}{A_{\text{MC,0}}} \right)
  \]

Offset considerations

- But offset can be also systematic
  - due to the chosen architecture, the bias point, a wrong layout (systematic mismatch)...
  - Must be fixed by designer !!!
- Examples
  - Related to design (layout)
    \[
    V_{\text{off}} = V_{\text{sat}} + R_{\text{L}} \Delta t
    \]
  - Related to usage
    - If \( V_{\text{off}} \) and \( V_{\text{eff}} \)
      \[
      \Delta t = \frac{V_{\text{off}}}{V_{\text{eff}}} \Delta t_{\text{sat}} - \Delta t_{\text{sat}}
      \]

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    - Common Mode Rejection Ratio
    - Design for low mismatches
    - Noise fundamentals
    - Characterization
- Advanced design techniques
Common Mode Rejection Ratio, CMRR

- Without $R_L$ spreading, $v_{inc}/(2R_B)$ in each load resistance
- Impact of spreading in MOST

$$v_{inc} = R_L \Delta (L_L) = R_L \frac{v_{inc}}{2R_B} \frac{\Delta W/L}{L/W}$$

$$\Rightarrow A_{inc} = \frac{v_{inc}}{v_{out}} = \frac{R_L}{2R_B} \left( \frac{2\Delta V}{V_{exp}} \frac{\Delta W/L}{L/W} \right)$$

Random CMRR and Offset trade-off

- Design of low offset and high CMRR differential pair

$$v_{inc} = \Delta V + \frac{V_{exp}}{2} \left( \frac{\Delta R}{R} \frac{\Delta W/L}{L/W} \right) \quad CMRR = \frac{2\Delta V}{V_{exp}} \frac{R}{\Delta W/L} \frac{\Delta W/L}{L/W}$$

- The lower the offset, the higher the CMRR
  1. Optimize for low offset
     - Low $V_{eff}$ (0.1V), large transistors, matched resistors
     - reduce $V_t$ spreading and current mismatch
  2. Optimize for large CMRR

Systematic CMRR

- Current source output resistance: $R_S$
- Common Mode $V_{inc}$ change bias current $V_{inc}/R_B$
- $V_{inc}/R_B$ equally shares between $T_1$ and $T_2$
- Small-signal analysis to calculate induced output voltage

$$CMRR = 2 \frac{R_{m1} R_{m2}}{R_{ds1} R_{ds2}}$$

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Design for low mismatches

Mismatch vs size for capacitors

- Wet etched
- Dry etched

- $2 : 1 : 2$
- $1 : 4$
Noise considerations

- Noise is any unwanted signal that interferes with a desired signal.
  - It can be deterministic or random.
  - It can be inherent to the circuit itself or coming from interferences with the outside world.
- Interference noise is caused by an identifiable external source. It can be deterministic or random.
  - e.g. 50Hz hum in a loudspeaker, cellular phone interfering with a TV set, …
  - It can usually be eliminated by proper methods of grounding, shielding, etc (electromagnetic compatibility, EMC)
- Inherent noise is generated by the circuit itself. It is always random.
  - e.g.: resistance and transistors are noisy
  - Different shape of random noises are thermal, shot and flicker
  - It can not be eliminated (inherent) but its effects can be reduced by changing the circuit structure or the power consumption.

Random noise basics

- Noise combination
  - Different noise sources combine as voltages in series and current in parallel
  - Assuming uncorrelated noise sources

\[
V_{n1}(t) + V_{n2}(t) = V_{n1(n1)} + V_{n2(n2)}
\]

• Frequency-domain analysis
  - Noise spectral density
  - Noise is considered only in the bandwidth of the system → filtered out elsewhere
  - Noise rms value @ 100Hz for a 90Hz bandwidth? A 0.1 Hz bandwidth?

\[
V^2_{n(100Hz)} = 10 \mu V^2/\sqrt{Hz}
\]

\[
V^2_{n(1Hz)} = 10 \mu V^2/\sqrt{Hz}
\]
### Inherent noise models

<table>
<thead>
<tr>
<th>Element</th>
<th>Noise Models</th>
<th>$k = 1.38 \times 10^{-23} J.K^{-1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor $R$</td>
<td>$V_{nR}^2 = 4kTR$ (Noiseless)</td>
<td></td>
</tr>
<tr>
<td>MOSFET $J_{DS}$ (Active region)</td>
<td>$V_{nJ}^2 = 4kT(q^2/2)J_{DS}$ (Noiseless)</td>
<td>$V_{T1}^2 = k \times W/L \cdot C_{ox}$</td>
</tr>
</tbody>
</table>

- **1/f noise tangent principle!!!**

### Noise considerations

- Basic considerations regarding noise in feedback systems

  - $V_{n1}$ represents the input noise in $v_i$.
  - $V_{n2}$ represents the equivalent input noise of $A_1$ and the output noise of $b_2$.

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**Cours Circuits Intégrés Analogiques**

**Chapitre II**

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**Wheatstone bridge SNR**

\[ V_{BBW} = \frac{V_{VBBW}}{2} \]

- **WL**: keep WL and \( V_{eff} \) constant

\[ WL = 10 \mu m^2 \Rightarrow W = \frac{10 \mu m^2}{L}; I_n = 28 \mu A \]

- \( L = \{1; 2; 5; 10; 20\} \rightarrow \delta(I_{diss}) = \sigma; \text{mean}(I_{diss}) = \mu A \)

**Effect of W/L**: keep WL and \( V_{eff} \) constant

\[ WL = 10 \mu m^2 \Rightarrow W = \frac{L}{W}; I_n = \frac{L}{W} ; I_n = 28 \mu A \]

- \( W/L = \{1; 2; 5; 10\} \)

**Case study: magnetometer signal conditioning**

**Wheatstone bridge SNR**

- **MC process & mismatch**: \( \delta(I_{diss}) = \sigma; \text{mean}(I_{diss}) = \mu A \)

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- **Analog IC Design Flow**
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  - Design for low-noise: active bridge example
  - Design for robustness: digitally programmable current source

**Characterization**

**Makes use of MC simulations**

**Define a DOE**

**Example: error in a current mirror**

- Set \( 1: 100 \) runs, \( T_1 \rightarrow T_2 \)

- Studied influences: \( V_{eff} \), WL, W/L, L

- Initial design: \( V_{eff} = 0.2 V \), W/L = 10, L = 1 \( \mu m \), \( V_S = 2 V \)

\[ I_n = I_{diss} = \frac{2kT}{2} \frac{W}{L} V_{eff}^2 = 28 \mu A \]

- MC process: \( \delta(I_{diss}) = \sigma; \text{mean}(I_{diss}) = \mu A \)

- MC process & mismatch: \( \delta(I_{diss}) = \sigma; \text{mean}(I_{diss}) = \mu A \)

**Design for low noise: active bridge example**

- **High power consumption**

- Targeted power consumption: 100 \( \mu A \) (for mobile applications) – less for autonomous systems

**Low resistance for SNR III**

- **Strain gauges**

- **Reference resistors**

- **SNR**

\[ \text{SNR}_{pp} = 20 \log \left( \frac{V_{cc} - V_{BBW}}{V_{BBW}} \right) - 20 \log \left( \frac{\Delta R}{R} \right) \]

- For a given signal (\( \Delta R/R \)), \( \text{SNR}_{pp} \) increases with \( V_{cc} \) and reduces with \( R \) and \( BW \)
Output SNR and LNA's noise figure

- LNA is necessary to reach a measurable signal
- LNA will amplify signal and noise of the WB
- LNA will add its own noise to the output
- LNA's noise figure $NF_{dB}$ is used to characterize the loss of SNR due to the LNA

\[
\Delta \text{SNR}_{dB} = 20 \log \left( \frac{V_{out} - V_{in}}{\sqrt{\text{BW} \times (V_{out} - V_{in})}} \right) = 20 \log \left( \frac{\Delta R \times V_{cc}}{R + \sqrt{6} \times V_{BW} \times \text{BW}} \right)
\]

Output SNR and LNA's noise figure

- Preserve input SNR by having an amplifier with negligible noise contribution
- Example: $R=1k\Omega$ and $V_{eff}=0.1V$
- How to reduce power consumption?

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  - Design for low-noise: active bridge example