Michel Renovell

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I) CURRICULUM

a) Professional Experience

2006-present	**Associate-Director of the ST2I (Sciences and Technology of Information and Engineering) Département at CNRS Headquarters.** The ST2I department manages more than 300 French labs.
2006-2009	**Director of the GDR SOC-SiP (CNRS French Network for Microelectronics Research)**
2004-2005	**Vice Chair of the IEEE Test Technology Technical Council TTTC (6000 members)**
2000-2005	**Head of the Microelectronics Team** of LIRMM (Laboratoire d'Informatique, Robotique et Microélectronique de Montpellier). The Microelectronics Team includes 25 permanent persons (Professor, Associate-Professor, Resarcher…) and 35 PhD students.
1992-2000	**Co-Head of the Microelectronics Team** of LIRMM
1986-1992	CNRS Researcher in the Microelectronics Team of LIRMM. Conducting research on defect-oriented testing, Analog circuit testing and FPGA testing.

b) Education

1996	'Habilitation à Diriger des Recherches', University of Montpellier, Montpellier, France.
1986	Ph.D. in Electrical Engineering, University of Montpellier, LIRMM, Montpellier, France.
1982	M.S. in Electrical Engineering, University of Montpellier, Montpellier, France.

c) Personnal data

Born	24 Octobre 1956, Montpellier, France.
Marital Status	married, 2 children.
Citizenship	France citizen.
Foreign lang.	English (fluent), Spanish (fluent).

d) Research profile

VLSI Testing	test, digital / analog / reconfigurable circuit testing, defect analysis, fault modelling

II) PROFESSIONAL ACTIVITY

a) Committee Chair

2006-xxxx	**Co-Chair for Europe of the Semiconductor Test Consortium – University Group**
2004-2005	**Vice-Chair of the IEEE *Test Technology Technical Council***
2003-2004	***Head of the French Test network (CNRS)***
2000-2004	***Chair of the Communication Group of the IEEE Test Technology Technical Council***
1996-2000	***Vice-Chair of the Technical Activity Group of the IEEE TTTC***
1999-present	***Chair of the FPGA Testing Technical Activity of the IEEE TTTC***

b) Permanent Editor of Journal

2006-present	***Editor of the Journal*** VLSI Design. Springer
2002-present	***Editor of the Journal*** IEEE Design & Test of Computers.
1998-present	***Editor of the Journal*** of Electronics Testing : Theory and Application (JETTA), Kluwer.

c) Awards

2006	**Best Paper Award DELTA2006 conference Kuala Lumpur Malaysia**
2005	**Best Paper Award Latin American Test Workshop 2005 Buenos Aires Argentina**
2003	***Nominated IEEE Computer Society Core Member***
2002	***Meritorious Service Award of IEEE Computer Society (received Baltimore - USA)***
2000-2004	**Certicate of Appreciation of IEEE Computer Society (received Washington)**
2001	***Teruhiko Yamada Memorial Award (received Kyoto – Japan)***

d) Reviewer for International Publishers/Institutions

2003-2005	***Reviewer for EEC Projects***
2005	***Reviewer for the Irish Science Foundation***
2005	***Reviewer for the Elsevier publisher***
2005	***Reviewer for the Morgan Kaufman Publishers***
2004	***Reviewer for the Dutch Agency for Technology (STW)***
2003	***Reviewer for the Canadian Science Foundation***

e) General Chair of Conferences

2008	**Co-*General Chair*** of the Int. Design & Test of Integrated System 2008 (Tunisia)
2008	***General Chair*** of the Int. Design & Diagnosis of Circuits and Systems 2008 (Slovaquia)
2006	**Co-*General Chair*** of the Int. Design & Test of Integrated System 2006 (Tunisia)
2004	***General Chair*** of the European Test Symposium 2004 (France)
2004	***Vice-General Chair*** of the East West Design & Test Workshop 2004 (Ukrain)
2003	***Vice-General Chair*** of the European Test Workshop 2003 (Netherland)
2002	***General Chair*** of the International Field Programmable Logic Conference 2002 (France)
2000	***General Chair*** of the IEEE International Mixed Signal Testing Workshop 2000 (France)

f) Executive Committee

2004-present	***Chair of the Executive Committee*** of the the International DELTA conference
2003-present	***Member of the Executive Committee*** of the Iberchip-Project
2003-present	***Member of the Executive Committee*** of the European Test Symposium
2002-present	***Member of the Executive Committee*** of the the International DELTA conference
2002-2004	***Member of the Executive Committee*** of the the Intern. Conf on Field Programmable Logic
2001-present	***Member of the Executive Committee*** of the International Workshop on Design and Diagnosis of Electronics Circuits.
2001-present	***Member of the Executive Committee*** of the International Conference on Design of Circuits and Integrated Systems.
2001-2006	***Member of the Executive Committee*** of the International DATE Conference (Design Automation and Test in Europe).
1999-present	***Member of the Executive Committee*** of the IEEE Intern. Mixed Signal Testing Workshop.

g) Program Chair

2008	***Program Chair*** of the South Brazilian Conf. on Integrated Circuit 2007 Porto Alegre Brazil
2008	***Program Chair*** of the International DELTA Symposium 2008 (Hong Kong)
2005	***Program Chair*** of the European Test Symposium 2005 (Estonia)
2005	***Vice-Program Chair*** of the East-West Design and Test Conference 2005 (Ukrain)
2004	**Vice-*Program Chair*** of the IEEE Intern. Mixed Signal Testing Workshop 2004 (USA).
2004	***Program Chair*** of the International DELTA workshop 2004 (Australia)
2003	***Program Chair*** of the IEEE International Mixed Signal Testing Workshop 2003 (Spain).
2002	***Program Chair*** of the International DELTA workshop 2002 (New Zealand)
2001	***Program Chair*** of the International Conference on Design of Circuits and Integrated Systems 2001 (Portugal)
2001	***Program Chair*** of the IEEE International Workshop on Design and Diagnosis of Electronics Circuits 2001 (Hungaria)
2000	***Program Chair*** of the Intern. Conf. on Design of Circuits and Integ. Systems 2000 (France)
1999	***Program Chair*** of the IEEE International Mixed Signal Testing Workshop 1999 (Canada)

h) Topic Chair

2007	***Topic Chair*** of the Latin-American Test Workshop 2007 (Lima Perou)
2006-2007	***Topic Chair*** of the European Test Symposium 2006 (England-UK)
2006	***Topic Chair*** of the VLSI Test Symposium 2006 (Berkeley USA)
2002-present	***Topic Chair*** of the **International Test Conference** (ITC).
2001-2003	***Topic Chair*** of the International DATE Conference (Design And Test in Europe).
1998-1999-2003	***Topic Chair*** of the IEEE European Test Workshop 1998 – 1999 - 2003.
1997	***Topic Chair*** of the International Conference on Innovative Systems 1997.

i) Tutorialist in International Conferences

2003-present	***IEEE Distinguish Lecturer***
2004	***Tutorial*** on FPGA Testing at the EWD&TC2004 Conference, Yalta, Ukrain.

2004	***Tutorial*** on FPGA Testing at the AQTR2004 Conference, Cluj-Napoca, Romania.
2004	***Tutorial*** on Defect Modeling at the DDECS2004 Conference, Bratislava, Slovaquia.
2004	***Tutorial*** on FPGA Testing at the LATW2004 Conference, Cartagena, Colombia.
2003	***Tutorial*** on FPGA Testing at the CSIT2003 Conference, Yerevan, Armenia.
2003	***Tutorial*** on Analog Circuit testing at the ISCAS2003 Conference, Bangkok, Thailand.
2003	***Tutorial*** on Defect Modeling at the IberChip2003 Conference, LaHavana, Cuba.
2002	***Tutorial*** on FPGA testing at the DCIS2002 Conference, Santander, Spain..
2002	***Tutorial*** on FPGA testing at the SBCCI2002 Conference, PortoAlegre, Brazil.
2002	***Tutorial*** on FPGA testing at the **International Test Conference** 2002, Baltimore, USA.

j) Member of Organizing Committee

2006	***Honorary Committee of*** the AQTR2006 Conference, Cluj-Napoca, Romania.
2006	**Europe Liaison for** the IEEE Asian Test Symposium (Furooka, Japan).
2004-present	**Finance *Chair*** of the IEEE VLSI Test Symposium (USA).
2003-2004	***Panel Chair*** of the IEEE Latin-American Test Workshop (Natal, Brazil).
2003-2004	***Publicity Chair*** of the IEEE Asian Test Symposium (Xian, China).
2003-2004	***Publicity Chair*** of the IEEE International Workshop on Defect-Based Testing (USA).
2003	***Publicity Chair*** of the IEEE VLSI Test Symposium (USA).
2002	***Tutorial Chair*** of the IEEE Intern. Mixed Signal Testing Workshop 2002 (Switzerland).

k) Editor of Proceedings

2002	***Editor of*** the International Field Programmable Logic Conference 2002 proceedings.
2002	***Editor of*** the International DELTA workshop (New Zealand) 2002 proceedings.
2001	***Editor of*** the IEEE Workshop on Design and Diag. of EC (Hungaria) 2001 proceedings.
2001	***Editor of*** the Intern. Conference on Design of Cir. and Integ. Systems 2000 (Portugal).
2000	***Editor of*** the Intern. Conference on Design of Cir. and Integ. Systems 2000 (France).

l) Member of Program Committee

ICCAD: 2006-present	International Conference on CAD
ITC: 2002-present	IEEE **International Test Conference**.
VTS: 2000-present	IEEE International VLSI Test Symposium.
DATE: 99-present	International Design And Test in Europe Conference.
ICCD: 2000-2002	International Conference on Circuit and Devices.
ETS: 96-present	IEEE European Test Workshop/Symposium.
ATS: 2001-present	IEEE Asian Test Symposium.
DBT: 2002-present	IEEE International Workshop on Defect-Based Testing.
IMSTW: 97-present	IEEE International Mixed Signal Testing Workshop.
TECS: 97-2003	IEEE International Workshop on Test of Embedded-Core Systems.
LATW: 2000-present	IEEE Latin-American Test Workshop.
DDECS: 2000-present	IEEE International Conference on Design and Diagnosis of Electronics Circuits.
ECS: 2001-present	IEEE International Conference on Electronic Circuit and Systems.
ISIS: 1997	International Conference on Inovative System in Silicon.
EDCC: 1996	European Dependable Computing Conference.
EWDC: 2001	European Workshop on Dependable Computing.
DCIS: 96-present	International Conference of Design of Circuits and Integrated Systems.
SBCCI: 98-present	South-Brasilian Conference on Integrated Circuit.

m) PhD Supervisor

2006-xxxx	Co-Supervisor of a PhD thesis in **Slovenia**
2006-xxxx	Co-Supervisor of a PhD thesis in **Iran**
2005-xxxx	Co-Supervisor of a PhD thesis in **Brazil**
2005-xxxx	Co-Supervisor of a PhD thesis in **Tunisia**
1990-present	Supervisor of 20 PhD students in France

n) Invited Paper

2005	International East-West Design & Test Workshop (Ukrania)
2005	Computer Science & Information Technology (Armenia)
2004	International Conference on Micro-Electronic (Tunisia)

2004 International Baltic Electronic Conference (Estonia)
2004 International System & Circuit Conference (Tunisia)
2003 International East-West Design & Test Conference (Ukrania)
2003 International Conference on Electronic Circuits and Systems (Slovaquia)
2001 International Symposium on Quality of Electron Devices (USA)
2000 International Test Conference (USA)
2000 International Conference on Field Programmable Logic (Austria)
1999 International Conference on Microelectronics (Algeria)
1998 Brasilian Conference on Integrated Circuit (Brazil)

o) Invited Seminar

2006 University of Cordoba (Argentina)
2006 University of Porto Alegre Brazil 2006 (Brazil)
2005 VirageLogic Yerevan (Armenia)
2003 Freiburg University 2003 (Germany)
2002 Stanford University 2002 (USA)
2000 CNES 2000 (France)
2000 AT&T Bell Labs Princeton 2000 (USA)
2000 University of Porto Alegre Brazil 2000 (Brazil)
2001 INTEL 2001 (USA)
1999 Sunrise California 99 (USA)
1999 Logic Vision California 99 (USA)
1999 University of Rio de Janeiro 99 (Brazil)
1998 University of Britsh Columbia (Canada)
1998 University of Victoria 98 (Canada)
1998 Quickturn California 98 (USA)
1997 University of Sao Paolo 97 (Brazil)

III) PRODUCTION :

a) Patent

FPGA Patent on FPGA testing, In Progress.
ADConverters International Patent on BIST for A to D Converters, Septembre 99.

b) Invited Papers in Journal

1. M. Renovell "*Some Aspects of the Test Generation Problem for an Application-Oriented Test of SRAM-Based FPGAs*", Invited Paper for the Journal of Circuits, Systems and Computers, pp. 143-158, vol. 12, n° 2, April 2003, Word Scientific Publishing Company.

c) Invited Papers in International Conferences with Proceedings

1. M. Renovell "*From Dependable Computing Systems to Computing for Integrated Dependable Systems*", Invited Panel, Fault Tolerant Computing Symposium, FTCS-28, pp. 296-301, June 23-25, Munich, Germany, 1998.

2. M. Renovell "*SRAM-Based FPGAs: A Structural Test Approach*", Invited Paper for IEEE XI Brazilian Symposium on Integrated Circuit Design SBCCI98, pp. 67-72, Rio de Janeiro, Brazil, Oct. 98.

3. M. Renovell "*Testing embedded SRAM-Based FPGAs*", Invited Paper for IEEE International Conference on Microelectronics, Aug., Ottawa, Canada, 1999.

4. M. Renovell "*A specific test methodology for symmetric SRAM-based FPGAs*", Invited Paper for 10th International Conference on Field-Programmable Logic and Applications, pp. 300-311, Villach, Austria, August 27-30, 2000.

5. M. Renovell "*Different Experiments in Test Generation for XILINX FPGAs*", Invited Paper for IEEE International Test Conference ITC'00, pp. 854-862, Atlantic City, NJ, USA, Oct. 3-5, 2000.

6. M. Renovell "*Revisiting the Classical Fault Models through a Detailed Analysis of Realistic Defects*", Invited Paper for IEEE International Symposium on Quality of Electronic Design, pp. 359-364, San Jose, USA, 2001.

7. M. Renovell "*Testing Challenges for Modern FPGAs*", Invited Paper for the 4th IEEE International Conference on Electronic Circuits and Systems ECS'03, pp. 1-9, Bratislava, Slovaquia, Sept. 11-12, 2003.

8. M. Renovell "*Structural Testing of Modern Reconfigurable Chips*", Invited Paper for the International East-West Design and Test Conference EWDTC'03, Yalta, Ukrain, Sept. 18-21, 2003.

9. M. Renovell "Principe et Problématique pour le test des System-On-Chip", Invited Paper for the International Conférence sur les Signaux, Circuits et Systèmes SCS'04, pp. 1-3, Monastir, Tunisie, Mars 18-21, 2004.

10. M. Renovell "Realistic Fault Models for Defects in Electronic Circuits", Invited Paper for the International Baltic Electronic Conference BEC'04, pp. 33-37, Tallin, Estonia, Octobert 4-6, 2004.

11. M. Renovell "Fundamentals of System Testing : Challenges for System-On-Chips", Invited Paper for the International Conference on Microelectronics ICM'04, pp. 176-180, Tunis, Tunisia, December 6-8, 2004.

12. M. Renovell "Modelization and Detection of Realistic Defects in CMOS Technology", Invited Paper for the International East-West Design and Test Conference EWDTC'05, Odessa, Ukrain, Sept. 15-19, 2005.

13. M. Renovell "Testing for Realistic Defects", Invited Paper for the International Conference on Computer Science and Information Technology CSIT'05, Yerevan, Armenia, Sept. 19-22, 2005.

d) Contribution to Book

1. F. Azais S. Bernard, Y. Bertrand, M. Renovell, "On-Chip Generator of a Saw-Tooth Test Stimulus for ADC BIST", Selected papers from the 11th International Conference on Very Large Scale Integration of Systems-on-Chip, Kluwer Academic Publishers, ISBN: 1-4020-7148-5, pp. 425-436, 2002.

2. M. Renovell En collaboration avec Azais, S. Bernard, Y. Bertrand, M.L. Flottes, P. Girard, C. Landrault, B. Rouzeyre, S. Pravossoudovitch, "Test de Circuits et Systèmes Intégrés", auteur d'un chapitre, Hermes Science publications, ISBN 2-7462-0864-4, 2004.

3. M. Renovell En collaboration avec S. Bernard, P. Cauvet "Design for Testability Architecture", auteur d'un chapitre sur les SiP, Kluwer Academic Press, to appear on December 2006.

e) Journal

1. M. Renovell G. Cambon, D. Auvergne, *"FSPICE: A tool for fault modeling in MOS circuits*", Integration the VLSI journal 3, pp. 245-255, 1985.

2. M. Renovell G. Cambon*, "Topology dependence of floating gate faults in MOS integrated circuits*", IEE Electronics Letters, vol. 22, no 3, pp. 152-153, Jan. 1986.

3. M. Renovell G. Cambon, *"Electrical analysis and modeling of Floating-Gate Fault",* IEEE Transactions on CAD of ICs and Sys, Vol. 11, no 11, Nov. 1992, pp. 1450-1458

4. M. Renovell P. Huc, Y. Bertrand, *"Realistic fault model for External Shorts in MOS Technologies",* IEE Electronics Letters, Vol. 29, no 9, pp. 813-814, April 1993.

5. M. Renovell J. Figueras, *"Current Testing in Dynamic CMOS Circuits",* Jour. of Electr. Testing : Theory and Application (JETTA), Kluwer Academic Publisher, Vol. 6, no. 1, pp. 127-131, Feb. 1995.

6. S. Lavabre, Y. Bertrand, M. Renovell, C. Landrault, *"Testability Improvements of Sequential Circuits by Emulation of Test Configurations",* Journal of Solid State Devices and Circuits, Vol. 4, n°1, Jan. 1996, pp. 32-38.

7. M. Renovell, F. Azais, Y. Bertrand, *"On-Chip Signature Analyzer for Analogue Circuit Testing",* IEE Electronics Letters, vol. 32, no 24, pp. 2185-2186, September 1996.

8. M. Renovell, J.M. Portal, J. Figueras, Y. Zorian, *"Testing the Interconnect Structure of RAM-Based FPGA",* IEEE Design & Test, Vol. 15, n°1, pp.45-50, January-March 1998.

9. M. Renovell, J.M. Portal, J. Figueras, Y. Zorian, *"SRAM-based FPGA: Testing the Embedded RAM Modules"*, Journal of Electr. Testing: Theory and Application (JETTA), Kluwer Academic Publisher, pp. 159-167, Vol. 14, n°1/2, Jan./Fev. 99.

10. M. Renovell, F. Azais, Y. Bertrand, *"Detection of Defects Using Fault Model Oriented Test Sequences"*, Journal of Electr. Testing: Theory and Application (JETTA), Kluwer Academic Publisher, pp. 13-22, Vol. 14, n°1/2, Jan./Fev. 99.

11. M. Renovell F. Azais, J-C Bodin, Y. Bertrand, *"Combining Functional and Structural Approaches for Switched-Current Circuit Testing"*, Journal of Electr. Testing: Theory and Application (JETTA), Kluwer Academic Publisher, 2000.

12. M. Renovell J.M. Portal, J. Figueras, Y. Zorian, *"Testing the Local Interconnect Resources of SRAM-based FPGAs"*, Journal of Electr. Testing: Theory and Application (JETTA), Kluwer Academic Publisher, 2000.

13. M. Renovell J.M. Portal, J. Figueras, Y. Zorian, *"An Approach to Minimize the Test Configurations for the Logic Cells of the XILINX XC4000 FPGA Family"*, Journal of Electr. Testing: Theory and Application (JETTA), Kluwer Academic Publisher, 2000.

14. F. Azais M. Renovell, Y. Bertrand, A. Ivanov, S. Tabatabaei, *"PLL Testing: A Unified Digital Test Approach"*, IEEE Design & Test, 2000.

15. M. Renovell F. Azais, Y. Bertrand, *"Analyzing Some Cases of Test Escapes"*, IEEE Design & Test, 2000.

16. A. Ivanov S. Rafiq, M. Renovell, F. Azais, Y. Bertrand, *" On the detectability of CMOS floating gates transistor faults"*, IEEE Transactions on CAD, Vol. 20, n° 1, January 2001, pp. 116-128.

17. F. Azais S. Bernard, Y. Bertrand, M. Renovell, *"A low-cost BIST architecture for linear histogram testing of ADCs"*, Journal of Electronic Testing (JETTA), Kluwer Academic Publisher, Vol. 17, n° 2, April 2001, pp. 139-147.

18. F. Azais S. Bernard, Y. Bertrand, M. Renovell, *"Optimizing sinusoidal histogram test for low cost ADC BIST"*, Journal of Electronic Testing (JETTA), Kluwer Academic Publisher, Vol. 17, n° 3/4, June/August 2001, pp. 255-266.

19. M. Renovell J.M. Portal, P. Faure, J. Figueras, Y. Zorian, *"A discussion on test pattern generation for FPGA - Implementated circuits "*, Journal of Electronic Testing (JETTA), Kluwer Academic Publisher, Vol. 17, n° 3/4, June/August 2001, pp. 283-290.

20. F. Azais S. Bernard, Y. Bertrand, M. Renovell, *"Analog Built-In Saw-Tooth Generator for ADC Histogram Test"*, Microelectronics Journal (MEJO), Elsevier Sciences, Vol. 33, Issue 10, pp. 781-789, Oct. 2002.

21. F. Azais S. Bernard, Y. Bertrand, M. Comte, M. Renovell,*"A-to-D Converters Static Errors Detection from Dynamic Parameters Measurement"*, Microelectronics Journal (MEJO), Elsevier Science, vol. 34, n°10, pp.945-953, 2003.

22. F. Azais Y. Bertrand, M. Renovell, A. Ivanov, S. Tabatabataei, *"An all Digital DFT Scheme for testing catastrophic faults in PLL"*, IEEE Design & Test of Computer, Vol. 20, Issue 1, pp. 60-67, Jan-Feb. 2003.

23. F . Azais S. Bernard, M. Comte, Y. Bertrand, M. Renovell and M. Lubazewski, "*Estimating Static Parameters of A-to-D Converters from Spectral Analysis* ", Journal of Electronic Testing (JETTA), Kluwer Academic Publisher, 2003.

24. S. Bernard F. Azais, Y. Bertrand, M. Renovell, "On-chip Generation of Ramp and Triangle –Wave Stimuli for ADC BIST", Journal of Electronic Testing (JETTA), Kluwer Academic Publisher, vol. 19, n°4, pp. 469-479, August 2003.

25. M. Renovell J.M. Galliere, F. Azais, Y. Bertrand, "Modelling the Random Parameters Effects in a Non-Split Model of Gate Oxide Short", Journal of Electronic Testing (JETTA), Kluwer Academic Publisher, Vol. 19, n°4, August 2003, pp. 377-386.

26. I. Polian P. Engelke, M. Renovell, and B. Becker, "Modeling Feedback Bridging Faults with non-zero Resistance", Accepted to appear in Journal of Electronic Testing (JETTA), Kluwer Academic Publisher, 2004.

27. S. Bernard M. Comte, F. Azais, Y. Bertrand, M. Renovell, "Efficiency of Spectral-based ADC Test Flows to Detect Static Errors", Journal of Electronic Testing (JETTA), Kluwer Academic Publisher, vol. 20, n°3, pp. 257-267, June 2004.

28. F. Azais S. Bernard, M. Comte, Y. Bertrand, M. Renovell, M. Lubaszewski, "Correlation between Static and Dynamic Parameters of A-to-D Converters in the viewof a Unique Test Procedure", Journal of Electronic Testing (JETTA), Kluwer Academic Publisher, vol. 20, n°4, pp. 375-387, August 2004.

29. A. Gonzales M. Lubaszewski, L. Carro and M. Renovell, "A New FPGA for DSP Applications Integrating BIST Capabilities", Journal of Electronic Testing (JETTA), Kluwer Academic Publisher, vol. 20, n°4, pp. 423-431, August 2004.

30. R. Bouchakour J.M. Portal, J.M. Galliere, F. Azais, Y. Bertrand, , M. Renovell, "A Compact DC Model of Gate Oxide Short Defect", Microelectronic Engineering, Vol. 72, 1-4, pp. 140-148, 2004.

31. F. Azais S. Bernard, M. Comte, Y. Bertrand, M. Renovell, "Efficiency of Optimized Dynamic Test Flows for ADCs: Sensitivity to Specifications", Journal of Electronic Testing: Theory and Applications (JETTA), Kluwer Academic Publisher, vol. 21, n°3, pp. 291-298, December 2004.

32. F. Azais M. Lubaszewski, P. Nouet, M. Renovell, "A Strategy for Optimal Point Insertion In Analog Cascaded Filters", Journal of Electronic Testing (JETTA), Kluwer Academic Publisher, vol. 21, n°1, pp. 9-16, 2005.

33. M. Renovell J.M. Galliere, F. Azais, Y. Bertrand, “Delay Testing Viability of MOS Transistors with Gate Oxide Shorts”, Journal of Computer Science and Technology, Vol. 20, n°2, pp. 195-200, 2005.

34. P. Girard O. Heron, S. Pravossoudovitch, M. Renovell, “Delay Fault Testing of Look-Up Tables in SRAM-Based FPGAs”, Journal of Electronic Testing (JETTA), Kluwer Academic Publisher, vol. 21, n°1, pp. 43-55, 2005.

35.T.R. Balen A. Andrade, F. Azais, M. Lubaszewski, M. Renovell, *“Applying the Oscillation Test Strategy to FPAA’s Configurable Analog Blocks*", Journal of Electronic Testing (JETTA), Kluwer Academic Publisher, vol. 21, n°2, pp. 135-146, 2005.

36. P. Girard O. Heron, S. Pravossoudovitch, M. Renovell, “An Efficient BIST Architecture for Delay Faults in the Logic Cells of Symmetrical SRAM-Based FPGAs”, Journal of Electronic Testing (JETTA), Kluwer Academic Publisher, vol. 22, n°2, pp. 161-172, April 2006.

f) Refered Conference Proceedings

1. M. Renovell G. Cambon, D. Auvergne, *"Modeling and electrical simulation of faults in MOS integrated circuits",* Intern. Conf.on CAD, pp. 89-92, Paris, Jun.1985.

2. M. Renovell P. Faure, G. Cambon, *"Mask dependent models of faults in MOS integrated circuits",* IC Technology Conf., Limerick, Eire, pp. 125-134, September 1986.

3. M. Renovell P. Faure, G. Cambon, *"Modélisation logique des grilles flottantes dans les technologies MOS",* 3rd Intern. Conf. QEC, pp. 29-34, Bordeaux, March 1987.

4. A. Elleuch M. Renovell, J. Lassalle, G. Cambon, *"Méthodologie et outil d'extraction automatique des sites de pannes",* Intern. Conf. on Microele, Alger, Nov. 1988.

5. A. Elleuch M. Renovell, J. Lassale, G. Cambon, *"Transistor à grille flottante : Modélisation logique de pannes dépendantes de la topologie",* International Conference on Microelectronics 88, Alger, novembre 1988.

6. M. Renovell S. Rayon, Y. Bertrand, G. Cambon, *"Testability Design for PLA-Implemented FSM",* 1st European Test Conf. (ETC), pp. 246-251, Paris, Ap. 1989.

7. M. Renovell A. Elleuch, J. Lassale, G. Cambon, *"Automatic Extraction and Modelisation of Layout Dependent Faults",* 12th Fault-Tolerant Systems and Diagnosis Conference, Prague, Tchécoslovaquie, pp. 96-100, Septembre 1989.

8. M. Renovell G. Cambon, A. Elleuch, J. Lassale, "*Computer Aided Location and Model Analysis of Faults in MOS Integrated Circuits*", ISSSE'89 International Symposium on Signals Systems and Electronics, Erlangen RFA, pp. 609-612, Sept. 89.

9. M. Renovell S. Rayon, Y. Bertrand, G. Cambon, *"Short Fault in Dynamic CMOS PLA",* 13th Fault Tolerant Syst. and Diagnosis Conf., Varna, Bulgarie, June 1990.

10. M. Renovell M. Ildevert, Y. Bertrand, *“Autonomously testable dynamic CMOS PLAs",* Europ. Test Conf. ETC'91, Munich, RFA, April 10-12, 1991, p. 519.

11. M. Renovell M. Ildevert, Y. Bertrand, *“DCPLA : A new BIST design for dynamic CMOS PLAs",* International Test Conf., Nashville, TN, USA, Oct. 28-31, 1991.

12. M. Renovell M. Ildevert, Y. Bertrand, *“A low overhead BIST scheme for dynamic CMOS PLAs",* Int. Conf. on VLSI Design, India, jan. 1992, pp. 352-355.

13. C. Counil M. Renovell, G. Cambon, *“Self-Test for F.I.R.filters",*VLSI Signal Processing V, Edited by K. Yao, R. Jain, W. Przytula, IEEE 1992, pp. 51-60.

14. C. Counil M. Renovell, G. Cambon, *“BIST for mixed signal analog/digital circuits",* Int. Symp. on Signals, Syst and Elect., Paris, 1-3 September 1992, pp. 958-961.

15. Y. Bertrand F. Bancel, M. Renovell, *“A DFT Technique to improve ATPG efficiency for seq. cir.",* Int.Conf. on VLSI Des., Bombay, India, Jan. 1993, pp. 51-54.

16. Y. Bertrand F. Bancel, M. Renovell, *“A new DFT Tech. to reduce test duration for seq. circ.",* Eur. Test Conf., Rotterdam, Netherland, Ap. 21-23, 1993, pp. 489.

17. Y. Bertrand F. Bancel, M. Renovell, *“Multiconfiguration Tech to reduce test duration for seq. cir.",* Int. Test Conf., Nashville, USA, October 1993, pp. 989-997.

18. M. Renovell P. Huc, Y. Bertrand, “*Fault Modelisation of External Shorts in CMOS Circuits*“, Asian Test Symposium, Nov.17-18, Pekin, China, 1993, pp. 237-242.

19. M. Renovell P. Huc, Y. Bertrand, *“CMOS Bridging Fault Modeling",* IEEE 12th VLSI Test Symposium, April, New Jersey, USA, 1994, pp. 392-397.

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