Power Supply Noise and Ground Bounce Aware Pattern Generation for Delay Testing

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As technology scales down, the effects of power supply noise and ground bounce are becoming significantly important. In the existing literature, it has been shown that excessive power supply noise can affect the path delay, while ground bounce is either neglected or assumed similar to power supply noise. Our work performs a detailed study of combined and uncorrelated power supply noise and ground bounce and their impact on the path delay. Our analyses show that different combination of power supply noise and ground bounce can lead to either delay speed-up or slow-down.

Our objective is to generate test patterns such that the combined effects of power supply noise and ground bounce are considered on circuit delay analysis. The impact of noise on delay is highly depended on the applied input patterns. Our research seeks to provide mathematical models to represent the circuit based on the physical extracted data after the circuit is placed & routed with power/ground grids. We propose close-form mathematical models to capture the impact of input patterns on path delay in the presence of power supply noise and ground bounce. We use a simulated annealing (SA) based approach to find patterns that maximize the critical path delay. In contrast to previous works which initially aim to find patterns for maximum supply noise and then compute delay, our method targets directly to find the worst case delay which might not necessarily occur under worst case power supply noise due to the speed-up/slow-down phenomena. Our method generates patterns that sensitize the path and also cause such power supply noise and ground bounce that leads to the maximum path delay.

References:


Figure 1 shows a sample two buffer circuit and its power and ground networks. As the gates are placed in different locations on the chip, the amount of power supply noise and ground bounce that they experience can vary significantly among them. Such variations on the power and ground networks lead to variations on the path delay which can be either a speed-up or slow-down effect.

(a)

(b)