



ART-2017

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2nd IEEE International Workshop on **Automotive Reliability & Test**

in conjunction with ITC / Test Week 2017 Fort Worth Convention Center, TX, USA November 2-3, 2017

The ART workshop focuses exclusively on test and reliability of automotive and mission-critical electronics, including design, manufacturing, burn-in, system-level integration and in-field test, diagnosis and repair solutions, as well as architectures and methods for reliable and safe operations under different environmental conditions. With increasing system complexity, security, stringent runtime requirements for functional safety and cost constraints of a mass market the reliable operation of electronics in safety-critical domains is still a major challenge. The ART Workshop offers a forum to present and discuss challenges and solutions among researchers and practitioners alike.

Organizing Committee

General Chair:	Y. Zorian, Synopsys
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Program Chair:	P. Bernardi, Polito Torino
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Publication:	M. Restifo, Polito Torino
Publicity:	L. Anghel, TIMA Laboratory
Registration:	T. McLaurin, ARM
Electronic Media:	A. Bosio, LIRMM

ART-2017 Schedule

2nd November, 2016

4:00 – 4:15 P.M.

Opening Remarks

General chair: Yervant Zorian (Synopsys, US) *Program chair:* Paolo Bernardi (Politecnico di Torino, I)



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Keynote1 – Mauro Pipponzi Function Safety Manager Intel

4:15 - 5:00 P.M.

The Pivotal Role of Automation in Functional Safety

Session 1 – Functional Safety Solutions from the Industry

5:00 - 6:30 P.M.

Moderator: Vincent Huard, STMicroelectronics FR

System-on-Chip Online Self-Test Runtime Control for Functional Safety

Christophe Eychenne¹, Gurgen Harutyunyan², Yervant Zorian (¹Bosch FR – ²Synopsys US)

Towards an ISO26262 Compliant DFT Architecture Enabling POST for Ultra-Large-Scale Automotive MCU

Yoichi Maeda¹, Hiroyuki Iwata¹, Jun Matsushima¹, Senling Wang², Yoshinobu Higami² and Hiroshi Takahashi² (¹Renesas Electronics Corporation - ²Ehime University JP)

Fault Grading of Functional Safety Mechanisms for Interconnect Block of Automotive SoCs

Federico Venini^{1,2}, Paolo Bernardi², Oscar Ballan¹, Wern Koe¹, Pranjal Chauhan¹, Shashidhar Surabhatt Krishnamurthy¹ and Sanjeeva Reddy Duggampudi¹ (¹Xilinx US – ²Politecnico di Torino I)

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Workshop Reception

7:00 – 9:00 P.M.

3rd November, 2017



Keynote2 – Kevork Kechichian Senior Vice President Engineering Qualcomm

8:15 – 9:00 A.M.

Session 2 – On-Line Embedded Memory Testing

9:00 - 10:00 A.M.

Moderator: Saman Adham, TSMC US

Comprehensive Online Functional Safety Solutions for Embedded Memories

Gabriele Boschi¹, E. Spanò¹, Riccardo Mariani¹, Gurgen Harutyunyan², Yervant Zorian² (¹Intel I – ²Synopsys US)

On-Line Software-based Self-Test of RAM Memories ECC Logic Marco Restifo¹, Paolo Bernardi¹, Sergio De Luca² and

Alessandro Sansonetti² (¹STMicroelectronics I – ²Politecnico di Torino I)

Coffee Break

10:00 - 10:30 A.M.

Session 3 – Automotive design

10:30 - 12:00 A.M.

Moderator: Gurgen Harutyunyan, Synopsys US

A Hierarchical DFT Architecture for Automotive Designs Nilanjan Mukherjee¹, Mohammed Abdelwahid¹, Ron Press¹, Tal Kogan², Amihay Rabenu², Tal Frucht² and Tay Kroul² (¹Mentor Graphics US – ²Intel ISR)

BIST On-Demand Using Distributed On-Chip Programmable Data Streams Carl Wisnesky Ii¹ and Patrick Gallagher¹ (¹Cadence US)

Joint Design/Test Approach to Manage Reliability Of Automotive Products In Advanced CMOS Nodes Vincent Huard¹, Souhir Mhira¹, Philippe Flatresse¹ and Alain Bravaix² (¹STMicroelectronics FR - ²ISEN-REER FR)

Lunch

12:00 A.M. – 1:00 P.M.

Embedded Tutorial – ISO 26262 Metrics

1:00 – 1:40 P.M.

Moderator: Adam Cron, Synopsys US

Measuring ISO 26262 Metrics of Digital and Mixed-Signal Circuitry in ICs

Stephen Sunter¹, Krzysztof Jurga² and Joe Dailey³ (Mentor, a Siemens Business ¹CDN, ²PL and ³US)

ART-2017 Schedule

Panel – Automotive Reliability and Test Perspectives from Industry

1:40 - 2:40 P.M.

Organizer: Paolo Bernardi, Politecnico di Torino I Moderator: Yervant Zorian, Synopsys US

Gabriele Boschi, Intel US Souhir Mihra, STMicroelectronics FR Daniel Tille, INFINEON D Federico Venini, Xilinx US – Politecnico di Torino I

Abstract: the panel will cover a broad spectrum of subjects, including open issues in the field of Automotive Reliability and Test perspectives for the next years from major companies. Panelists will address audience comments and remarks during open discussion following short presentations.

Break

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Session 4 – Industrial Flows from Verification to Manufacturing and In-Field

2:50 - 3:50 P.M.

Moderator: Marco Restifo, Politecnico di Torino I

Decreasing Defect Slippage using Formal verification of Automotive UML Designs Ghada Bahig¹ and Amr Elkadi² (¹Mentor Graphics ET, ²American University in Cairo ET)

The SRS platform - an approach for fail operational radar measurements and communication in highly automated driving

Markus Ulbricht, Mario Schölzel, Rizwan Tarig Syed and Milos Krstic (IHP D)

Closing Discussions

3:50 - 4:00 P.M.

2:40 - 2:50 P.M.

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