MAGPIE TUTORIAL

Introduction

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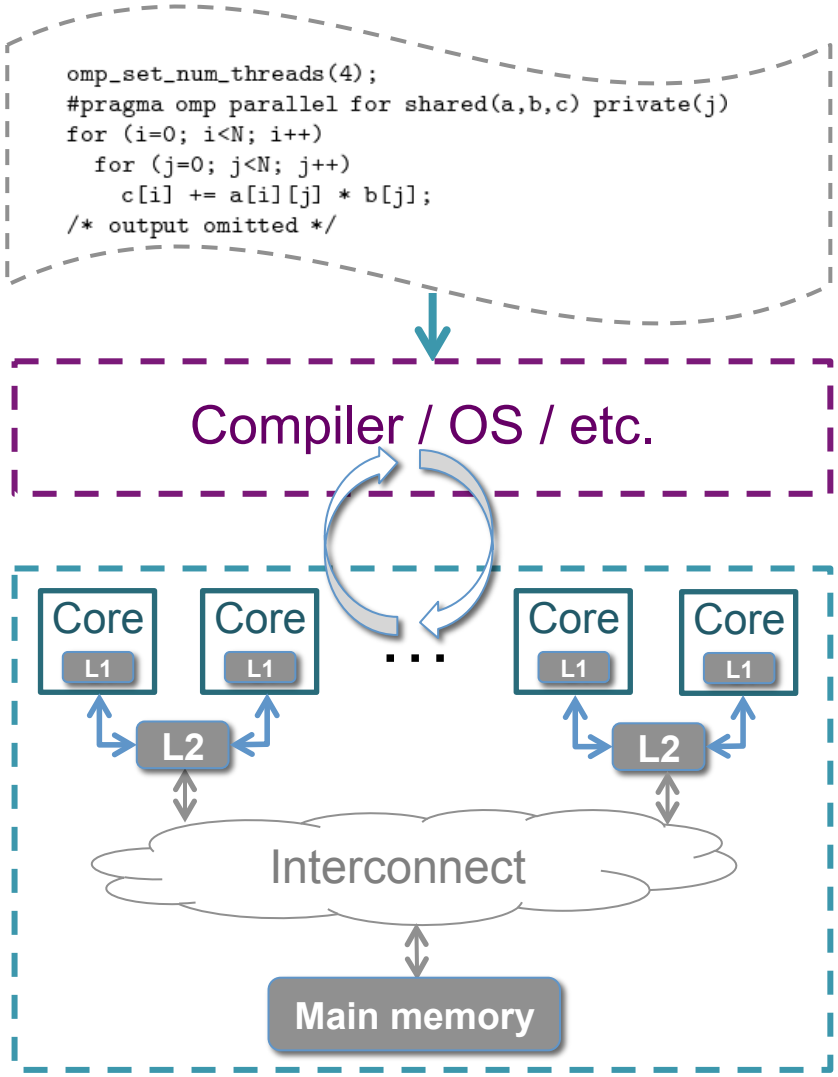
PROJET FINANCÉ PAR L'ANR
PROJECT FUNDED BY THE ANR

System design: motivations

```
omp_set_num_threads(4);
#pragma omp parallel for shared(a,b,c) private(j)
for (i=0; i<N; i++)
  for (j=0; j<N; j++)
    c[i] += a[i][j] * b[j];
/* output omitted */
```

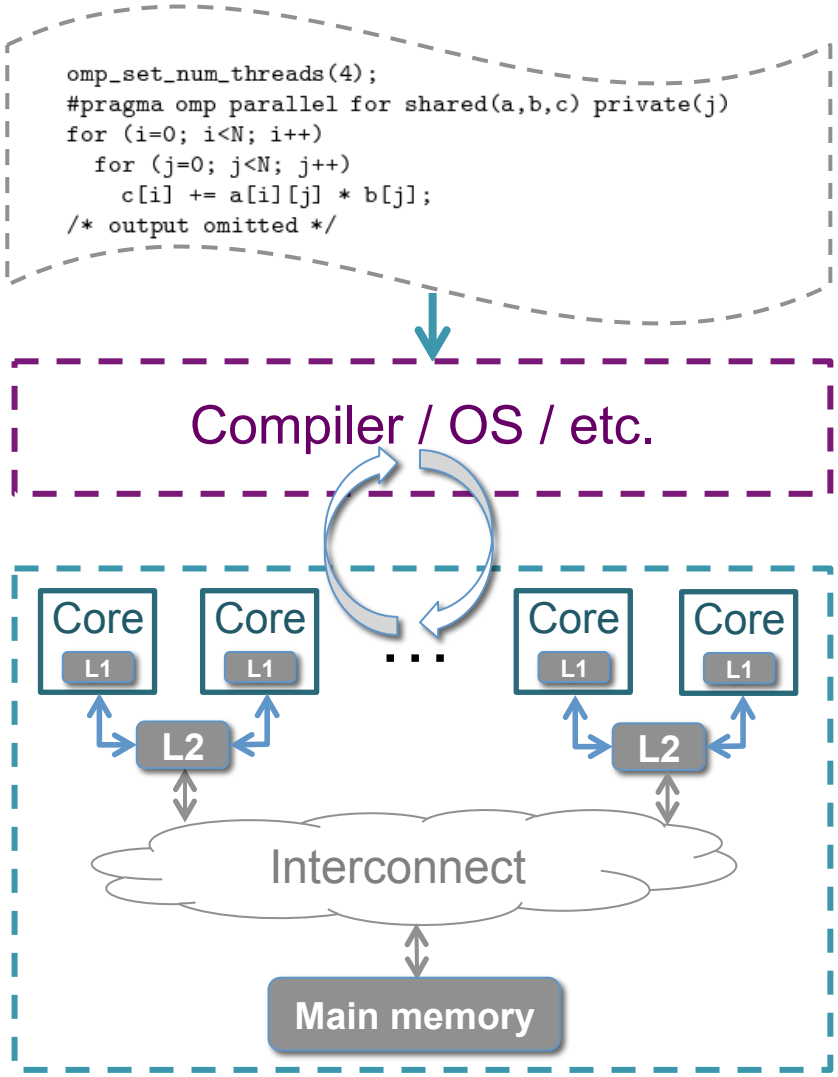


Which task and data allocation?

Which multicore architectures?

Which memory & com. Technology?

System design: requirements



Effective and accurate-enough design assessment

- ✓ Performance
- ✓ Area
- ✓ Power consumption
- ✓ Energy consumption

MAGPIE

Manycore **A**rchitecture ener**G**y and **P**erformance evaluat**I**on **E**nvironment

MAGPIE: buiding blocks

http://www.lirmm.fr/continuum-project/pages/magpie.html

- **gem5***: quasi-cycle accurate simulator
  - IPs: cores (x86, ARM…), memory, interconnect…
  - can boot a complete linux OS
  - detailed microarchitecture details / statistics

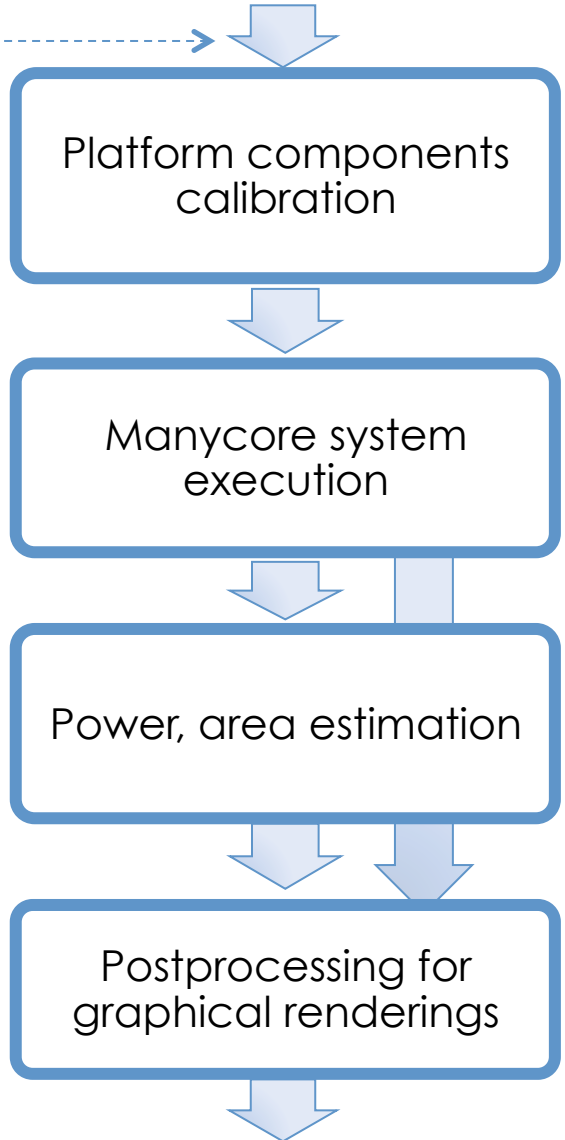
- **McPAT****: area, power and timing modeling for CMOS, SOI technologies

- **NVSim*****: area, power and energy estimator for non-volatile memory technologies

* http://www.gem5.org
** ww.hpl.hp.com/research/**mcpat**
*** http://nvsim.org

MAGPIE: script-based flow

- Sw: workloads, OS
- Hw: cores / Interconnect / memory parameters…



- **Automation scripts: make user life easy!**
  - No tedious and error-prone manual statistics manipulation
  - Significant time and effort saving

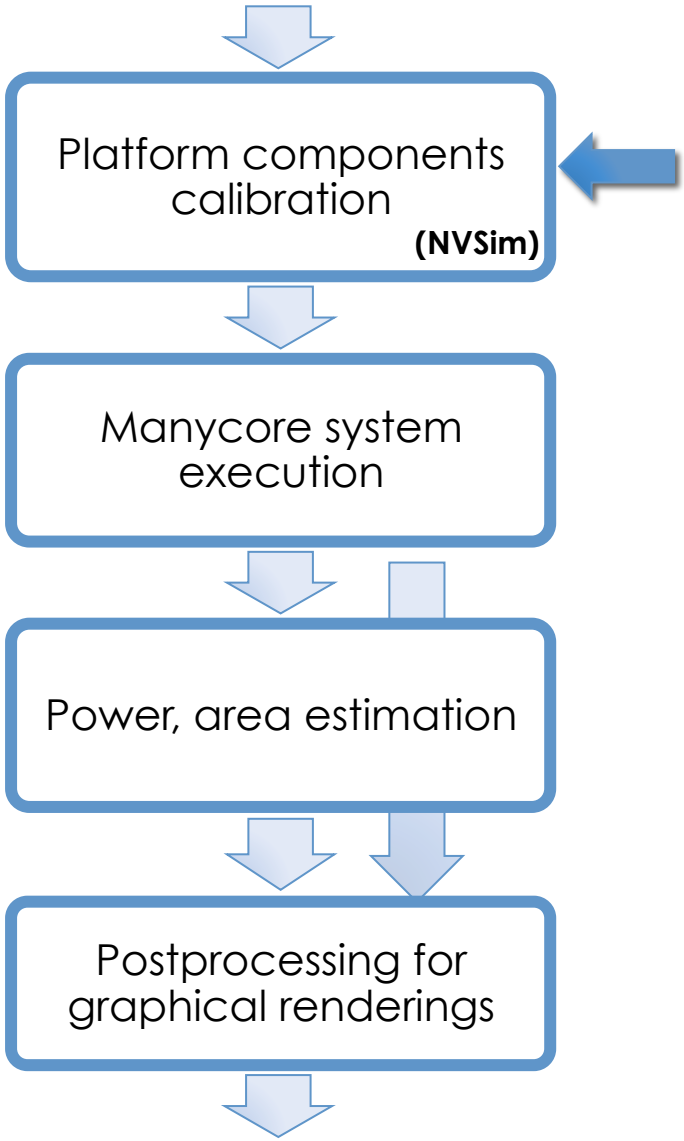
MAGPIE: design and evaluation

==========
CACHE DESIGN -- SUMMARY
==========
[...]

Area:
- Total Area = 0.091mm^2
[…]

Timing:
- Cache Hit Latency = 0.660ns
- Cache Write Latency = 0.478ns
- Tag Hit Latency = 418.135ps
- Data Row Activation Latency = 478.125ps
- Data Column Decoder Latency = 181.817ps
[…]

Power:
- Cache Hit Dynamic Energy = 0.023nJ per access
- Cache Write Dynamic Energy = 0.006nJ per access
- Cache Total Leakage Power = 44.765mW
[…]



MAGPIE: design and evaluation

---------- Begin Simulation Statistics ----------

sim_seconds	**0.185494**
sim_ticks	185493718000
host_seconds	226.05
sim_insts	**317057589**
sim_ops	350391966

[…]

system.cpu.dcache.ReadReq_misses::total	9907
system.cpu.dcache.WriteReq_hits::total	30242918
system.cpu.dcache.WriteReq_misses::total	11338

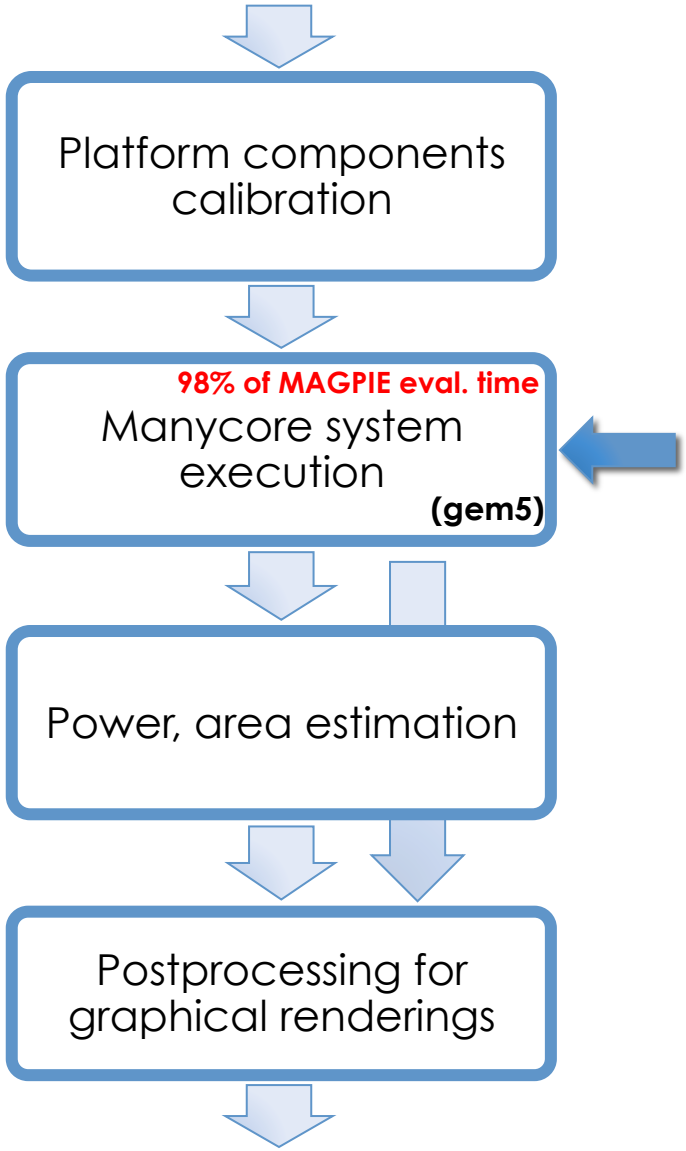
[…]

system.iobus.trans_dist::ReadReq	30
system.iobus.trans_dist::WriteReq	186

[…]

system.mem_ctrls.num_reads::total	83418
system.mem_ctrls.num_writes::total	13287

[…]

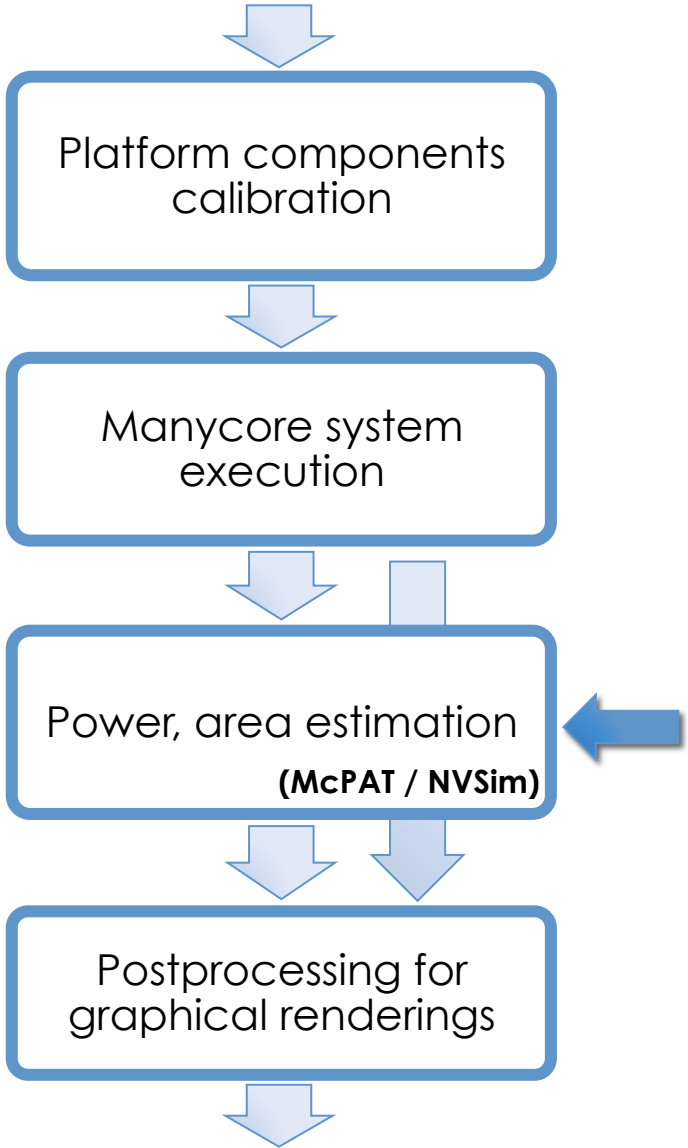


MAGPIE: design and evaluation

Core:
Area = 7.27488 mm^2
Peak Dynamic = 1.11806 W
Gate Leakage = 0.0965526 W
Runtime Dynamic = 0.0710242 W
[…]

Bus:
Area = 0.014895 mm^2
Peak Dynamic = 0.461444 W
Gate Leakage = 0.000981421 W
Runtime Dynamic = 9.23907e-05 W
[…]

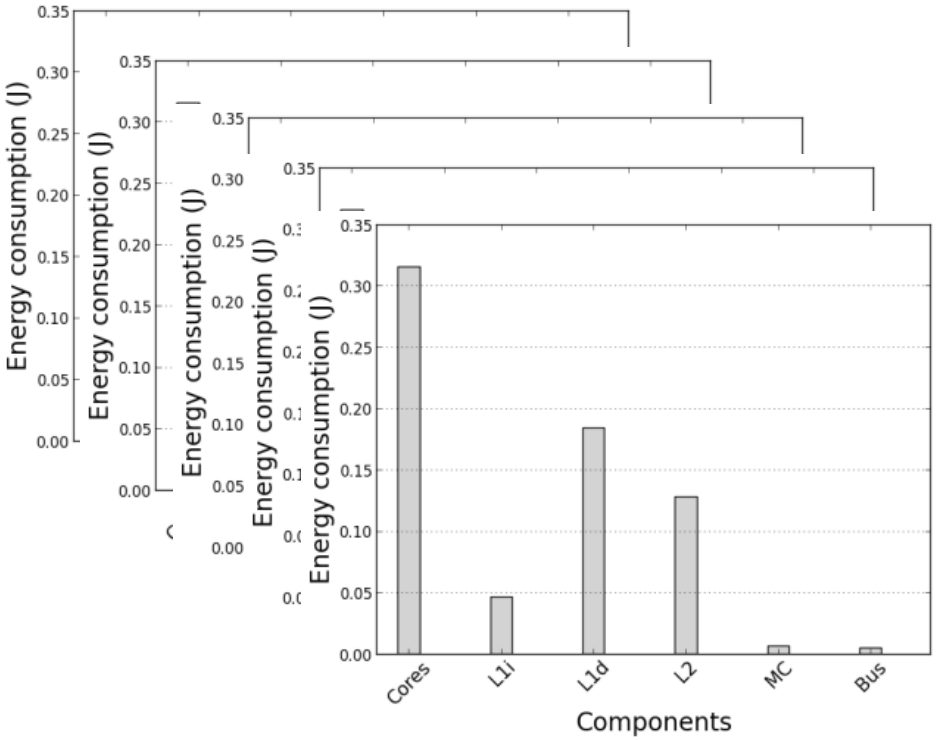
Memory Controller:
Area = 2.76641 mm^2
Peak Dynamic = 0.419928 W
Gate Leakage = 0.00964467 W
Runtime Dynamic = 0.0426932 W
[…]

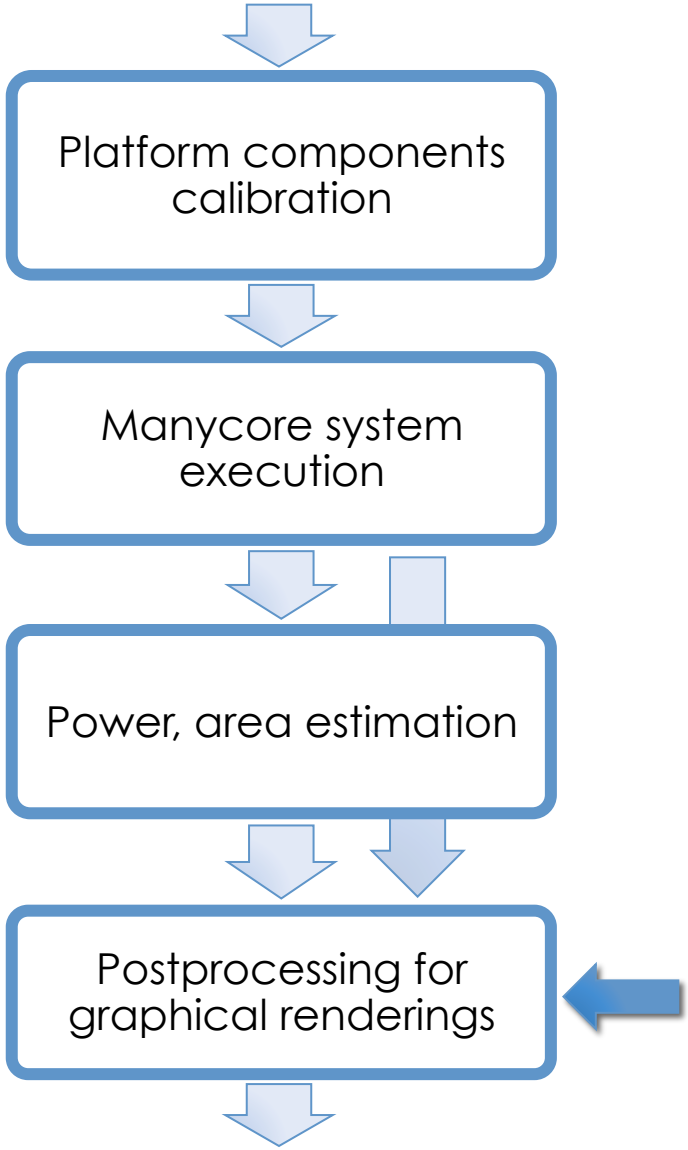


MAGPIE: design and evaluation

CSV output stat files

+





EXAMPLE

Evaluation of NVM in big.LITTLE architecture

Emerging memory technologies

- Magnetic Memories: STT-RAM…
  - Non volatility, high density, good endurance…
  - **Low static power**

	SRAM	DRAM	Flash (NOR)	Flash (NAND)	FeRAM	MRAM	PRAM	RRAM	STT-RAM
Non-volatile	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Cell size (F^2)	50–120	6–10	10	5	15–34	16–40	6–12	6–10	6–20
Read time (ns)	1–100	30	10	50	20–80	3–20	20–50	10–50	2–20
Write / Erase time (ns)	1–100	15	1 µs / 10 ms	1 ms / 0.1 ms	50 / 50	3–20	60 / 120	10–50	2–20
Endurance	10^{16}	10^{16}	10^5	10^5	10^{12}	$>10^{15}$	10^8	10^8	$>10^{15}$
Write power	Low	Low	Very high	Very high	Low	High	High	Low	Low
Other power consumption	Current leakage	Refresh current	None	None	None	None	None	None	None
High voltage required	No	3 V	6–8 V	16–20 V	2–3 V	3 V	1.5–3 V	1.5–3 V	<1.5 V

How to allocate tasks and data?

Which multicore architecture?

Which underlying technologies?

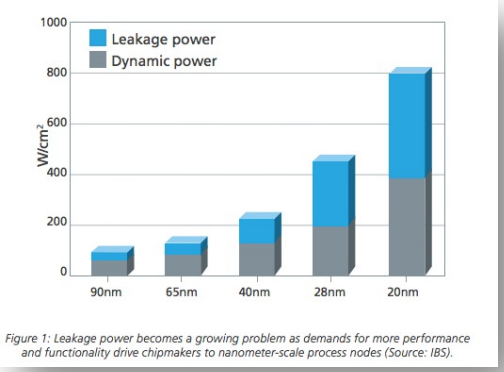
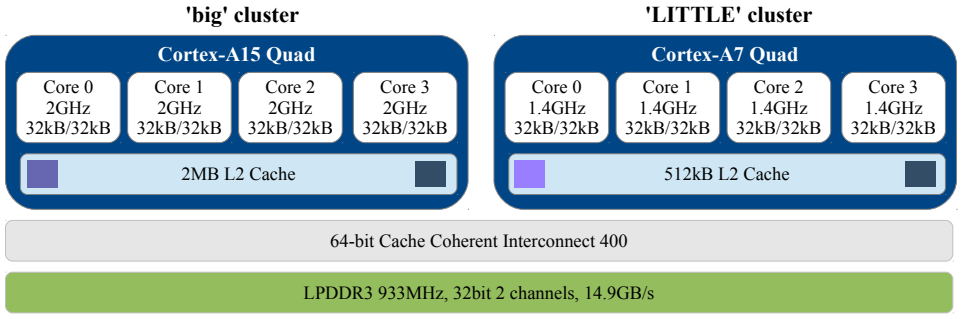
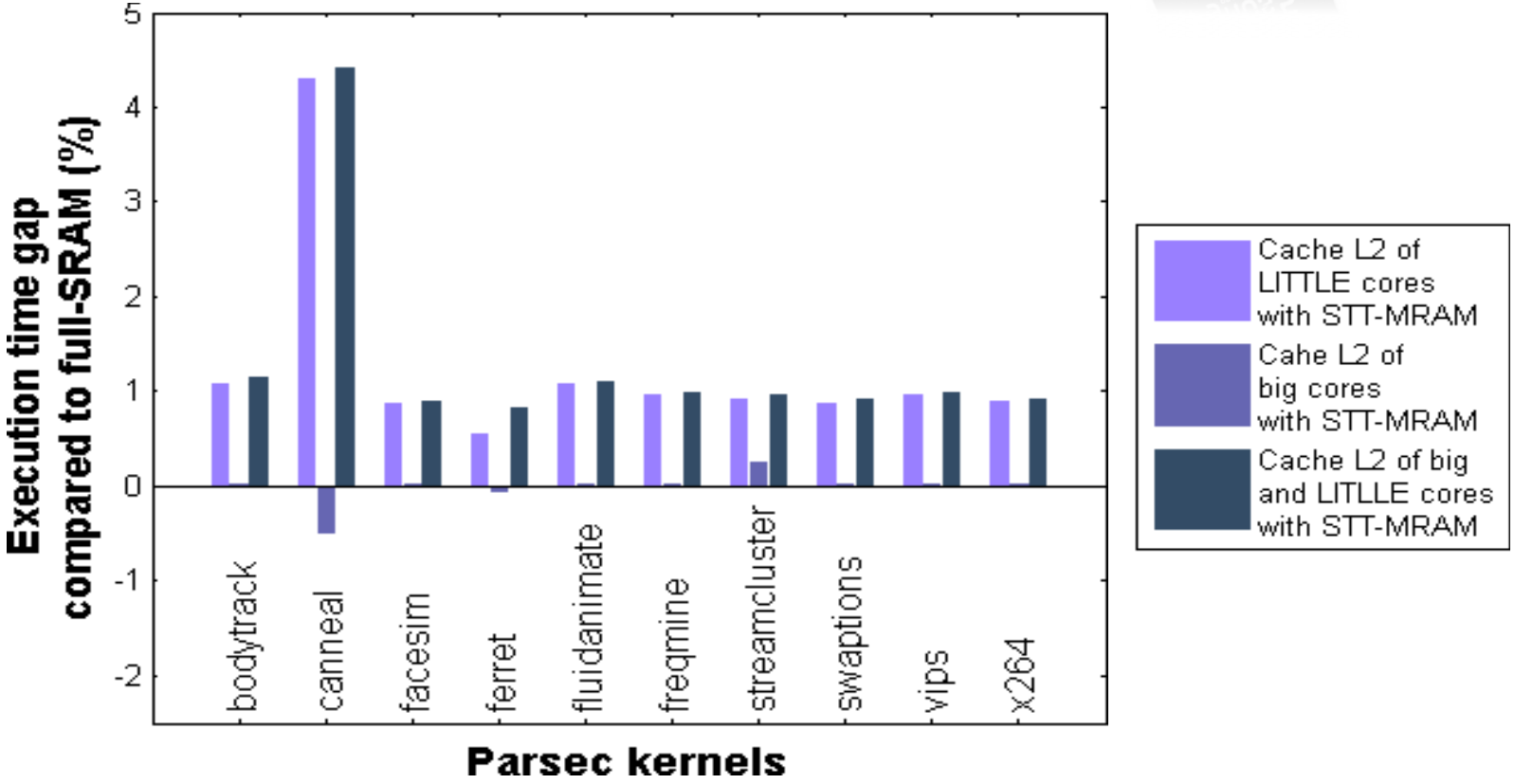


Figure 1: Leakage power becomes a growing problem as demands for more performance and functionality drive chipmakers to nanometer-scale process nodes (Source: IBS).

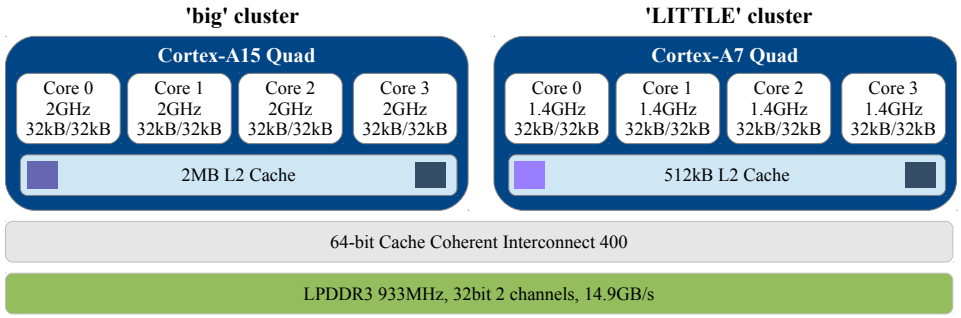
http://www.flashmemorysummit.com/English/Collaterals/Proceedings/2009/20090813_ThursPlenary_Tabrizi.pdf

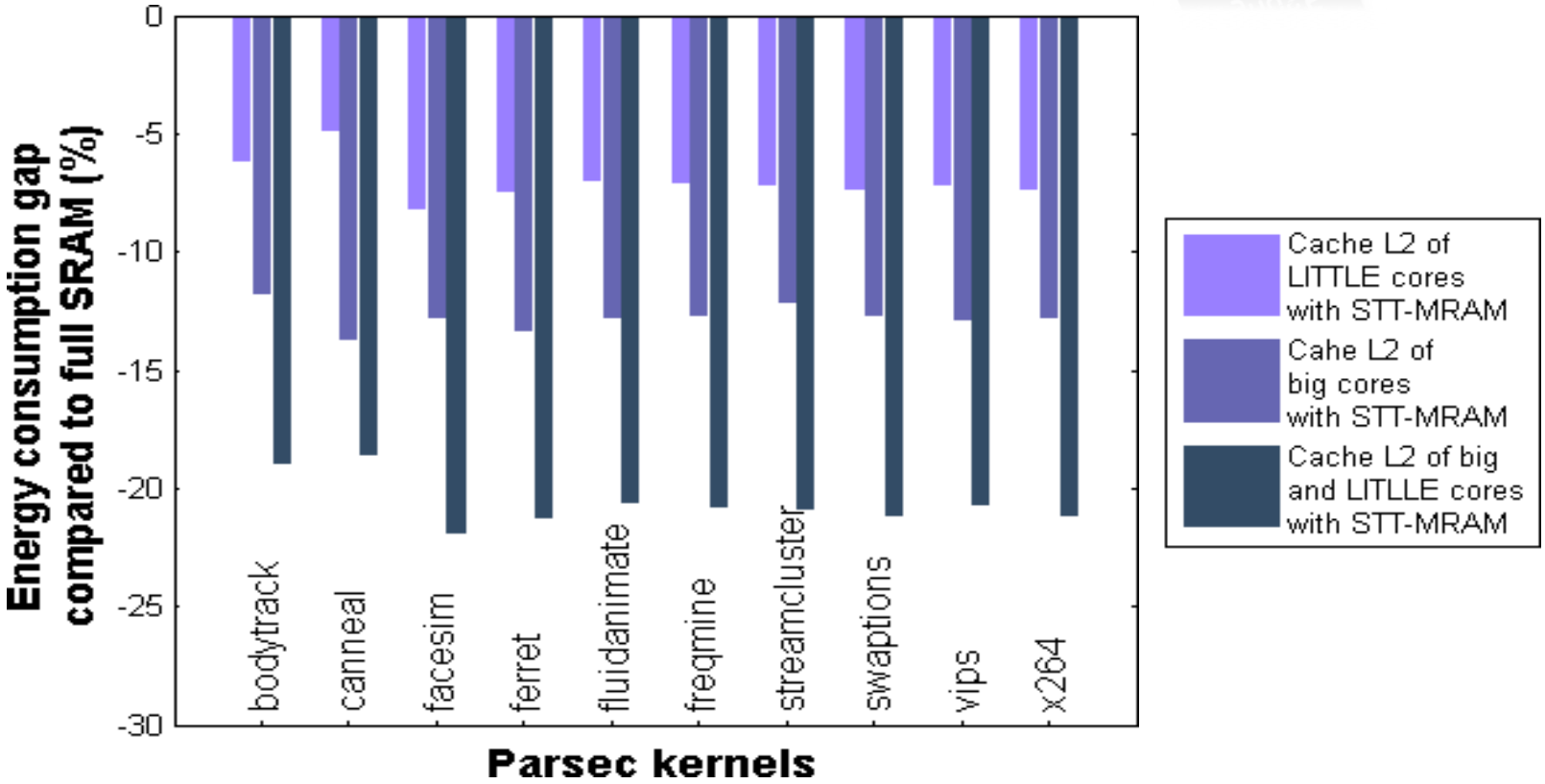
Magnetic memory: MRAM vs. SRAM



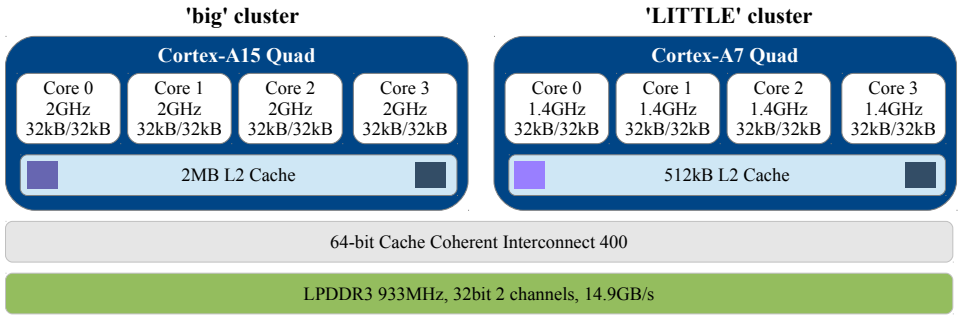


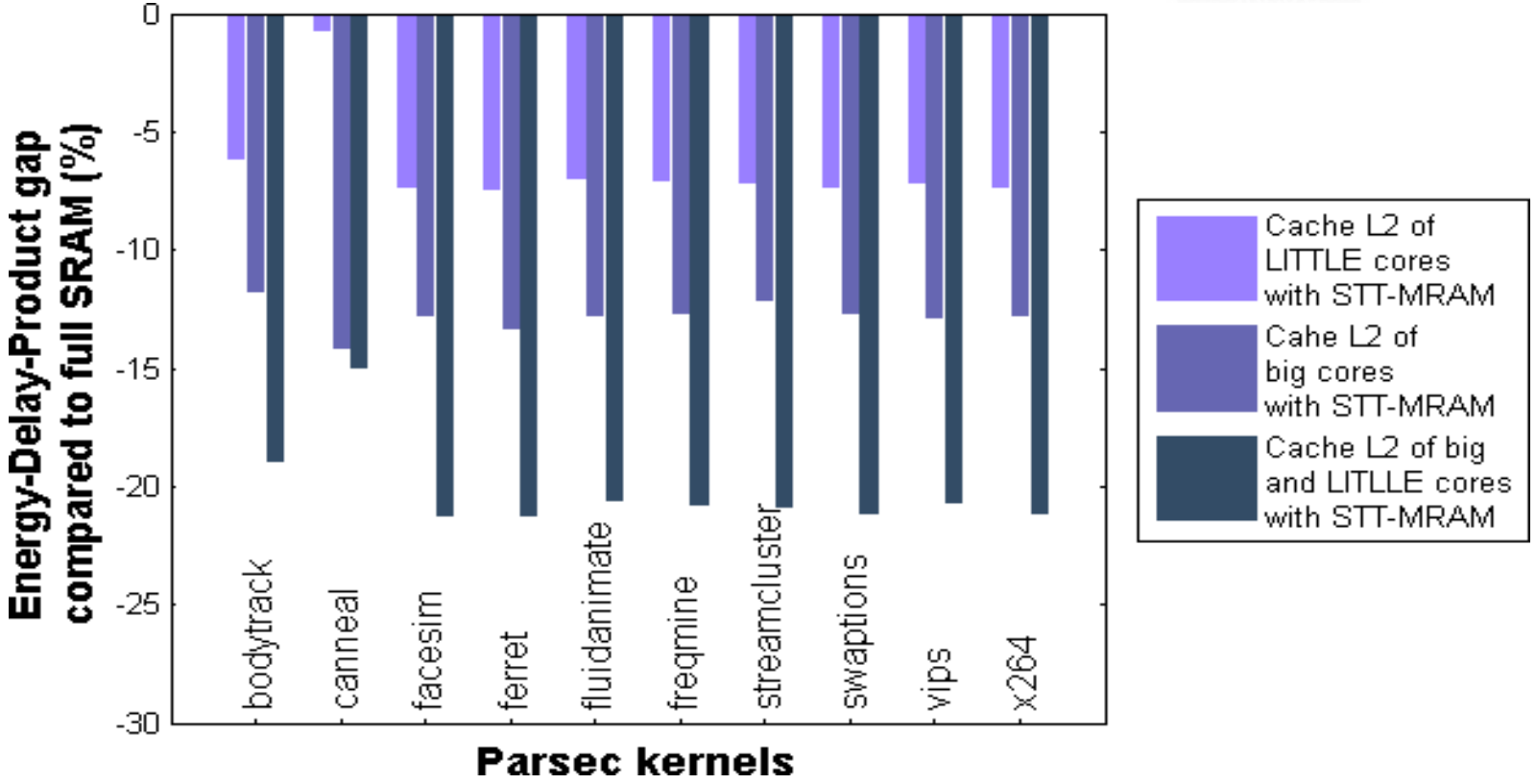
Magnetic memory: MRAM vs. SRAM





Magnetic memory: MRAM vs. SRAM





THIS TUTORIAL

Agenda

Agenda

- First steps with gem5
- Configuration and usage
- Application to real workload
- Closing notes