IEEE 16th International Conference on
Design & Technology of Integrated System in Nanoscale Era
June 28th - 30th, 2021, Apulia - Italy (Virtually)
https://www.lirmm.fr/dtis2021

CALL FOR PARTICIPATION

Scope

The aim of the conference is to cope with technology scaling limits and the emergence of novel paradigms. The areas of interest include the design, test and technology of electronic products, ranging from integrated circuit modules and printed circuit boards to full systems and microsystems, as well as the methodologies and tools used in the design, verification and validation of such products.

Integrated Systems Design:

- SOC, SIP design
- Multiprocessor systems
- Embedded systems
- Wireless systems
- Network on Chip
- Analog, Mixed Signal, RF systems
- MEMS and MOEMS systems
- Low Voltage, Low Power systems
- Innovative technologies
- Synthesis (physical, logic)
- Verification
- 3D integration
- Hardware Security

Integrated Systems Technology:

- Emerging resistive memories
- Device Modeling
- Material Characterization
- Failure Analysis
- New Components
- Packaging
- Process Technology
- Reliability Issues
- 3D Integration

Integrated Systems Testing:

- Defect and Fault Modeling
- Testing
- MEMS/MOEMS Testing
- SOC and SIP Testing
- Delay Testing
- Memory Testing
- Fault Simulation, ATPG
- DFT, BIST, BISR
- On-line Testing
- Fault Tolerant Systems
- ATE Issues
- Alternative Test Strategies
- 3D Testing
- Test and Security Issues

Conference Registration

Standard Registration Process (with payment):

Each accepted paper shall be accompanied by at least one full conference registration at the speaker rate (i.e., two speaker registrations are needed for two accepted papers, e.g. from the main author or a co-author of the paper) : https://www.lirmm.fr/dtis2021/registration.html

Student Registration Process (free fare):

The student attendees that do not participate to the conference as speakers may register at the following link: https://forms.gle/dGoBmCTgpEvmPWTe9

Conference Program

DTIS 2021 starts on Monday, June 28th and offers a three-day technical program which includes 6 Regular Paper Sessions, 2 Special Sessions, 3 Keynotes and 2 Embedded Tutorials.
The Keynotes address the following topics: Reliable Robotics in Academia and Industry, Memory-Centric Artificial Intelligence and the use of COTS within European Space Agency programs. Embedded tutorials focus on Side-Channel Attacks and RISC-V design and test. **This year, DTIS 2021 is organized in conjunction with IOLTS 2021** (https://orion.polito.it/iolts/). Regular sessions, special sessions and embedded tutorials are held in parallel. Keynotes are shared between the two conferences.

Program available here: https://www.lirmm.fr/dtis2021/program.html

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