CALL FOR PAPERS

Design and Test of Integrated Systems

Elsevier Microelectronics Reliability

Special Issue

Journal of Microelectronics Reliability seeks original manuscripts for a Special Issue on **Design & Test of Integrated Systems** scheduled to appear in July 2022.

The development of highly reliable and secure emerging devices and architectures offer key advantages for research in the fields where the increasing demand for massive storage and high computation speed at low-power consumption require substantial research efforts. Moreover, the predictions are that, in the near future, novel technologies and dedicated designs will be introduced in the fields of automotive and healthcare, where the pressing challenge is the need of high security and quality requirements targeting 0 defective parts per million (ppm). In addition, advanced computing systems built with novel or advanced technologies bring the benefit of increased computational capability that will offer users better services and more diverse functionalities. In this context, this special issue is focused on test and reliability in design and technology of electronic products, ranging from integrated circuits modules and printed circuit boards to full systems and microsystems, as well as methodologies and tools used in the design verification and validation process.

Integrated Systems Design:

- SOC, SIP design
- Multiprocessor systems
- Embedded systems
- Wireless systems
- Network on Chip
- Analog, Mixed Signal, RF systems
- MEMS and MOEMS systems
- Low Voltage, Low Power systems
- Innovative technologies
- Synthesis (physical, logic)
- Simulation, Validation, Verification
- 3D integration
- Hardware Security

Integrated Systems Technology:

- Emerging resistive memories
- Device Modeling
- Material Characterization
- Failure Analysis
- New Components
- Packaging
- Process Technology
- Reliability Issues
- 3D Integration

Integrated Systems Testing:

- Defect and Fault Modeling
- Analog and Mixed Signal Testing
- MEMS/MOEMS Testing
- SOC and SIP Testing
- Delay Testing
- Memory Testing
- Fault Simulation, ATPG
- DFT, BIST, BISR
- On-line Testing
- Fault Tolerant Systems
- ATE Issues
- Alternative Test Strategies
- 3D Testing
- Test and Security Issues

Submitted articles must not have been previously published or currently submitted for journal publication elsewhere.

As an author, you are responsible for understanding and adhering to our submission guidelines.

Please submit your paper to Elsevier Microelectronics Reliability at
https://www.journals.elsevier.com/microelectronics-reliability.
Please select **SI_DTIS** when you reach the “Article Type” step in the submission process.

Please note the following important dates.

Submission Deadline: **December 15, 2021**
Notification of Final Acceptance: **June 15, 2021**
Publication date: **July 2022**

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