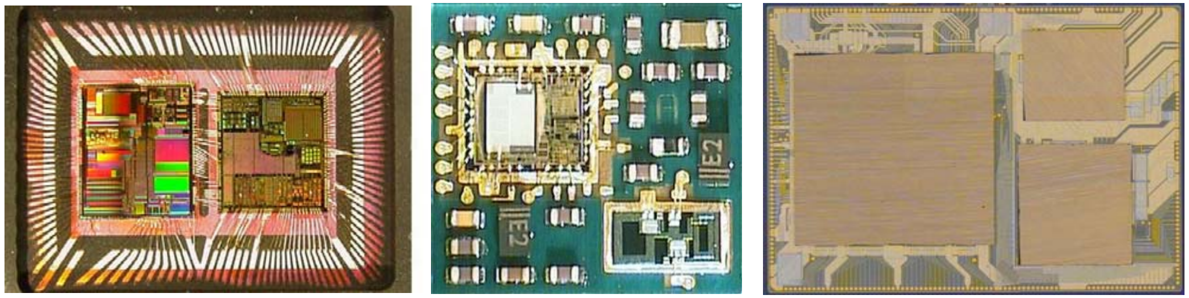
SiP Technology and Testing

Name: Philippe Cauvet
Date: 2007, March 28

Outline

- Definition
  - Market / Applications
    - Design and technology
    - Packaging Technologies
  - Test Challenges
- Conclusion

What is a SiP?



System-in-package (SiP) = any combination of semiconductors, passives, and interconnects integrated into a single package

SiP (System-in-Package) is a functional system or subsystem assembled into a single package

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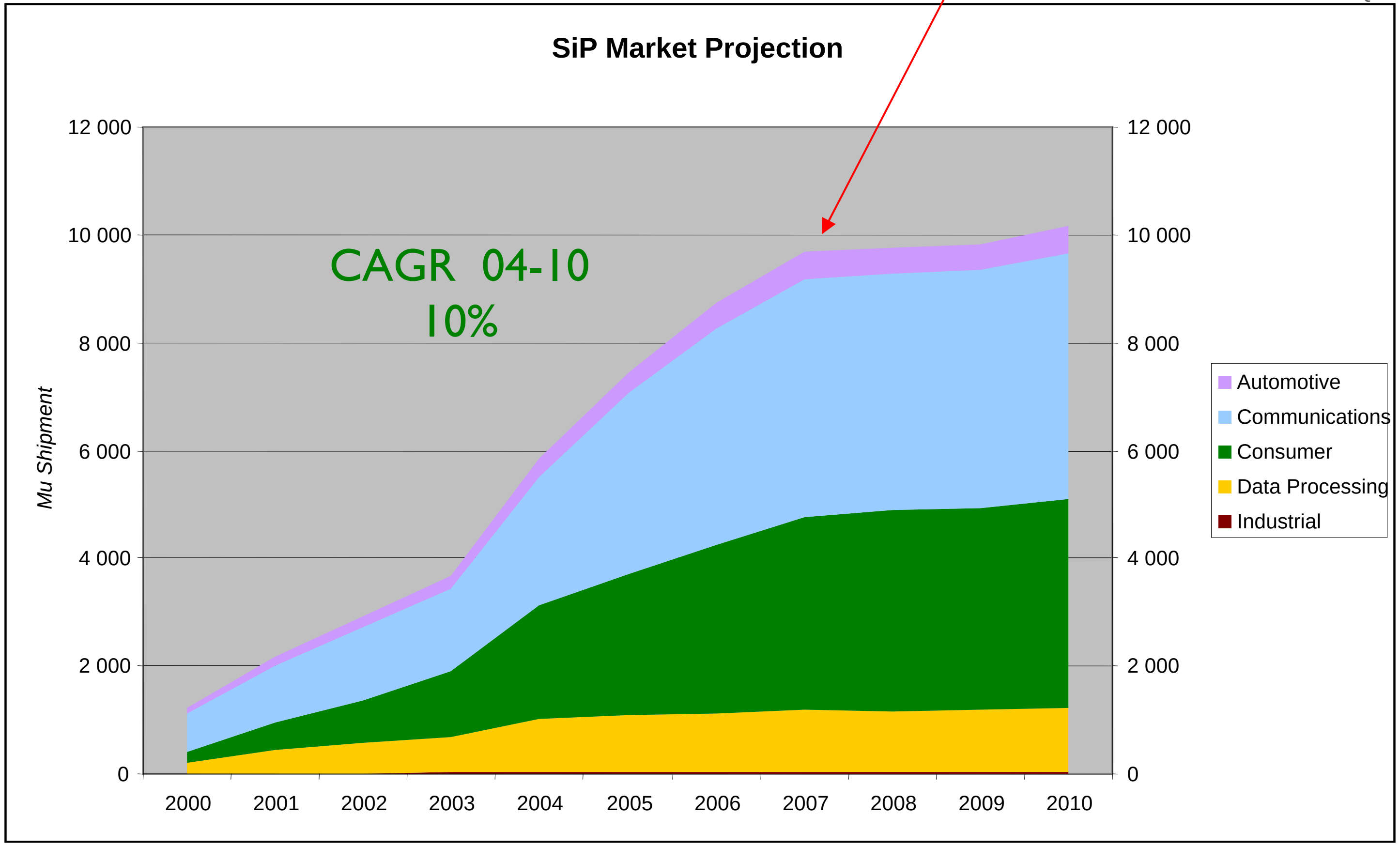
Market Trends

Industry moves to SiP

Why a slowdown ?
Missing CAD tools certainly an obstacle

Source: Gartner 1Q06



- Gartner updates every quarter its SiP Market Projection
- Gartner view slightly increased since 3Q04 with 10% CAGR 04-09 compared to 5% CAGR 04-09 for Semiconductors: **SiP and SoC grow in parallel!**
- Gartner sees as much SiP in Consumer as Communication

Applications

Leading Applications for SiPs

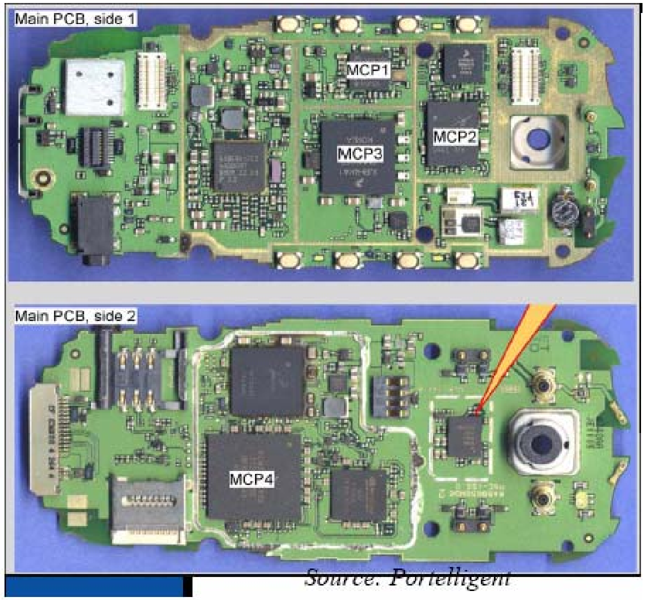
- **Applications include portable consumer products such as *digital camcorders and cameras***
- ***Mobile phone* is the volume driver**
  - **Logic and memory combo**
  - **Digital baseband section**
  - **Transceiver section**
  - **RF section**

Applications: DSC

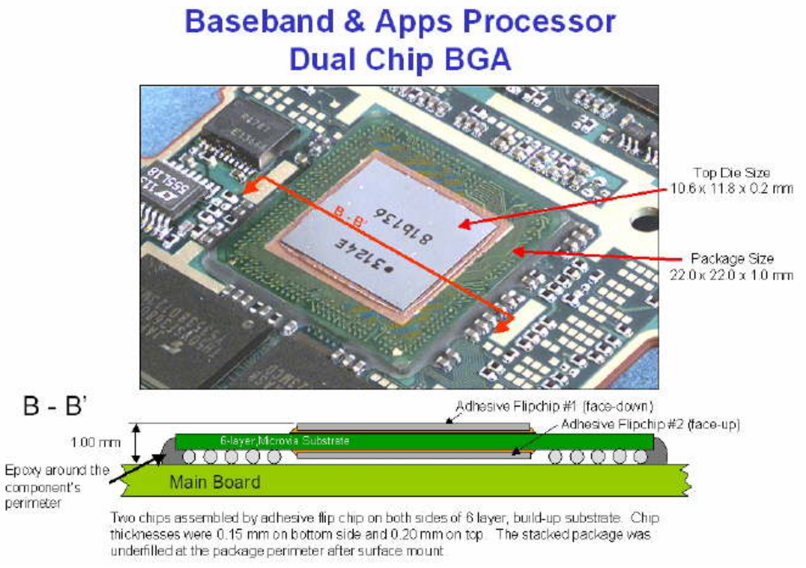
SiPs show up in portable devices

- The Sony DCS-T1, a 5MPixel camera, has the height and width of that of a credit card.

Applications: Mobile phones



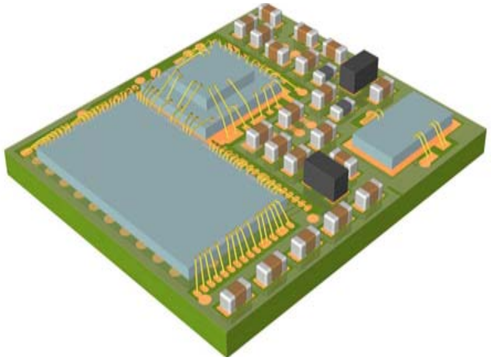
Source: Portelligent

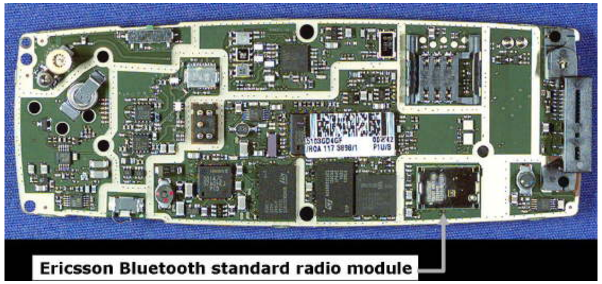


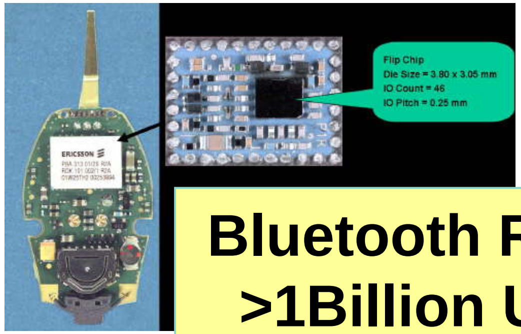
Baseband & Apps Processor
Dual Chip BGA

Two chips assembled by adhesive flip chip on both sides of 6 layer, build-up substrate. Chip thicknesses were 0.15 mm on bottom side and 0.20 mm on top. The stacked package was underfilled at the package perimeter after surface mount.

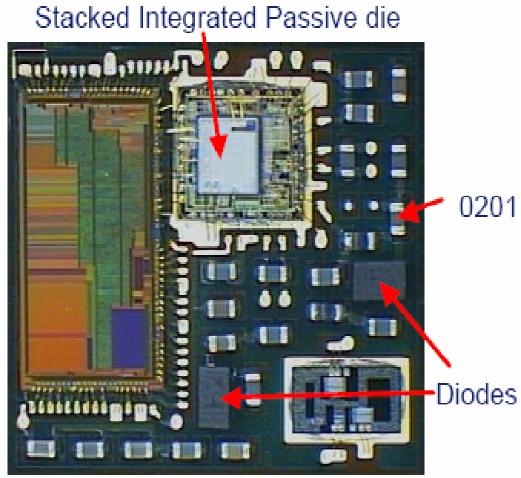
Applications: Bluetooth™

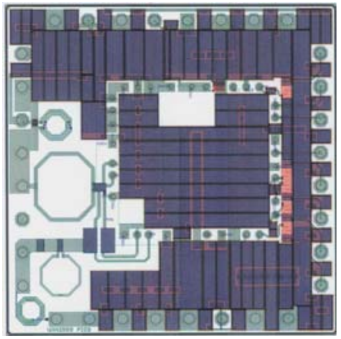


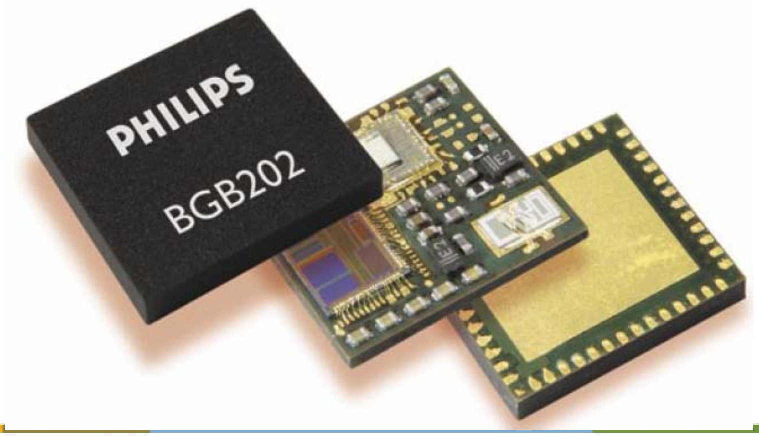




Bluetooth Radio: >1Billion Units shipped in 2006

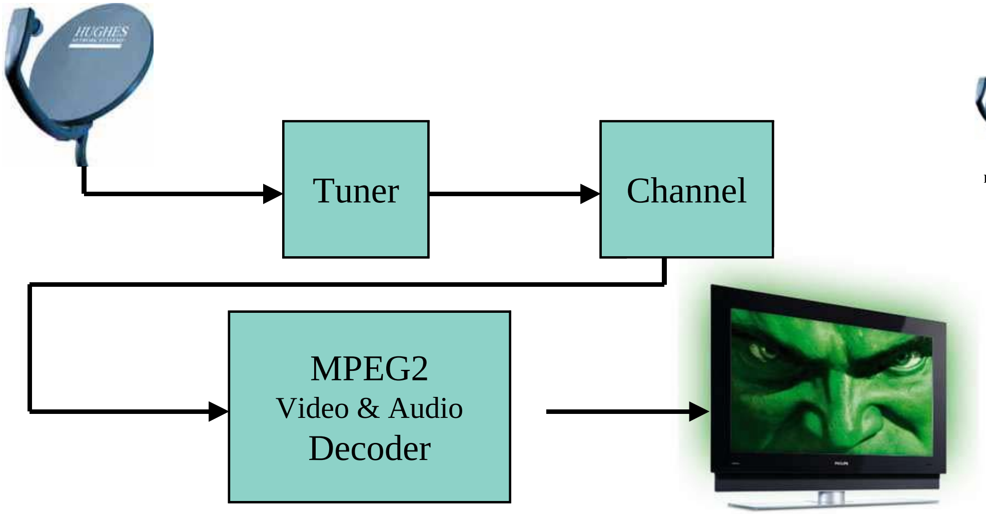


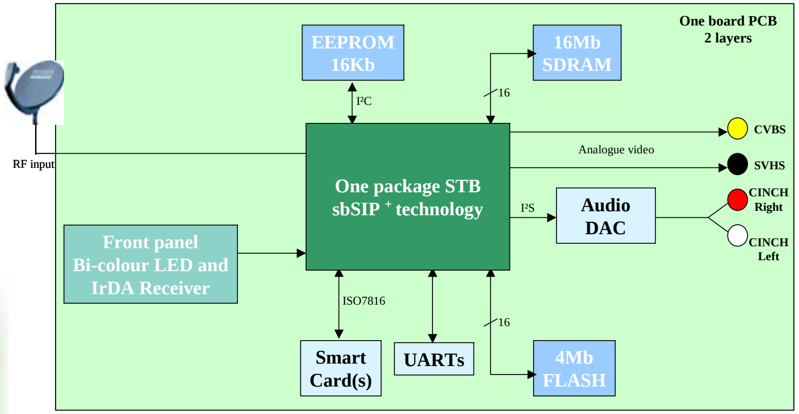


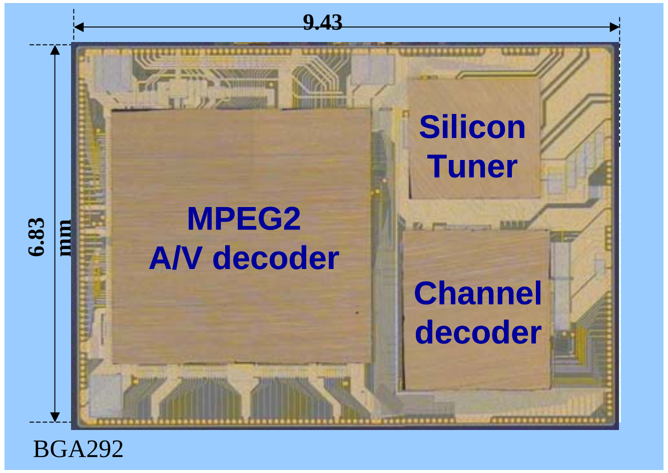


Laminate-based module
7.0mm x 8.0mm, Lamp2

Applications: OneChipSTB







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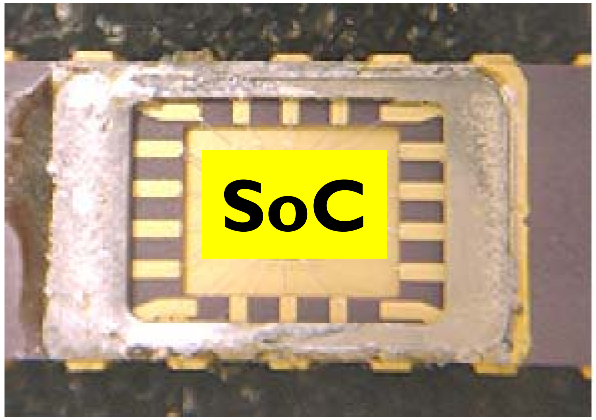
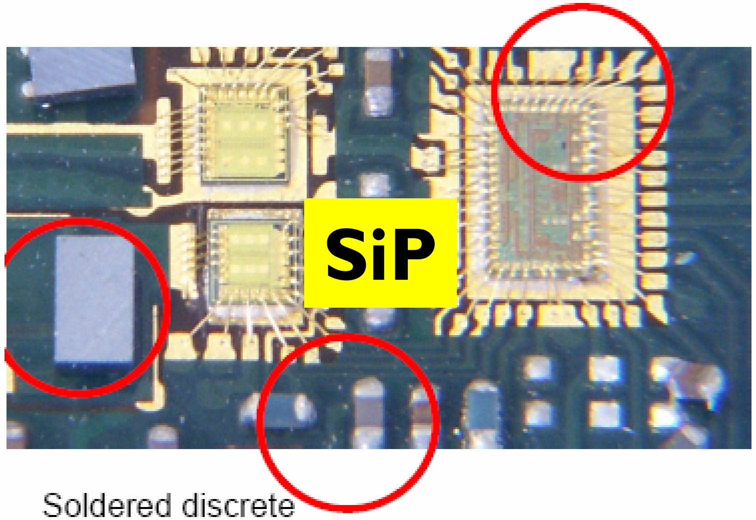
SiP vs SoC (1)



Single piece of silicon
Single technology
Single level of interconnection

Multiple chips
Multiple technologies
Multiple levels of interconnection…
…and 3D

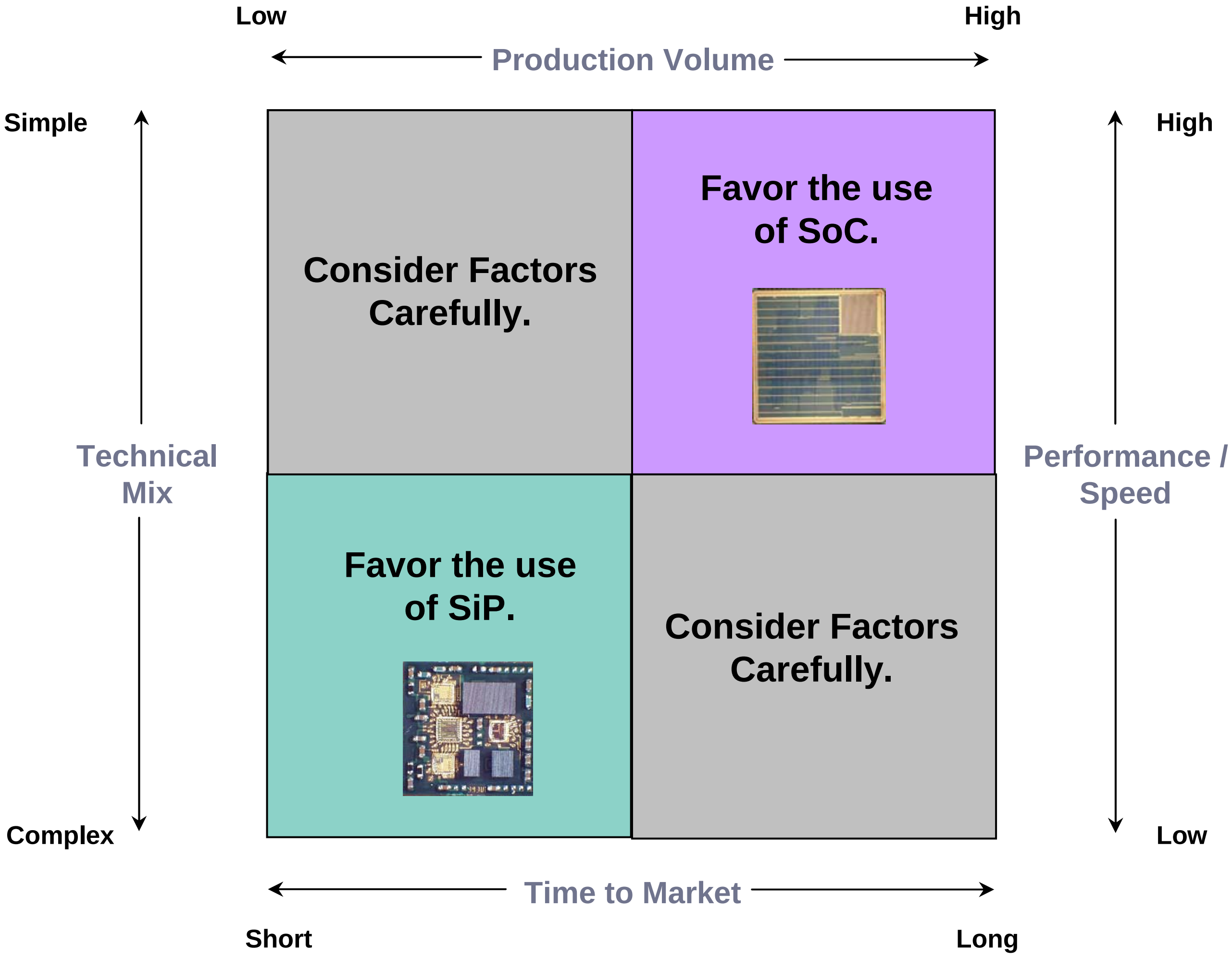


Passive filter
In Silicon
With
Flip chip
connections

BICMOS die
with
Bond wire
connections

Soldered discrete
passive devices

SiP vs SoC (2)



Factors to Consider:

- Production Volume
- Design Environment
- Dev Cost (Incl. IP Cost)
- Reliability
- Die Maturity
- Technologies (RF, Memories…)

\+

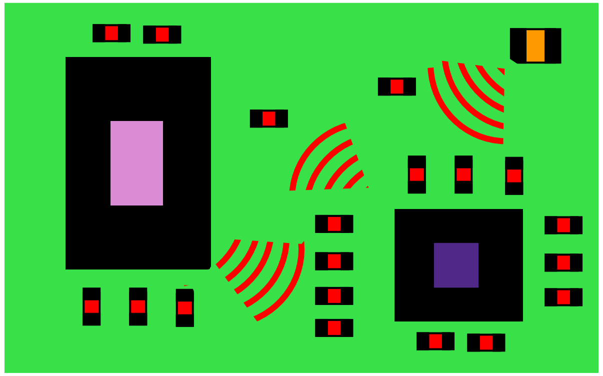
Market Environment

Source: Gartner 2006
Contibutor: JM Yannou, NXP SiP Innovation Manager

Focus on EMC (and SiP): new challenges

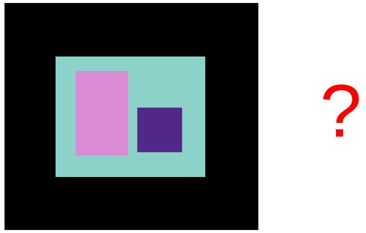
non SiP system

Components placement is done empirically ***after*** circuits design

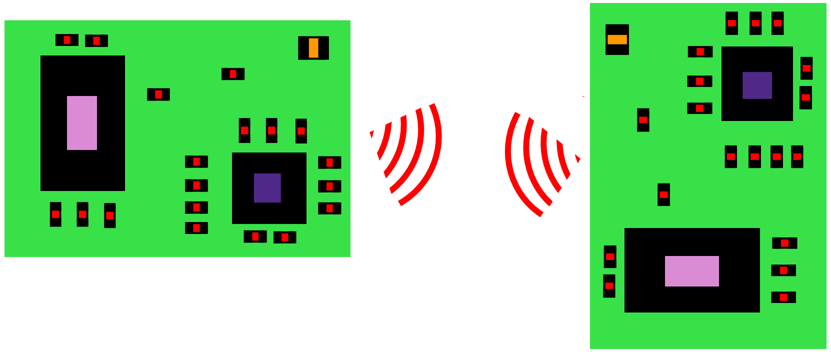


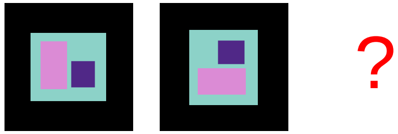
SiP

Components placement is done at the ***same time as*** circuits design: predictability needed!



system goes 3D! + components are closer to each other!





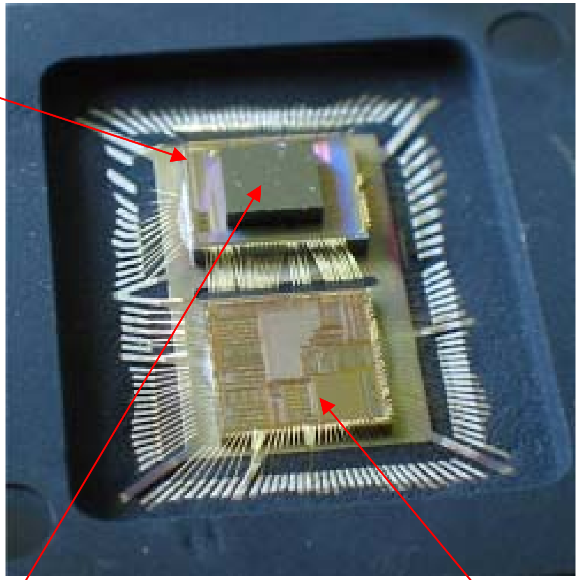
Example of an inter-system (inter SiP in susceptibility) EMC challenge

TV:
up to 862MHz

GSM:
from 890MHz on

The GSM antenna emits signals considered as noise by the close-by low-amplitude large-bandwidth TV RF receiving subsystem

Digital IC



Decoupling capacitors integrated in silicon (Philips PICS technology), flip-chip bumped on digital: -16dB noise reduction measured!

Analog IC

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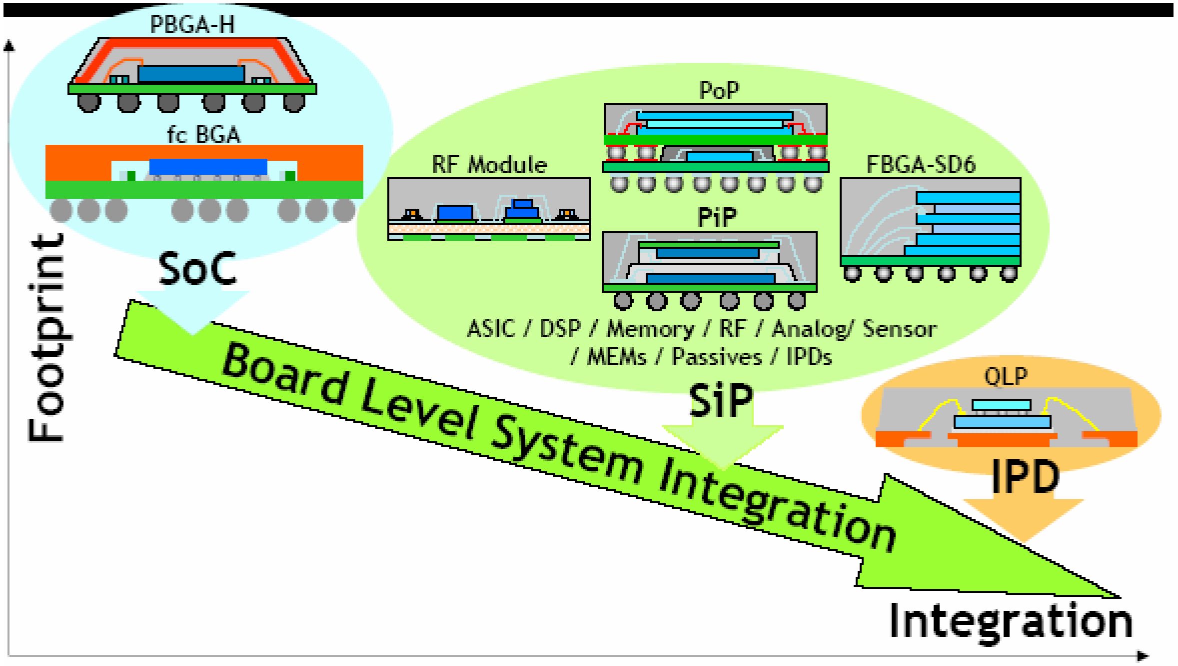
SiP vs SoC

SoC: System on Chip

SiP: System in Package

IPD: Integrated Passive Devices

Functional Integration Trend

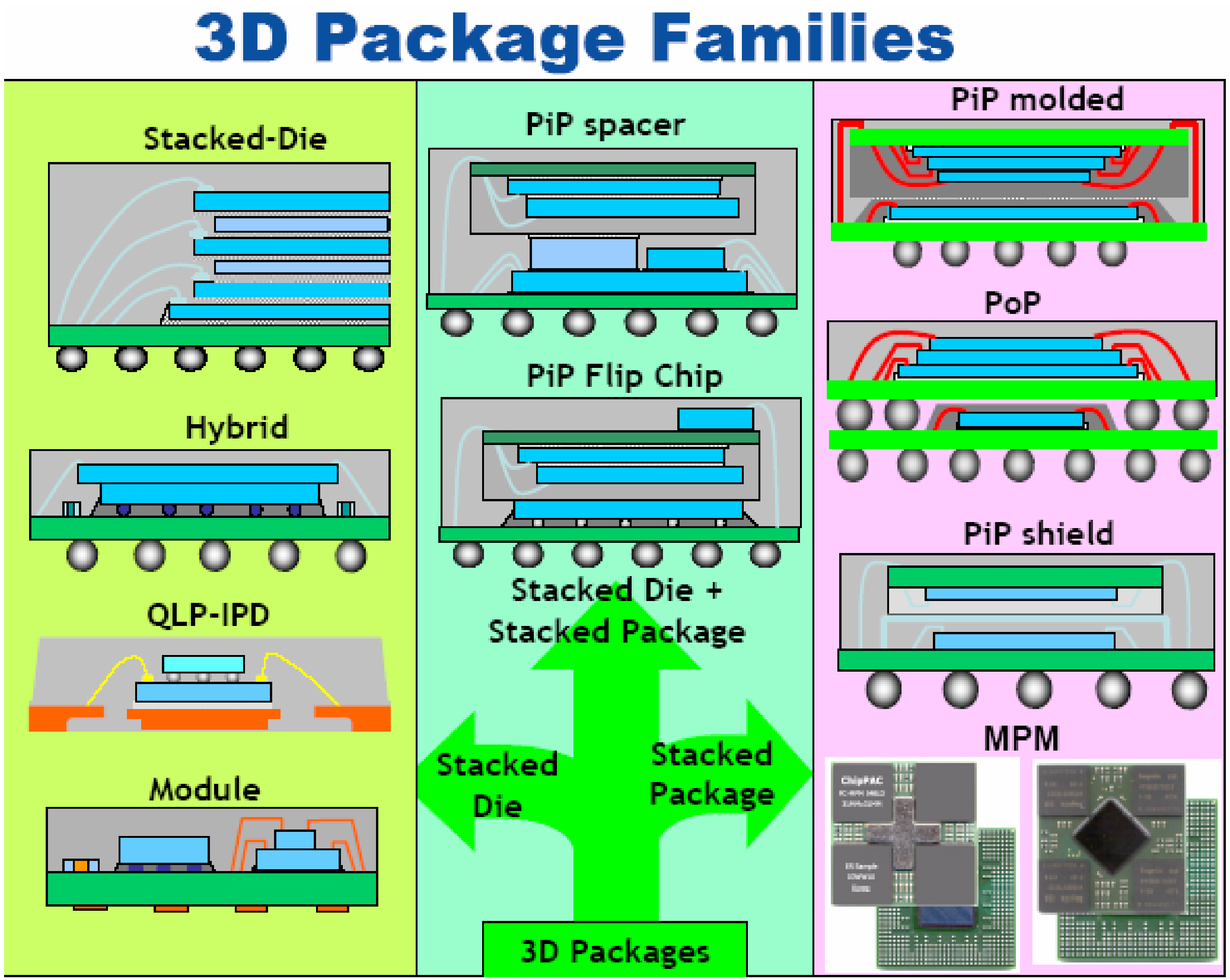


Functional integration in SoC, SiP and IPD enable product miniaturization

Packaging challenges

- **Higher integration requires smaller chips, with smaller *pad* pitch and size**
- **More chips = *thinner* chips (how to handle <100µm wafers?)**
- **More functionalities = more *power***
- ***Cost* of materials**

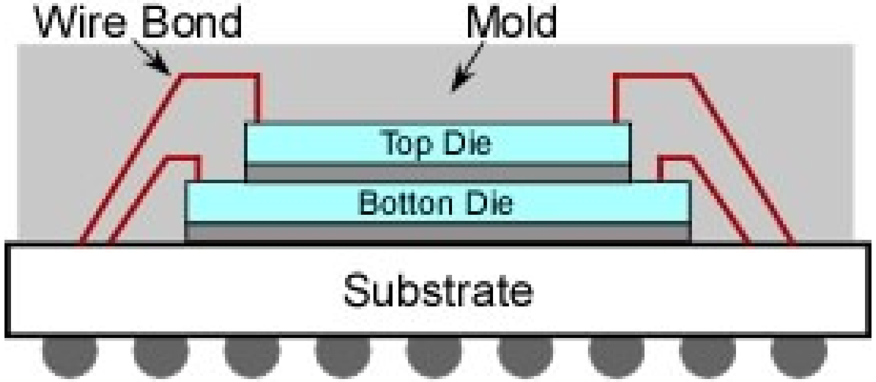
Packaging



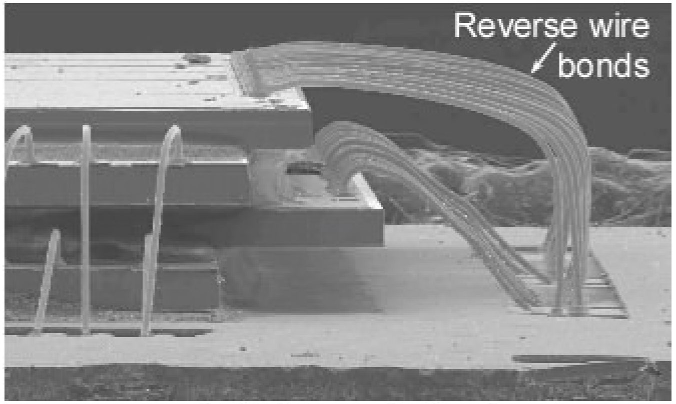
Source: STATSChippac

Packaging

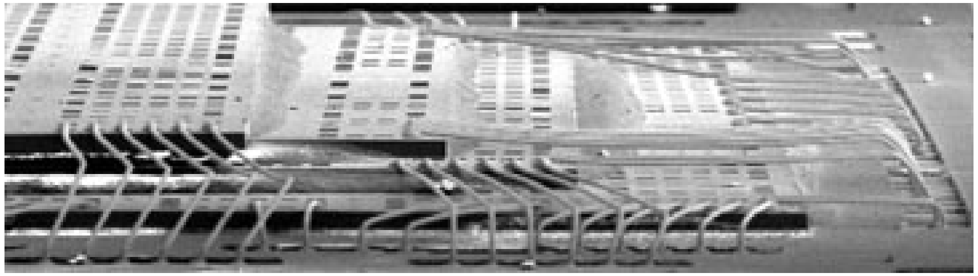
Same-size (or reduced botton die) stack



Pyramidal Stack



Intel quad stack

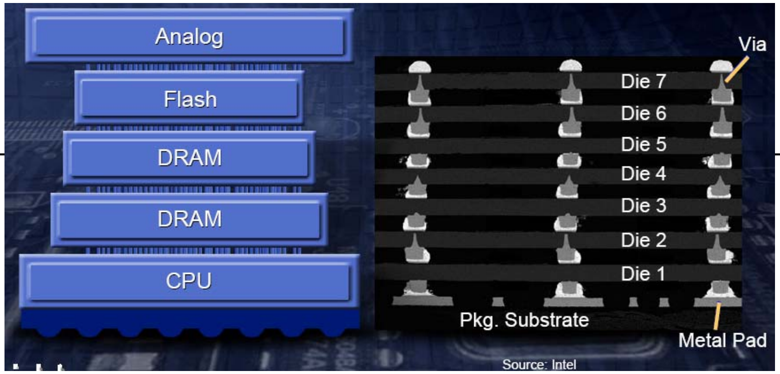


Source: DPC

Packaging

Intel

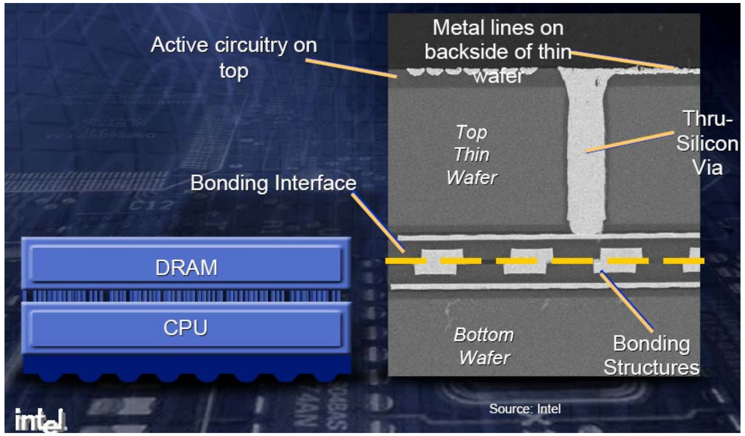
- Package-on-Package construction (folded flex circuit from Tessera)
  - Processor, flash & SDRAM



Source: Intel

- Prototype of 8-dies stack with no interposer (50µm die thickness)

- Intel is now using copper pillar bumping for its processors



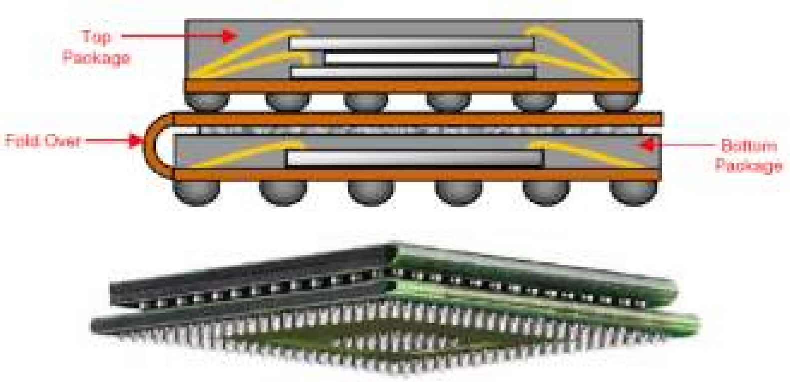
Source: Intel

Packaging

Tessera

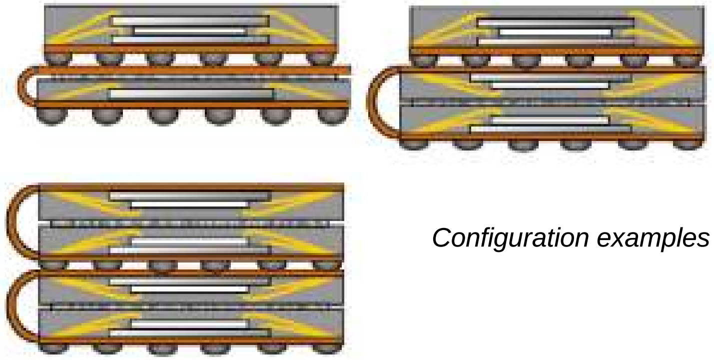
Carrier	R	L (Q)	C	Interconnectivity
Flex		60		14 lines/mm
Si/GaAs		?	0,11nF/mm²	?

- **Package-on-Package (folded carrier)**
  - 2 metal-layer polymide providing electrical and mechanical properties for interconnect
- **Processor with associated memory**



Tessera/Intel folded stacked CSP package

Folded Stacked CSP assembly process



Configuration examples

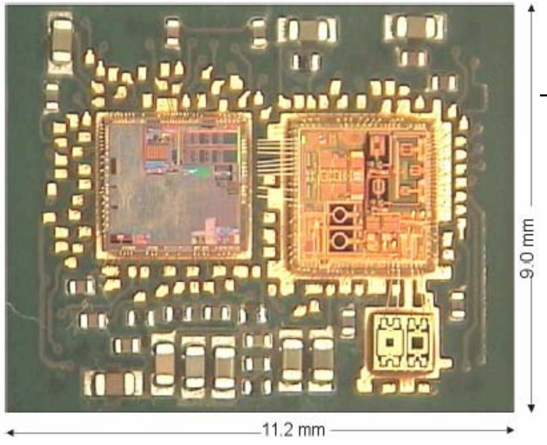
Sources : Prismark wireless technology report – March 2005

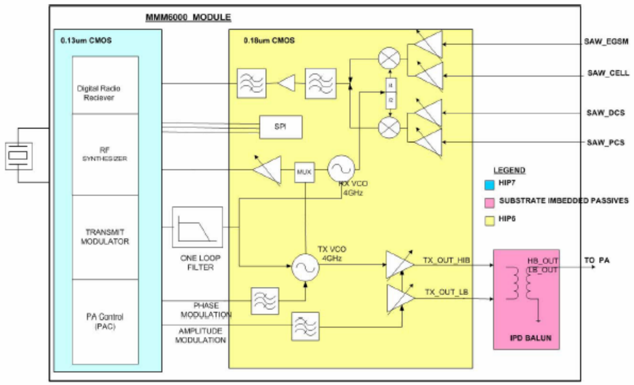
Packaging

MMM6000 Module

Freescale

- Single package transceiver for quad band EGPRS (GSM/GPRS/EDGE)
  - 11.2x9mm
  - 9 SMDs 0402
  - 18 SMDs 0201
  - 2.8x2.6mm 0.13µm CMOS
  - 2.7x2.9mm 0.18µm RFCMOS
  - 1.1x1.1mm IPD device

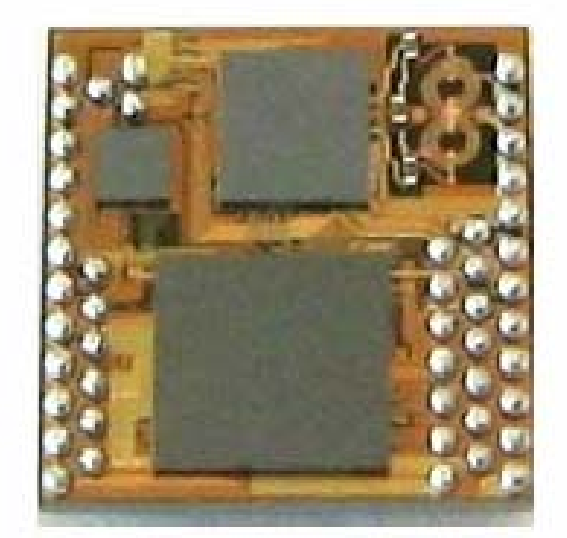




Packaging

- Silicon substrate with integrated passives

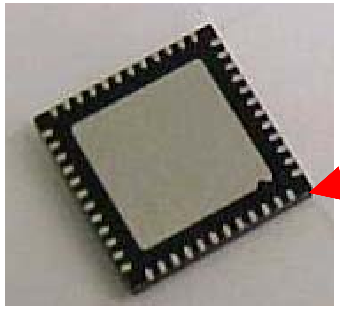
Size (mm)	9x9
I/O	12x12
Availability	Sampling?
Known Partnerships	?

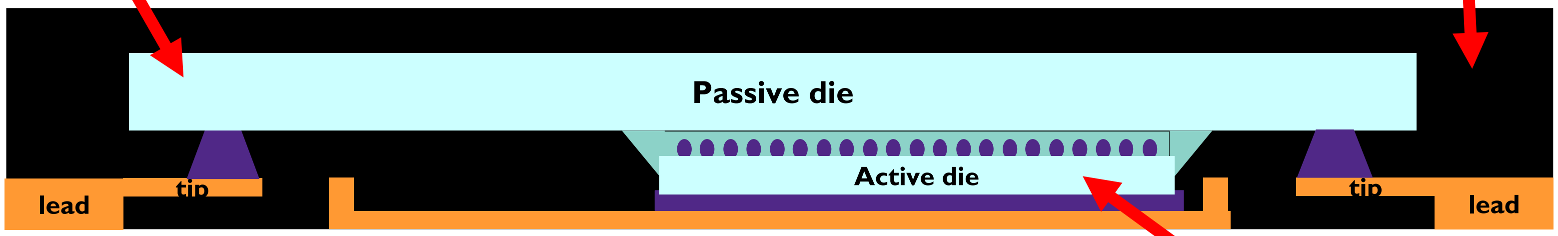


Source : Sychip

Packaging

NXP Silicon-based SiP concept





Standard HVQFN package

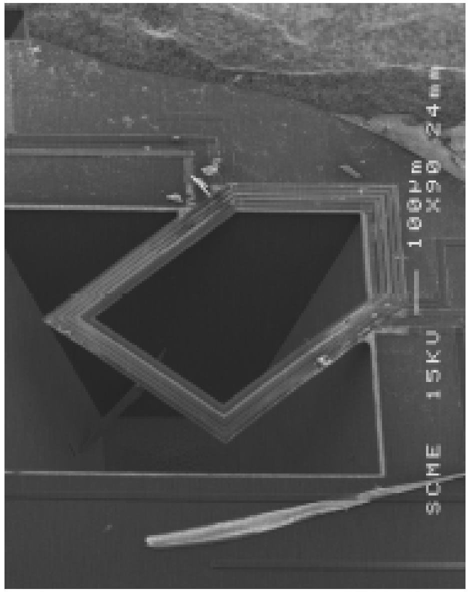
Flip chip Passive die

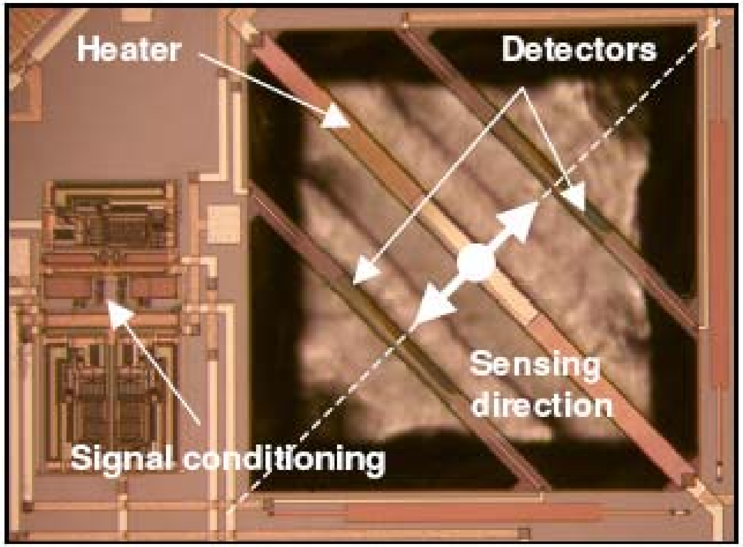
Flip chip Active die

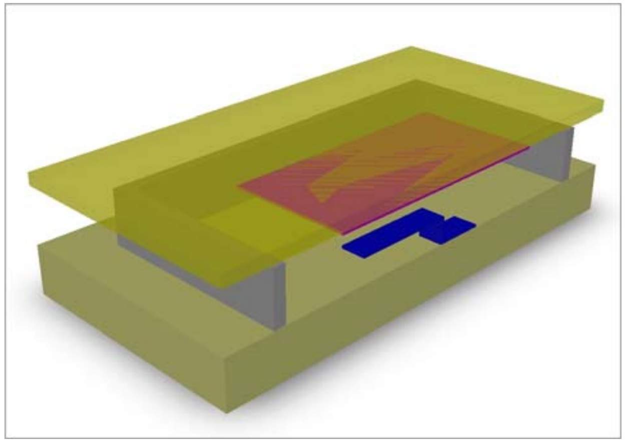
Key benefits

- **Performance (flip chip interconnects)**
  - ❖ **Inductance / 4 to 6!**
- **Size (3D stacking, passive integration)**
- **Low thermal resistance**

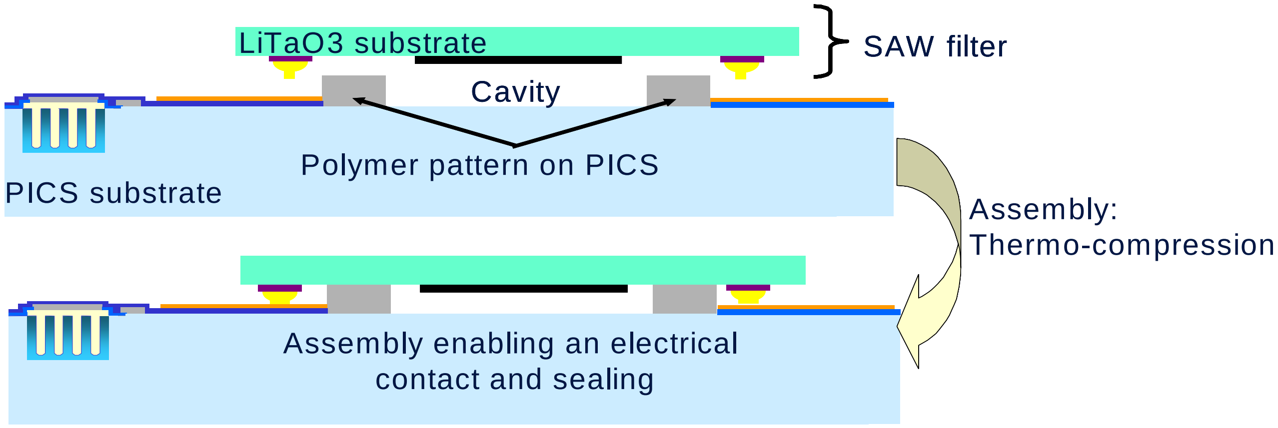
MEMS Packaging







MEMS packaging
SAW filter on silicon substrate



LiTaO3 substrate

SAW filter

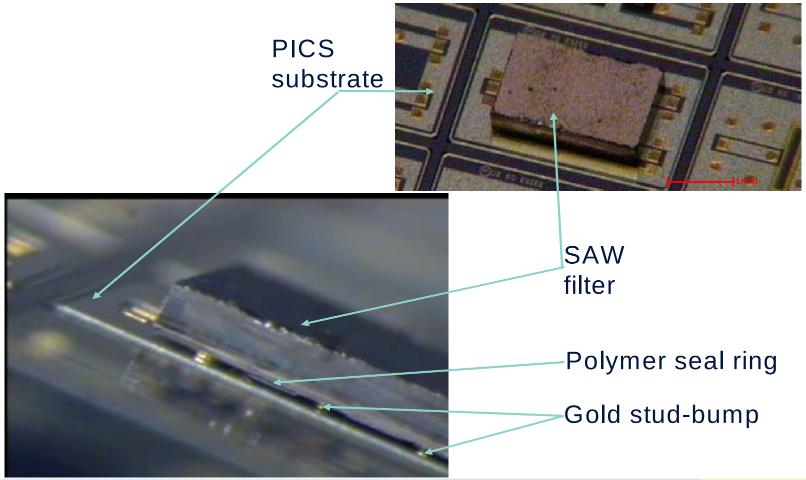
Cavity

Polymer pattern on PICS

PICS substrate

Assembly:
Thermo-compression

Assembly enabling an electrical contact and sealing



PICS substrate

SAW filter

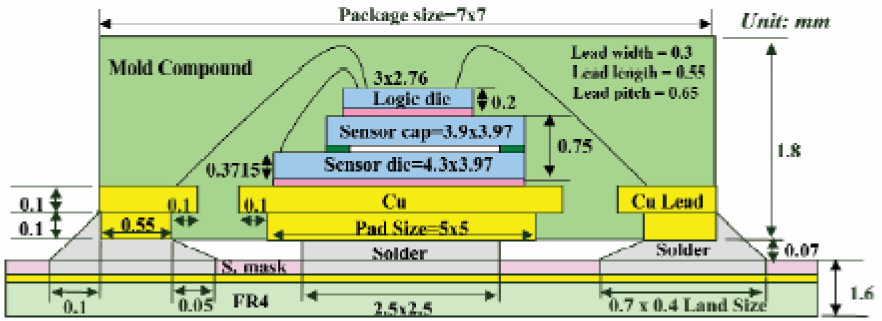
Polymer seal ring

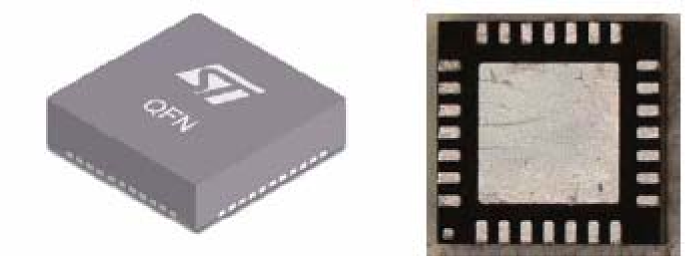
Gold stud-bump

MEMS Acceloremeter stacked die package

STMicroelectronics

- Targeted applications
  - Toys, medicals, phones, anti-theft
- 4.3x4.0x0.4mm MEMS die
- 3.9x4.0x0.4mm cap die
- 3x2.8x0.2mm logic die
- QFN 28 I/O, 2 stacked die
- Die to die and die-leadframe wirebonds





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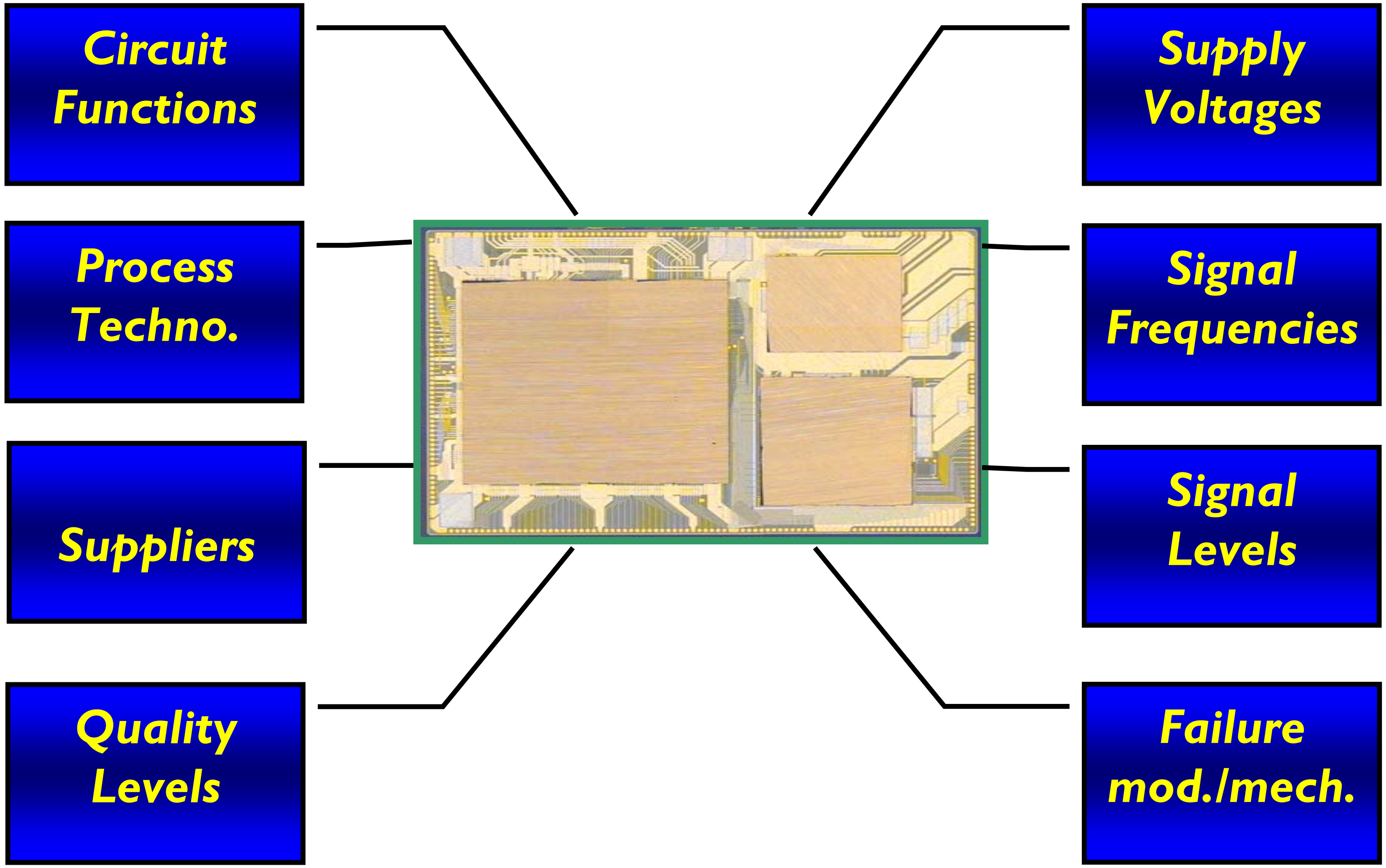
SiP vs SoC

Compared to a SoC, a SiP may have more…



Circuit Functions

Process Techno.

Suppliers

Quality Levels

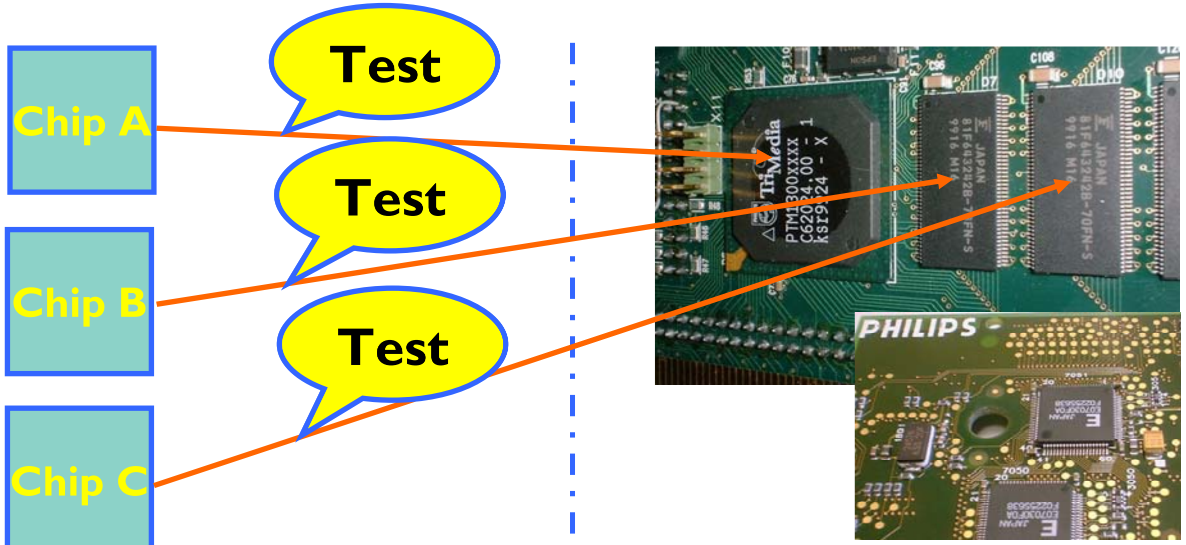
Supply Voltages

Signal Frequencies

Signal Levels

Failure mod./mech.

NXP SiP Test Vision

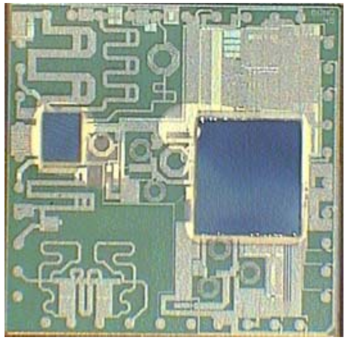


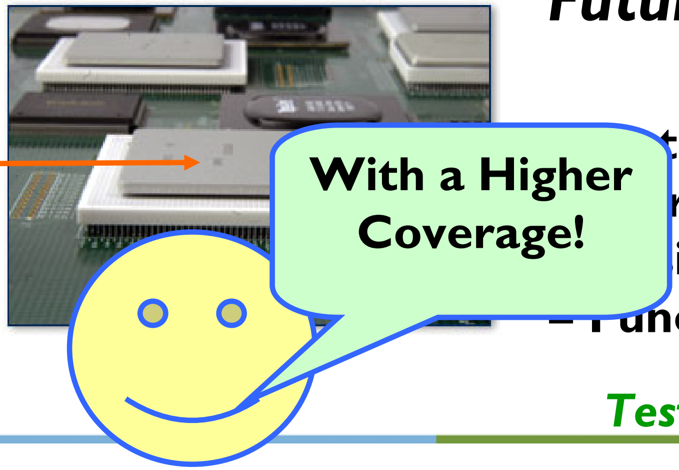
Test cost = 3U

Today:

+ Test of PCB
+ Interconnects
+ Passives
+ Functional

Test cost = 4U





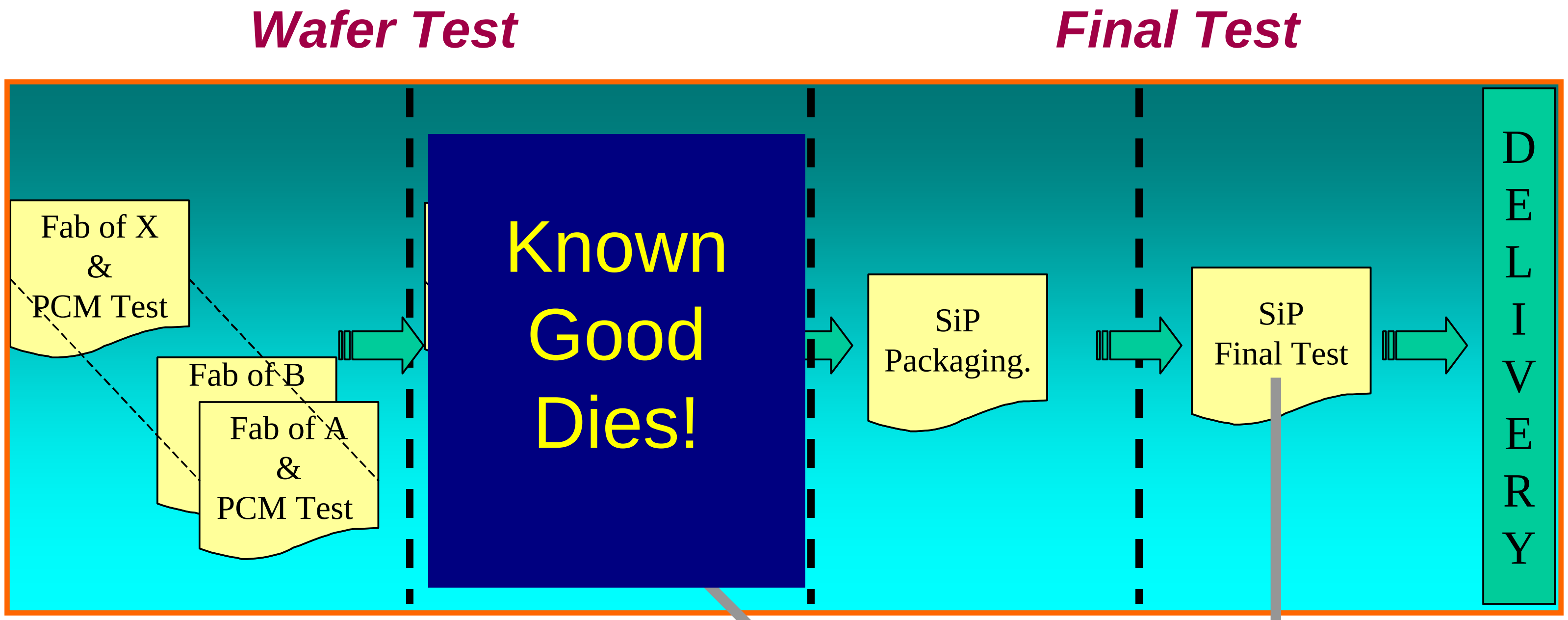
Future (w SiP):

t of PCB
rconnects
ives (almost 0!)
– unctional

Test cost < 3U

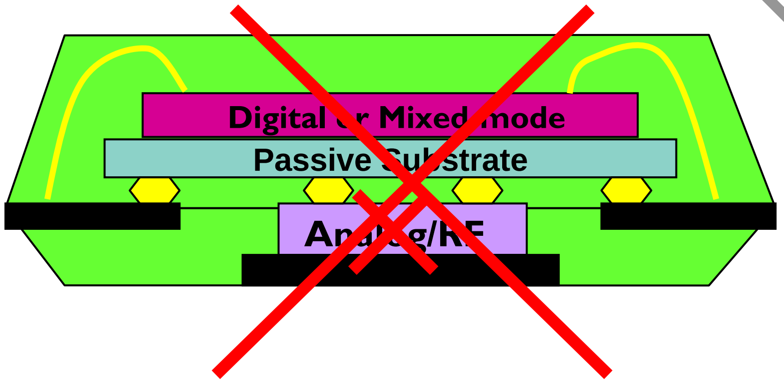
Test cost << 4U

A Complex Test Flow…



Wafer Test

Final Test



System-level Test:

- DfT
- Fast Diagnosis

  and…
- Known-Good-Dies!

Known-Good-Die

KGD Definition:

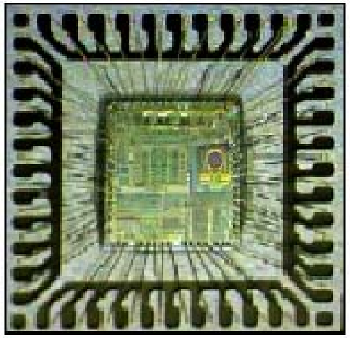
(from a test perspective)

- Good enough to meet, at die level, at least the same quality level as a packaged IC

- Implies that :
  - **KGD test = WT + FT of a packaged die!!**

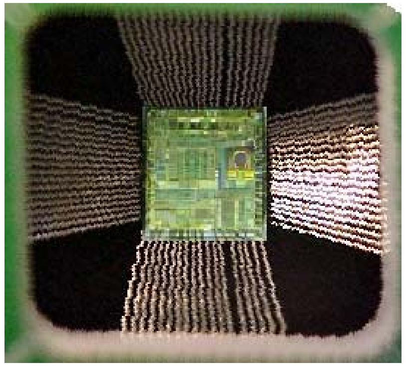
Cantilever RF probing concept

<u>Package:</u>
Wire bonding length

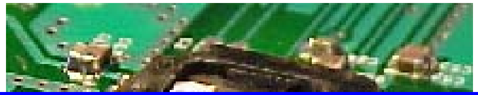


Bonding: 1-3mm
Leadframe: mm size

<u>Die under probes:</u>
Needle length



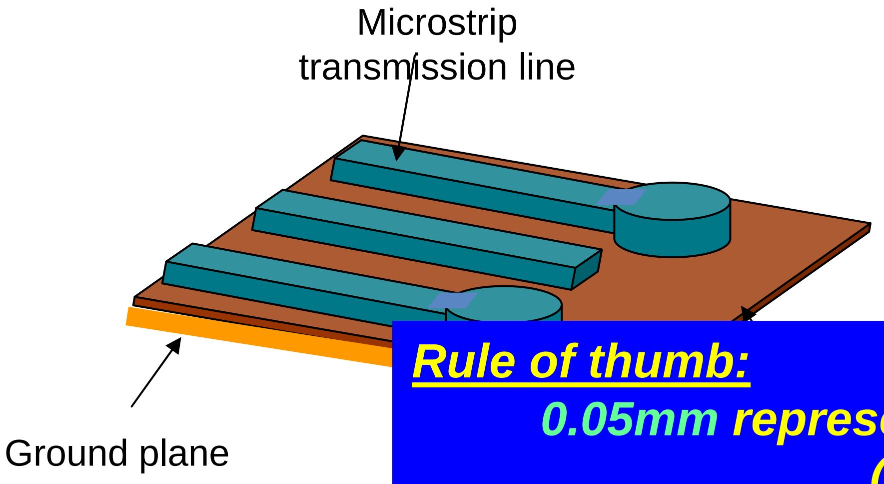
Probe tips: 3-5mm

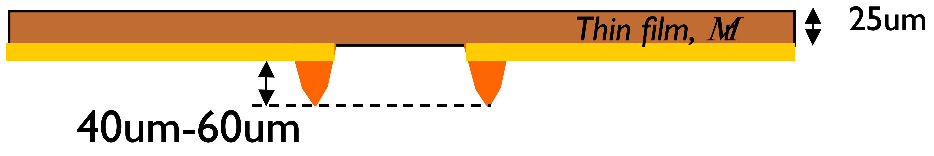


<u>Rule of thumb:</u>
10mm represent 10nH serial inductance
→ impossible to test a PA @freq, for example!

Total Probe length: 10-15mm

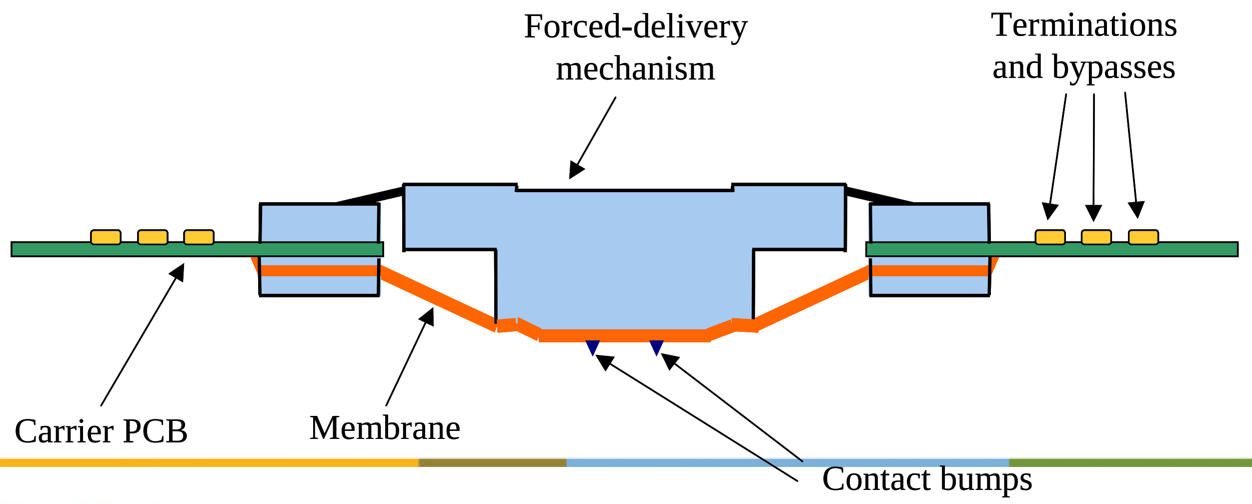
Thin film technologies for RF probing





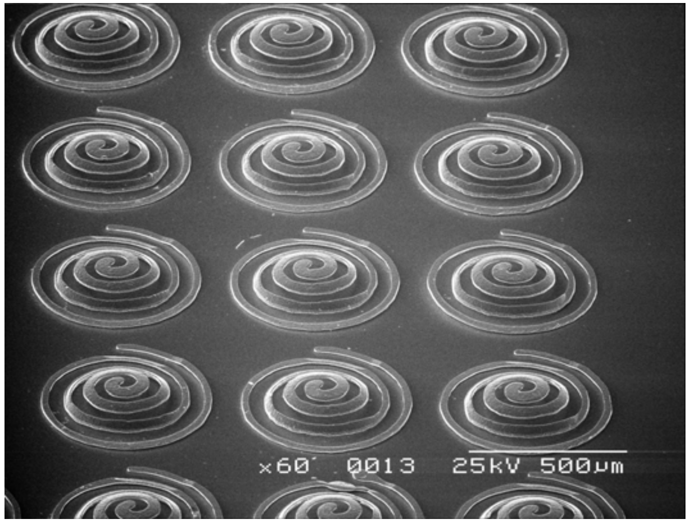
Rule of thumb:

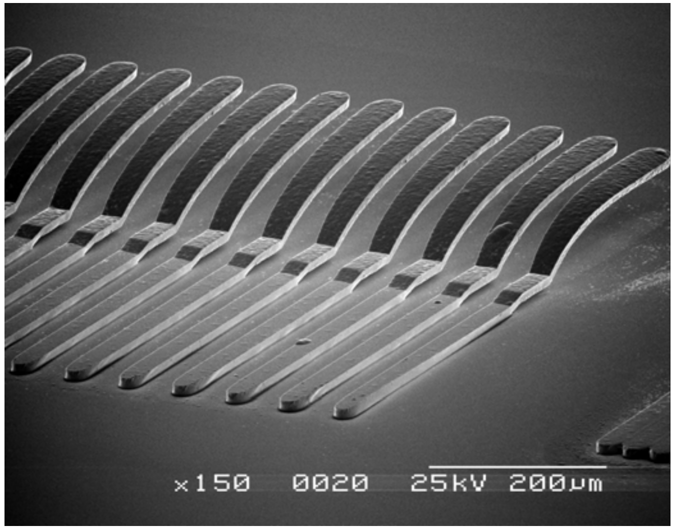
0.05mm represents less than 0.5nH serial inductance (typical 0.2nH specified)

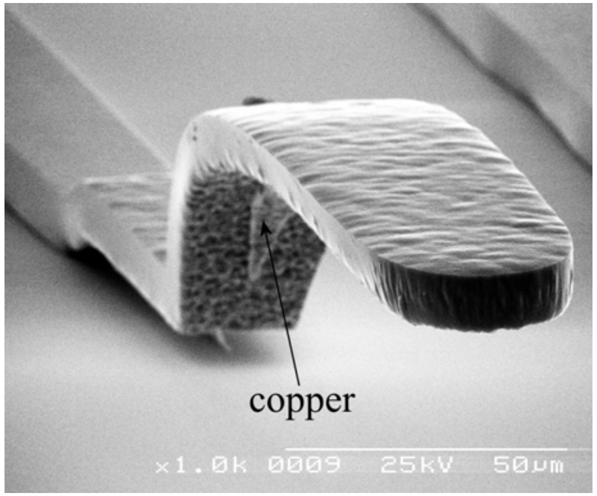


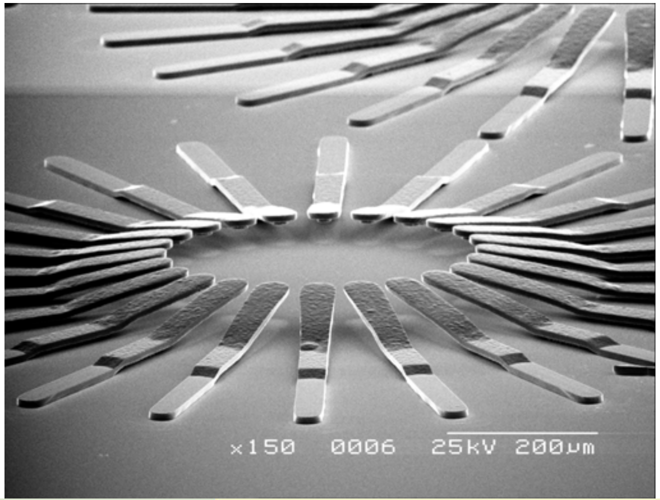
MEMS technologies for RF probing

- **Springs for solder bumps**
- **Cantilevers for contact pads**
- **RMS roughness 15 nm**
- **Length to 600 µm**
- **Width 29-55 µm**
- **Thickness 11 µm**
- **Planarity 1.07 µm over 1 mm range**







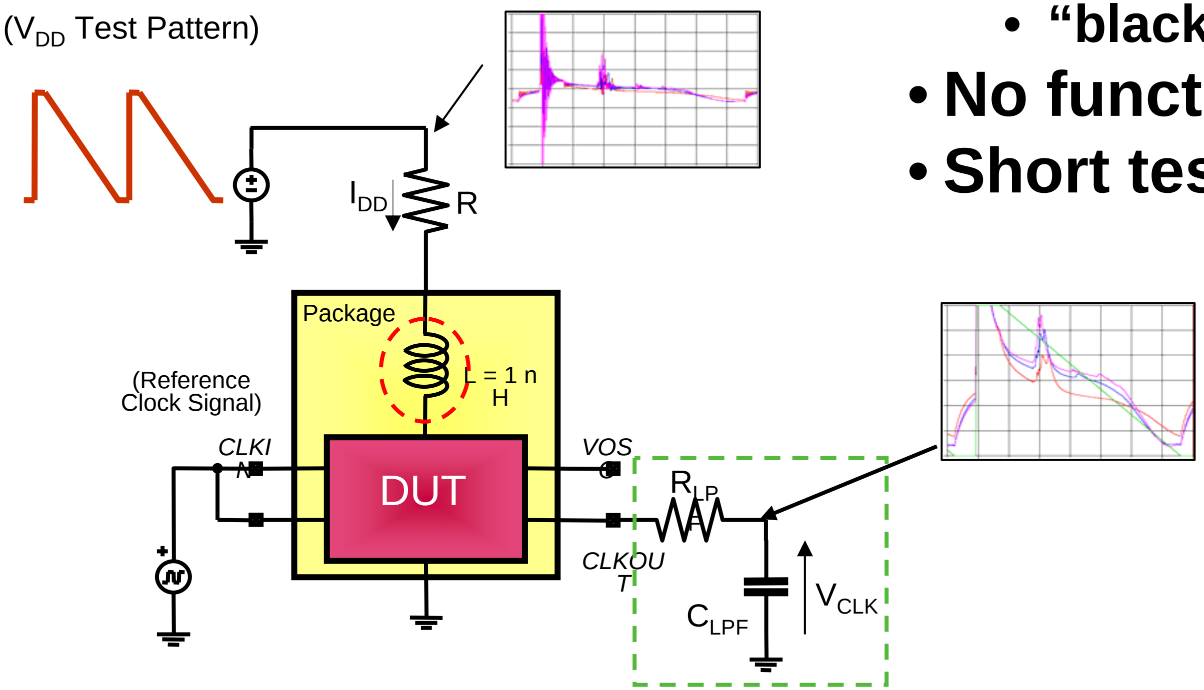


Full Test at Wafer

Alternative Test Methods

Signature-based Testing

- **Power supply sweep**
- **I-V Signatures**
- **Multiple observation points**
- **Simple method**
  - **“black-box” methodology**
- **No functional testing**
- **Short test time**



Management of diversity

Which leads SiP package test to:

✓ Require greater *diversity of ATE resources* than SoC

✓ Require greater *diversity of test & reliability screen methods* than SoC

✓ Have large *disparities in test times and resource utilization* among die

Solutions:

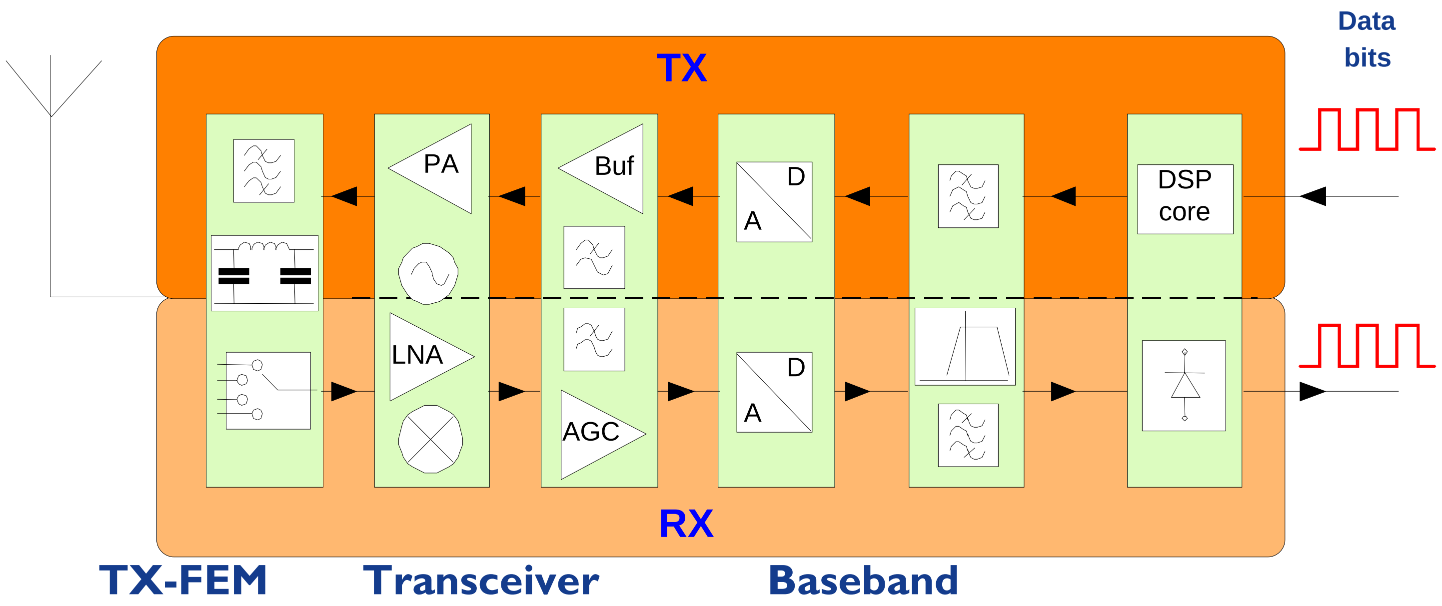
✓ Insert in multiple testers

✓ Better scheduling of test resources to allow independent, simultaneous test of each accessible chip in SiP

✓ BIST / DfT / DSP

System Testing Issues

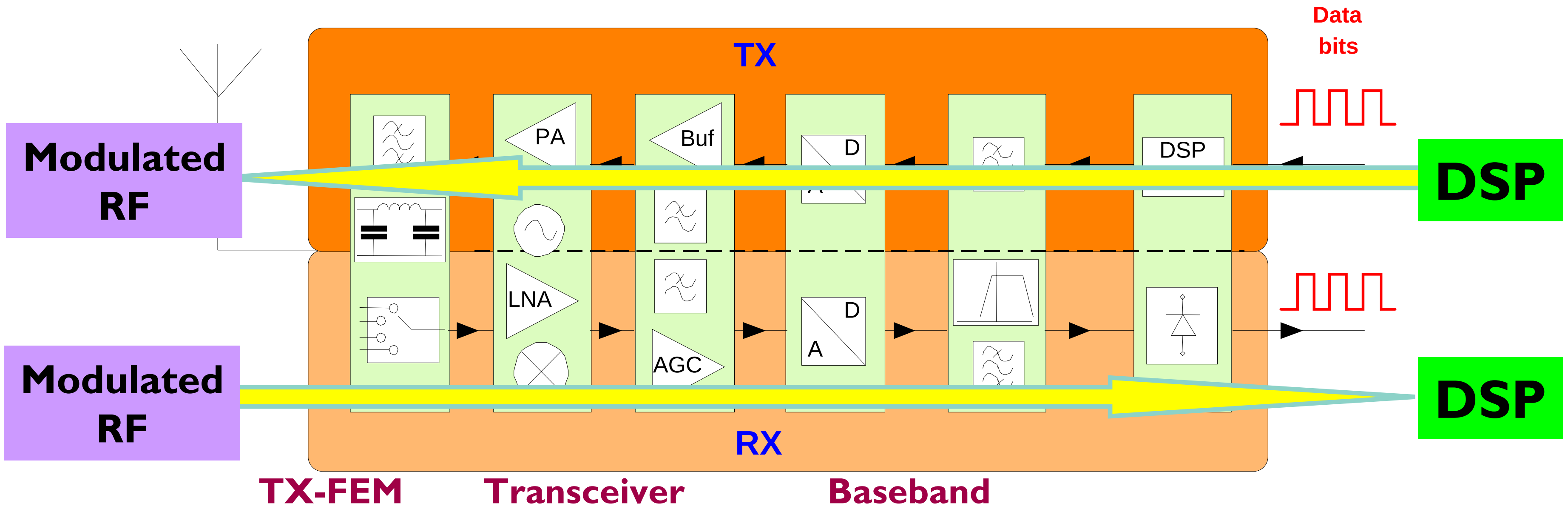
Intermediate Test Points may affect signal integrity and leads to longer test times



So, what to do?

1. Test Rx and Tx paths independently

Ref: "Seamless test of Digital Components in M/S paths", S. Ozev et al



Pro:

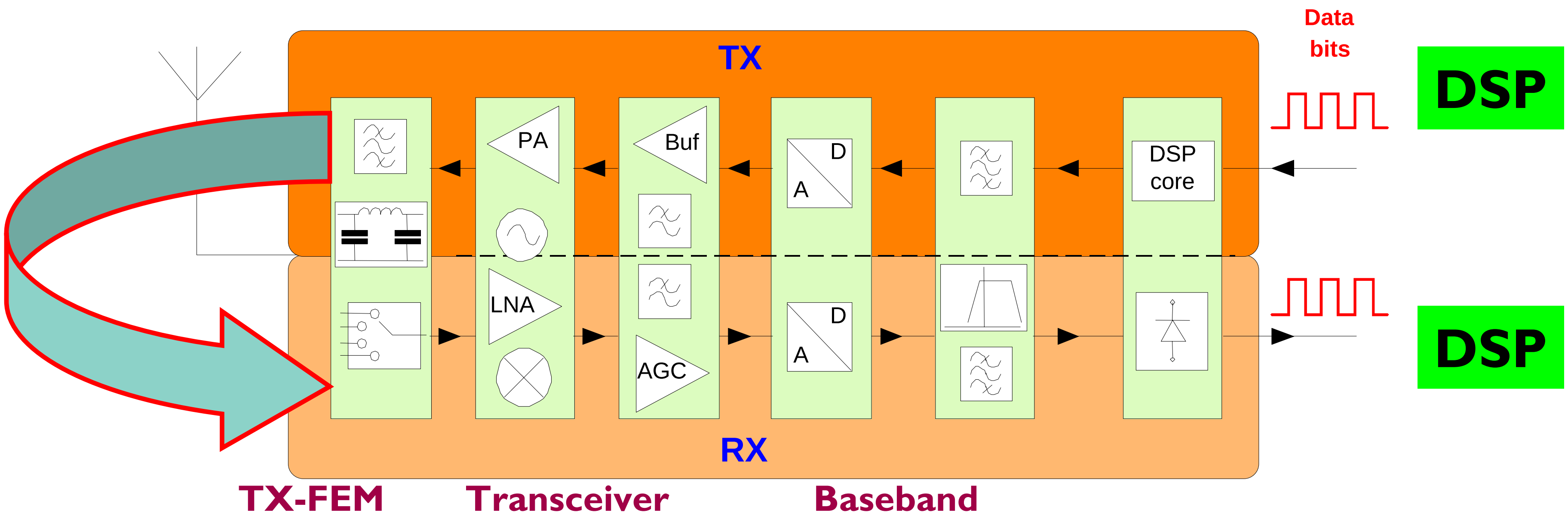
- close to the application conditions
- two-pass test = reduced test time
- reduced risk of signal degradation

Contra:

- expensive ATE
- quality of contacts critical
- diagnosis??

2. Test Rx and Tx paths together (loop-back)

Ref: "Wafer level RF Test and DfT for VCO Modulating Transceiver Architectures", S. Ozev et al



Pro:

- **low-cost (no?) ATE**
- **benefit from PICS capabilities**
- **test simulation**
- **easier BIST implementation**

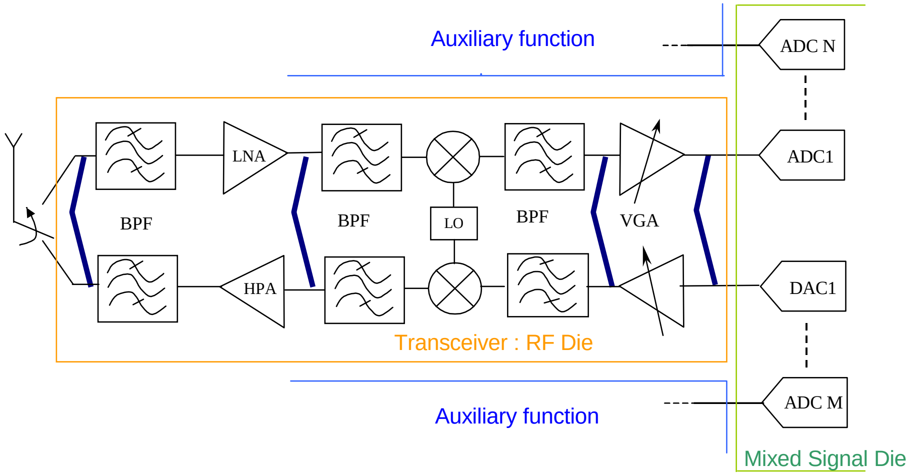
Contra:

- **need DfT (not a simple short-circuit!)**
- **correlation with lab measurements**
- **mgt of yield / test escapes**
- **diagnosis??**

Loop-back starts at the beginning

Biggest advantage:

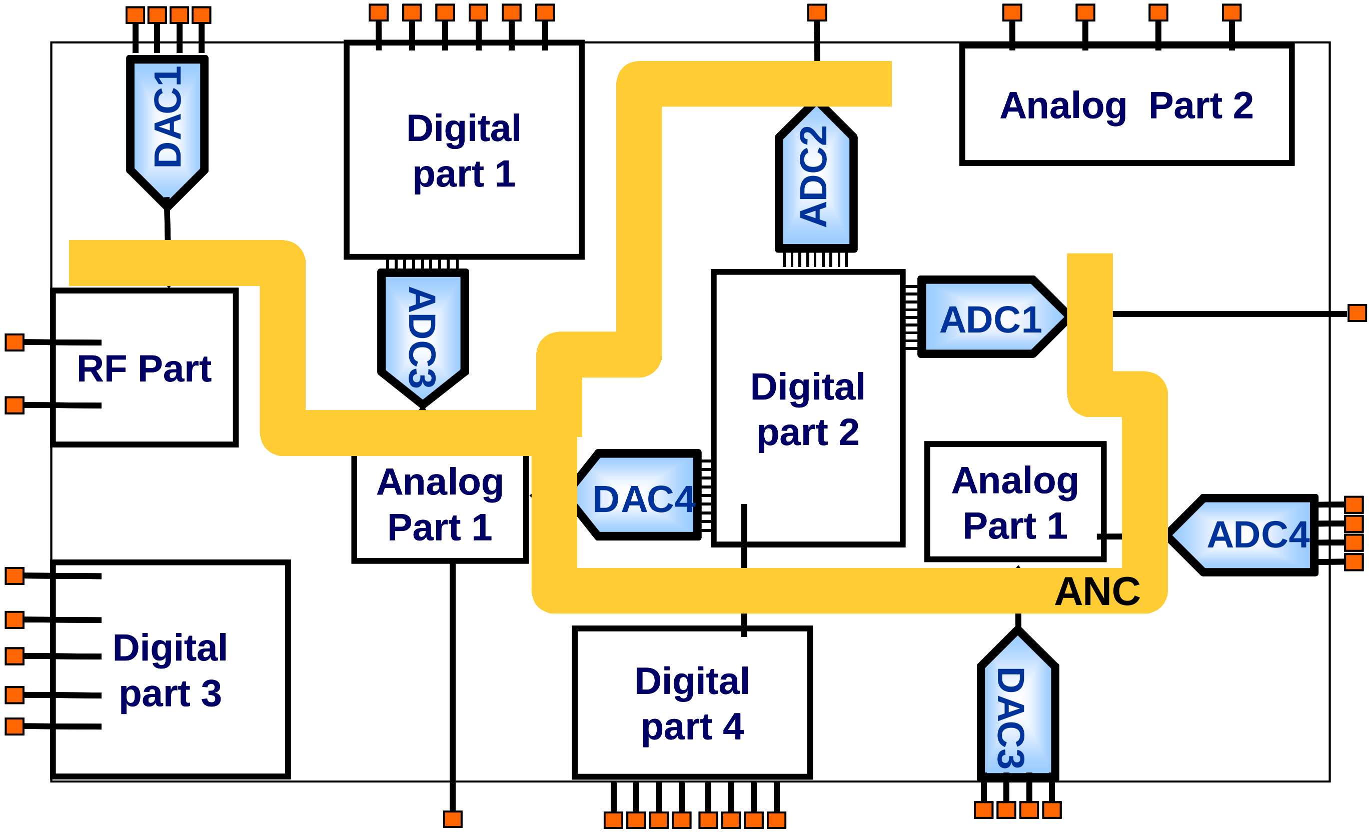
Full digital test



Challenges:

- ❑ **Loop-back**: Analog Design For Test issue
- ❑ **Test methods**: digital post processing
  - ✓ *ADCs DACs test*
  - ✓ *Compensate data converters errors → improve their performances*
    → similar to measurement instruments
  - ✓ *Test each block through other blocks*

Loop-back starts at the beginning

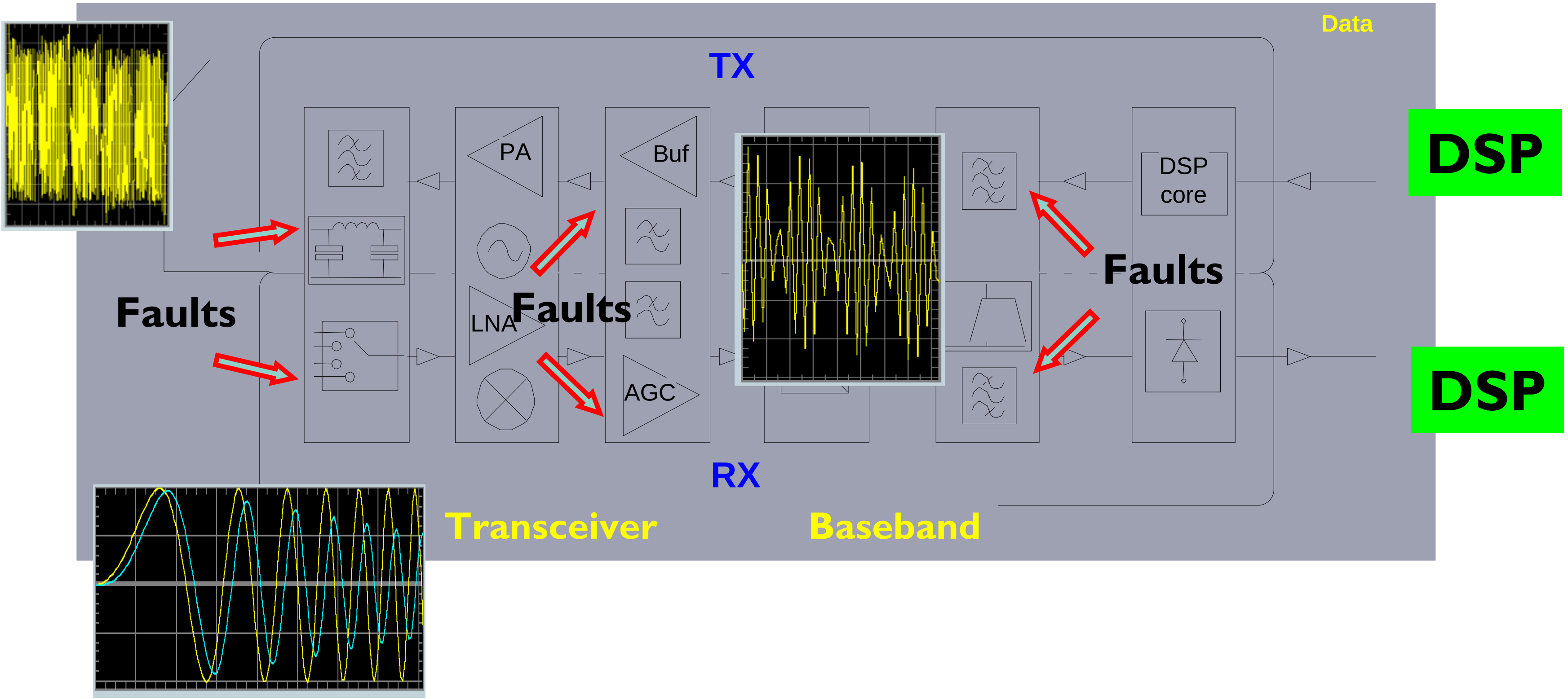


Strategy:

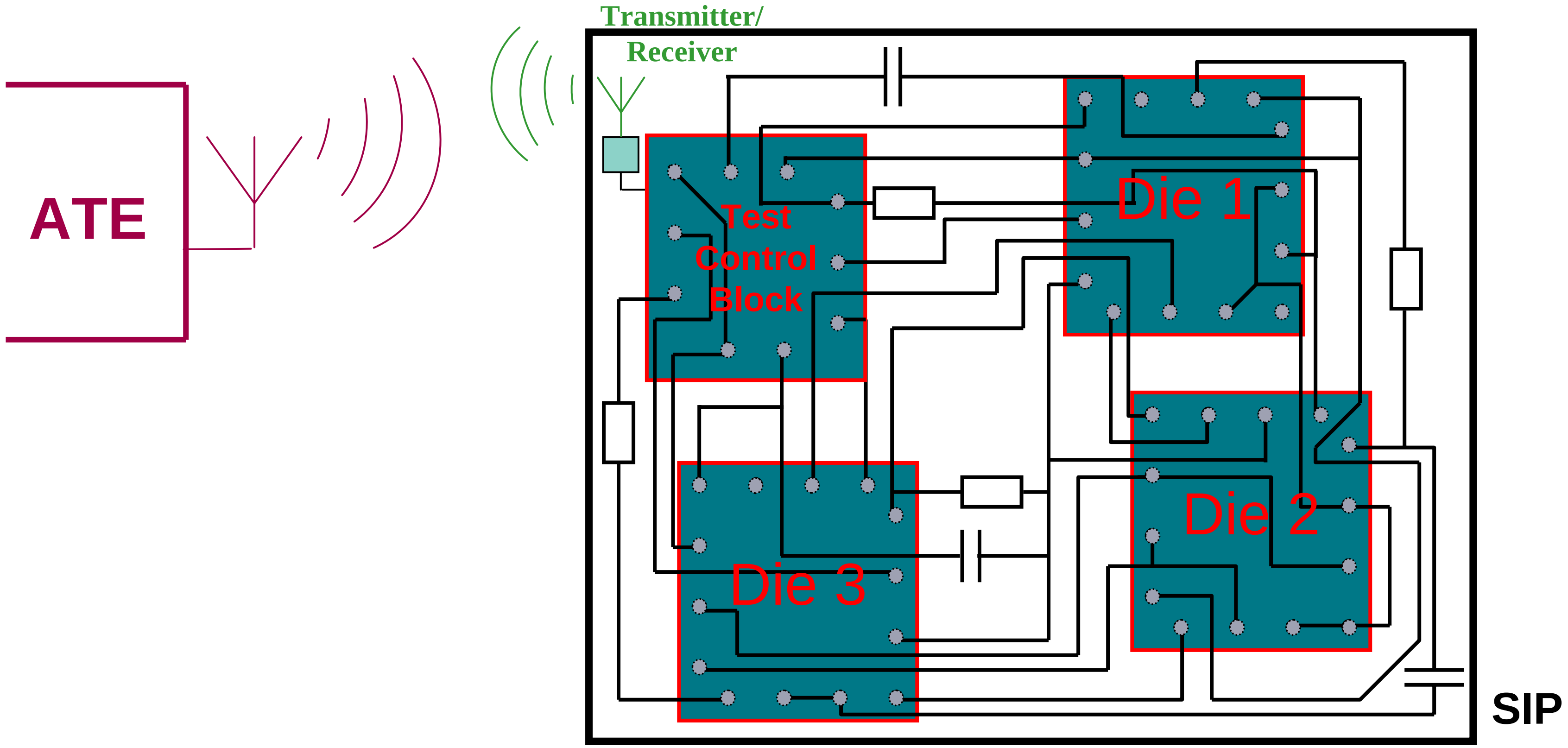
1. Find DSP-based methods / algorithms to re-use the analog/ms blocks as instruments
2. Implement hardware that supports the methods

SiP Testing

- **Diagnosis capabilities using signatures**



Testing Wirelessly (LIRMM+NXP)



Architecture for testing a SiP wirelessly

Outline

- Definition
  - Market / Applications
    - Design and technology
    - Packaging Technologies
  - Test Challenges
- **Conclusion**

Summary

- ***SiP is:***
  - **significantly growing**
  - **not a SoC**
  - **represents many challenges in:**
    - **design (tools, EMC,…)**
    - **packaging (stacked, planar, PiP, PoP, …)**
    - **test (KGD, System Testing,…)**

thus, SiP technologies offer many perspectives / opportunities
to students, researchers and engineers

Thank You

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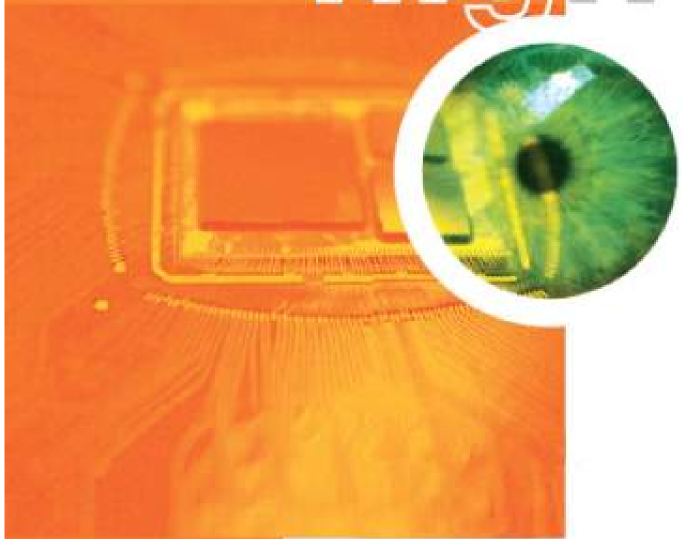
think high-tech



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Introduction 20h

SoC Design Methodologies 60h

Coupling Effects 60h

Advanced Processes 60h

Manufacturing 40h

SiP Design Methodologies 80h

Advanced Tests 80h

Business Management 40h

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- 1470 hours
  - 560 h classrooms (5 months) and
  - exercises (1 month)
  - 910 h Internship (6 months)
- 2 intakes: February and September

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