# *Mixed-Signals Integrated Circuit Testing*

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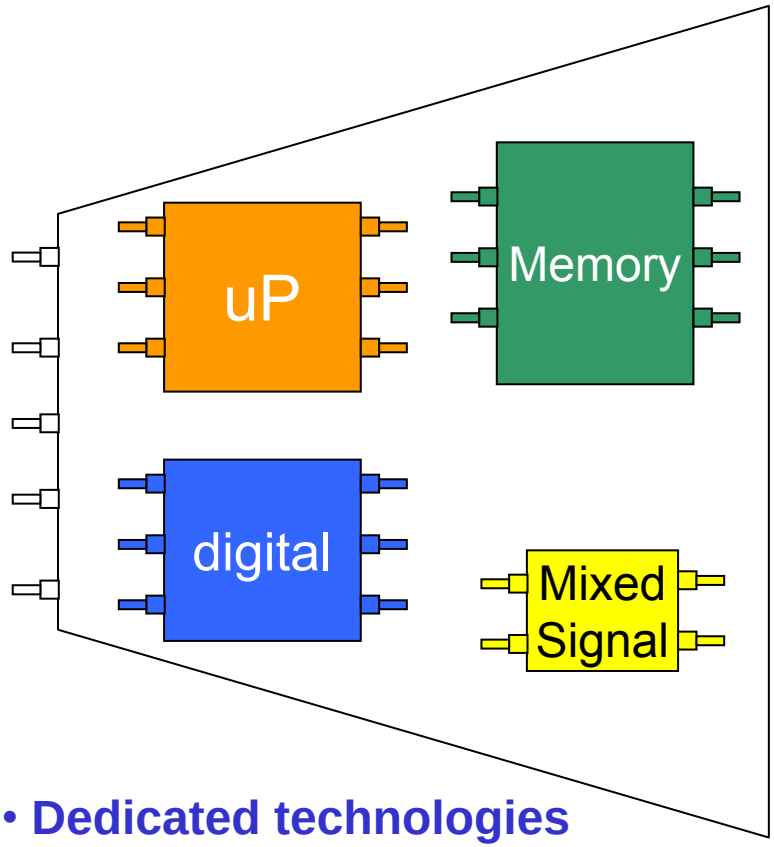
# *Outline*

1. Introduction
2. Analog versus digital testing
3. Structural and functional testing
4. Analogue DFT/BIST techniques
5. Computer-Aided Test (CAT) techniques
6. Conclusions

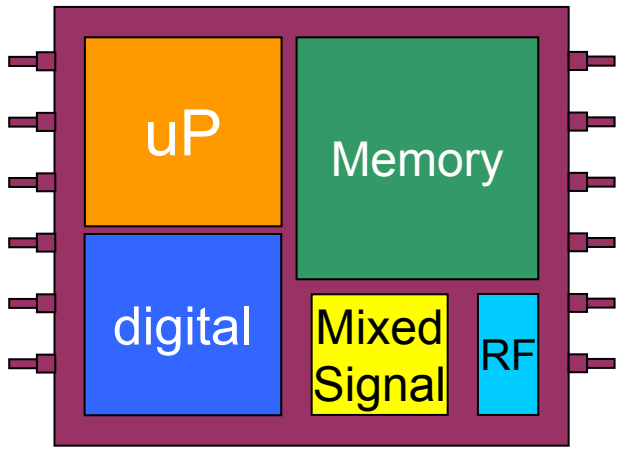
# 1 Introduction

**System-On-Board (SOB)**




- **Dedicated technologies**
- **Pre-tested ICs**
- **Board-Level Test**

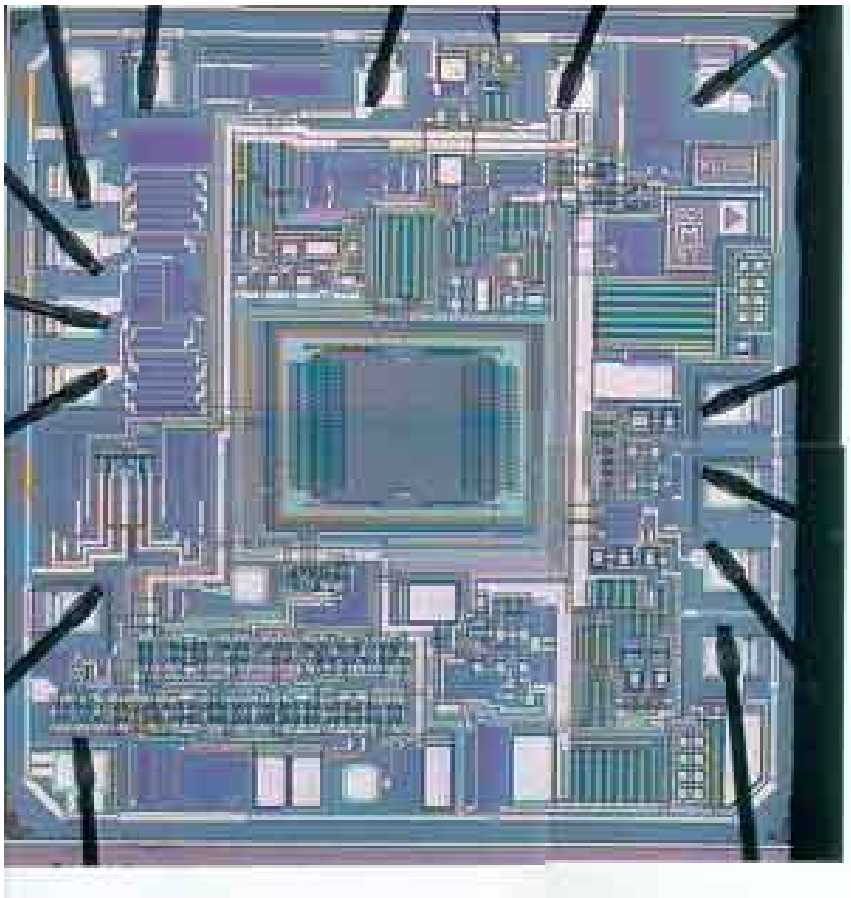
**System-On-Chip (SOC)**



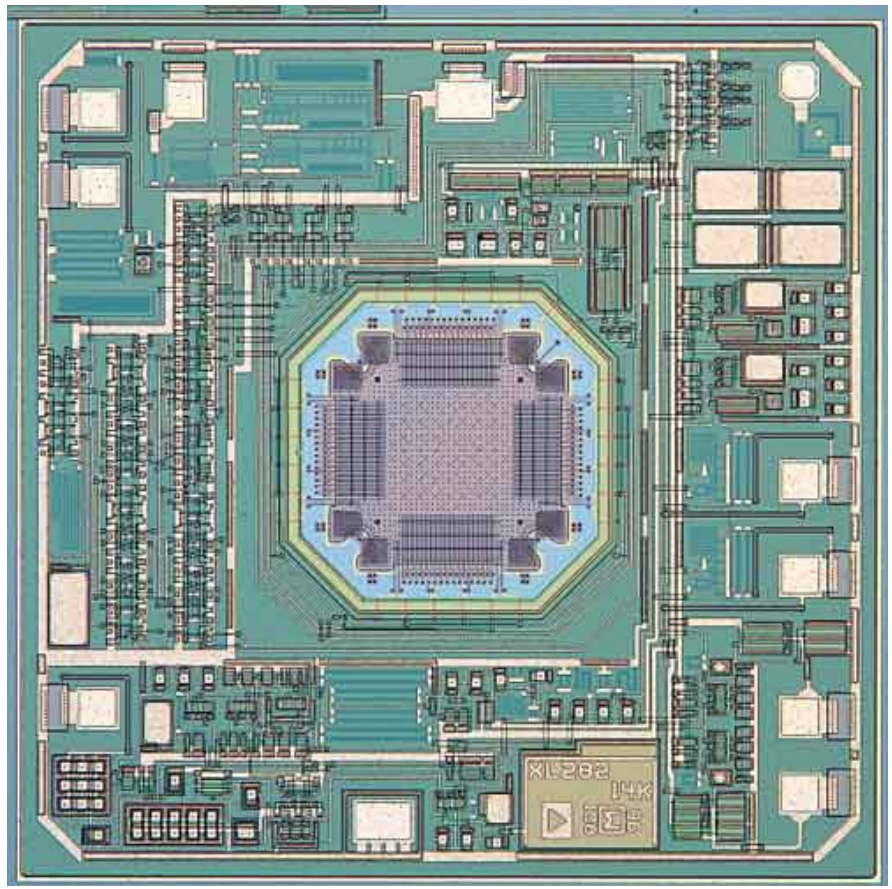

- **Mixed technologies on the same chip**
- **Pre-designed blocks (not tested)**
- **Core and IC level test data**

# 1 Introduction

## ➔Accelerometer examples :



Self-testable one axis accelerometer



Self-testable two axis accelerometer

# 1 Introduction

➔ **Motivation of mixed-signals testing :**

- Growth in mixed-signals ICs : efforts to combine analog, digital and memories to provide SoC solutions
- Driven by communication and consumer markets
- In mixed-signal systems, over 90% is often digital but 90% test cost can be analogue
- Communications and biomedical applications are demanding new SoC and SiP devices
- Testing mixed-signals devices is very different from digital testing

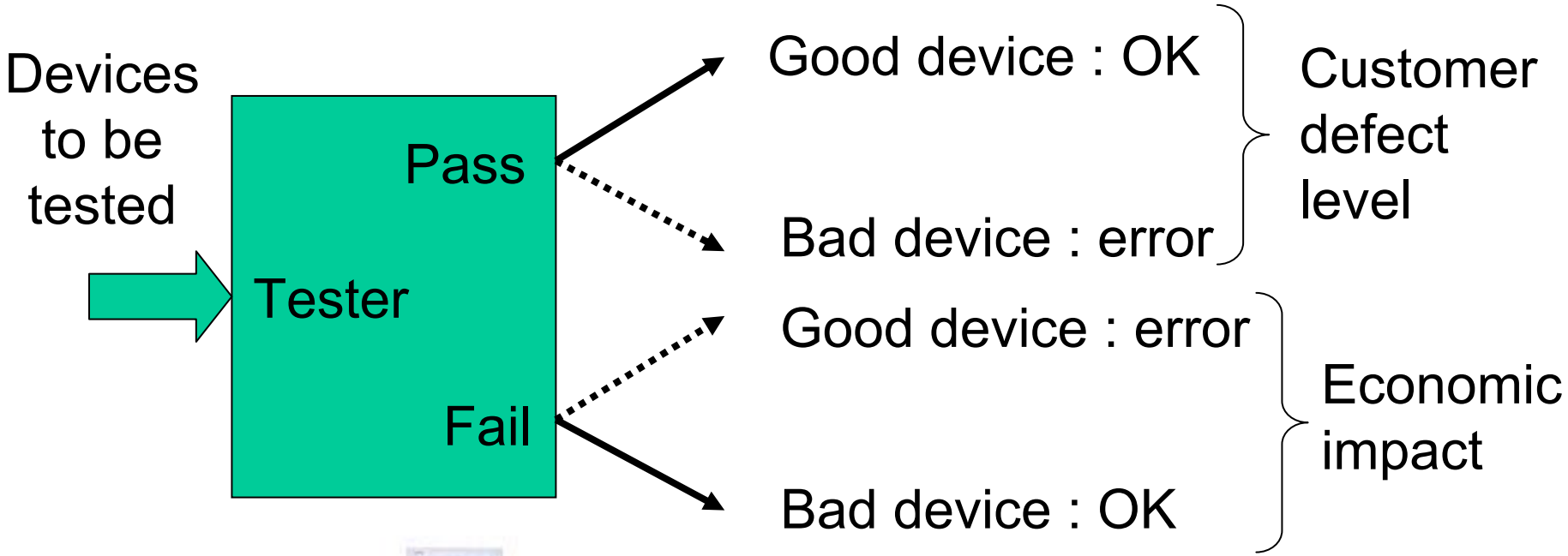
# 1 Introduction

➔ **What are we testing for ? Physical defects**

- Cause : process disturbances
  - Local (silicon defects, photolithography spots …)
  - Global (mask misalignment, bad micromachining …)
- Fault types :
  - Structural faults : opens, shorts, …
  - Parametric faults : variations in device parameters have a more important impact on analogue testing
- Failures :
  - Hard (incorrect performance, large performance error)
  - Soft (marginal out-of-spec performance)

# 1 Introduction

➔ **Production test: quality and economic impact**

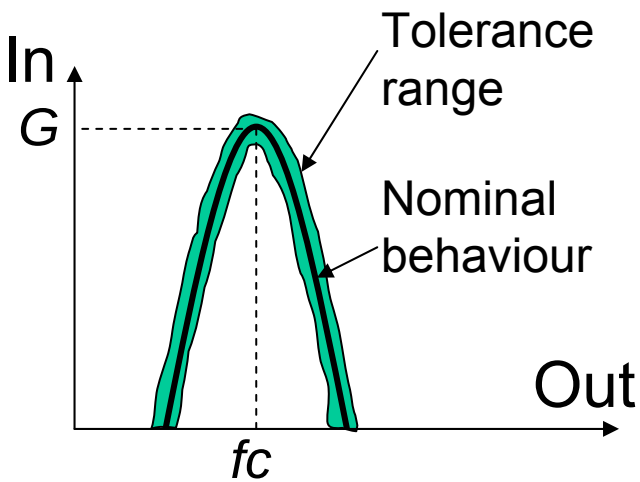



# 2 Analog versus digital testing

- **Digital Testing** :
  - ♠ Discrete binary values (0/1)
  - ♠ Truth tables (exact)
  - ♠ Simple parametric testing (e.g. current consumption at wafer level)
  - ♠ Fault-based (structural) or functional testing based on exact logic behaviour at chip and package levels

| X1 | X2 | X3 | X4 | Y |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |

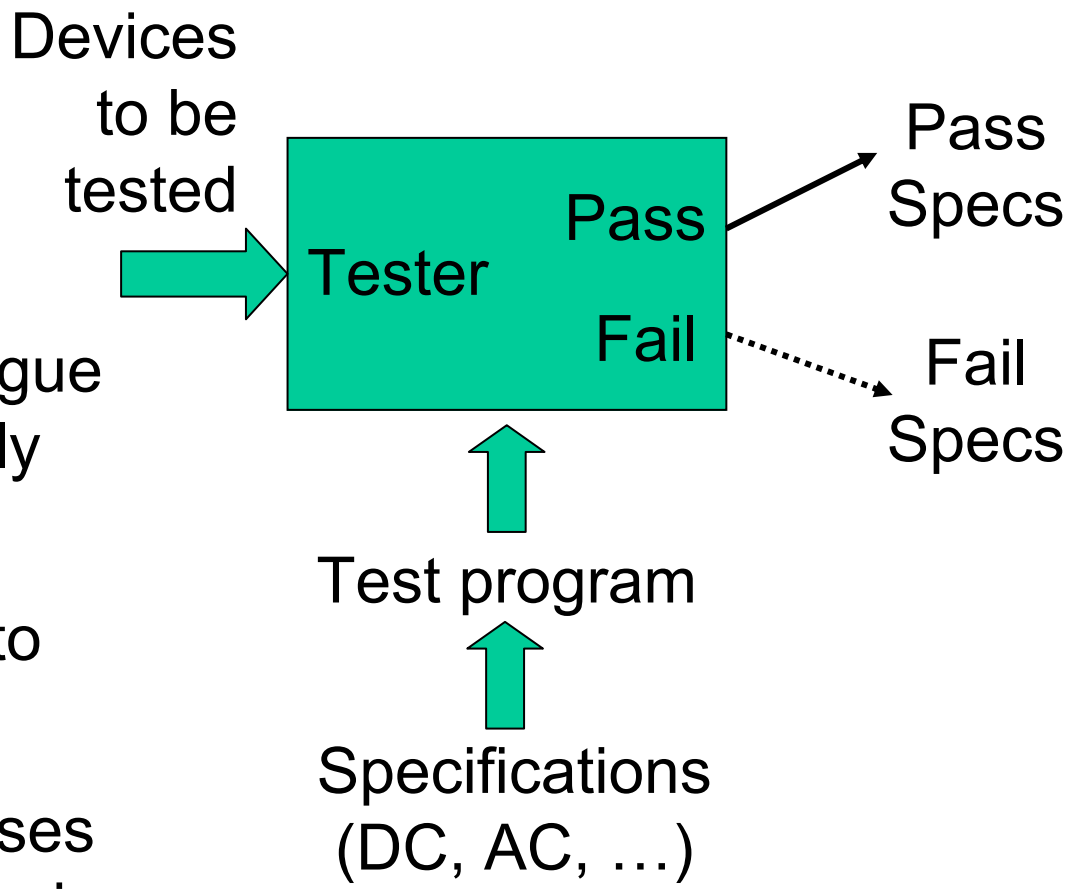
- **Analog Testing** :
  - ♠ Continuous values
  - ♠ Differential equations (approx)
  - ♠ Specification-based testing considering acceptance ranges for design parameters



# 3 Structural and functional testing

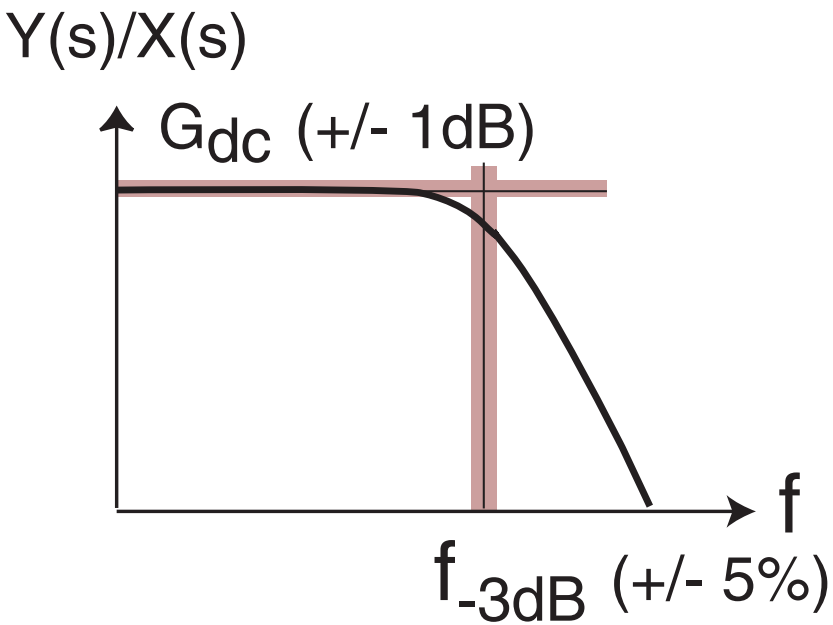
➔ ***Functional testing :***

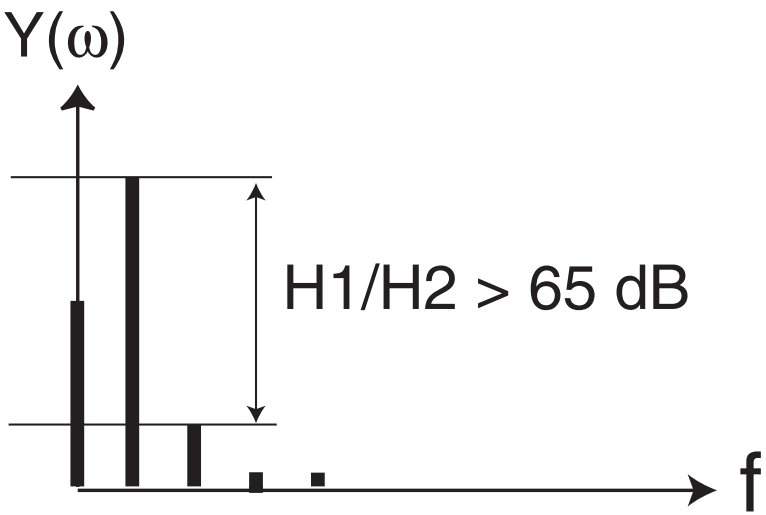
- Test matches the functionality
- Simple test vector generation
- Typically used for analogue devices but leads to costly test equipment
- Lengthy test time due to redundant tests
- Test complexity increases exponentially with device size for digital circuits



# 3 Structural and functional testing

➔ ***Examples of specification-based tests***

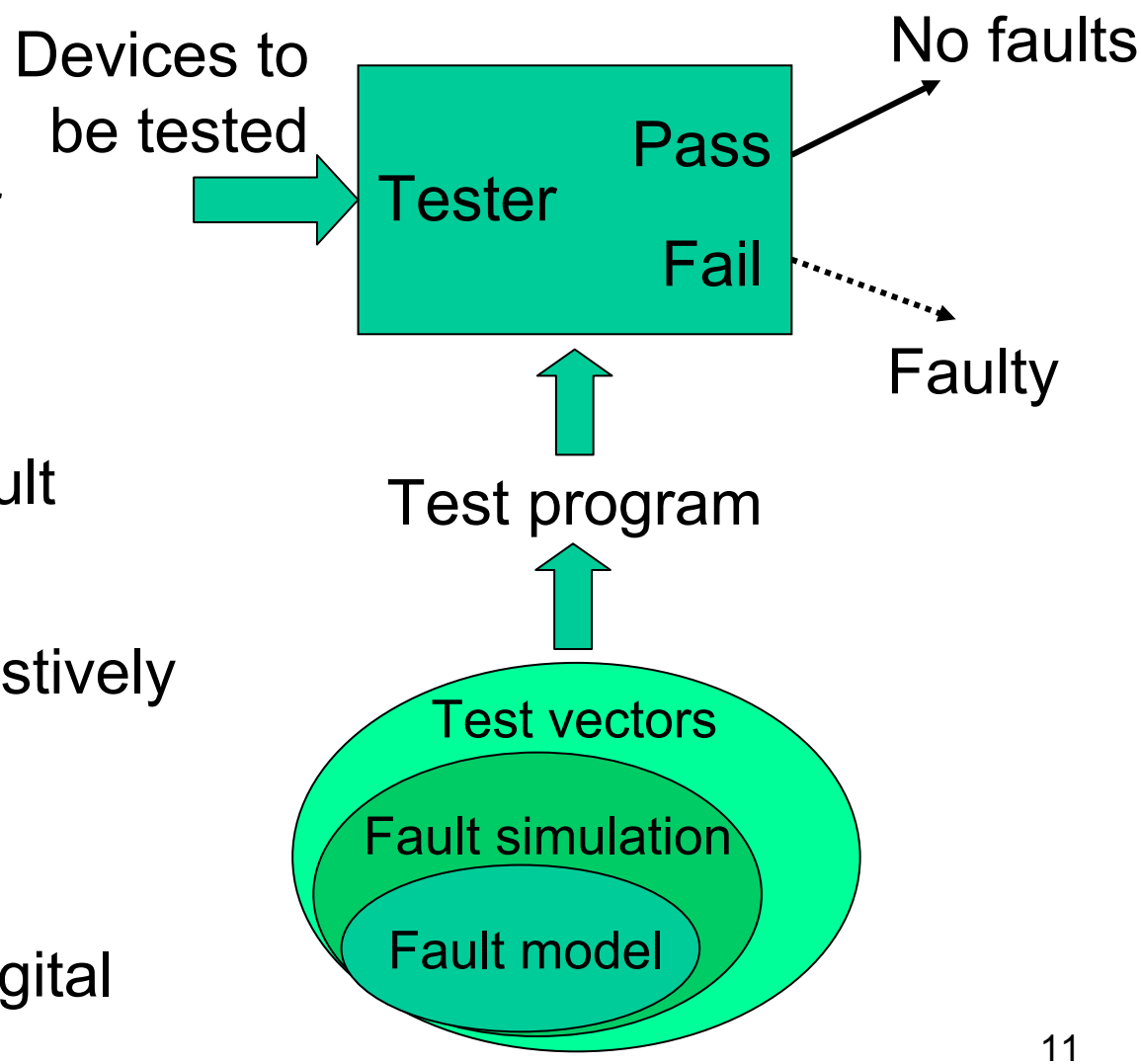


# 3 Structural and functional testing

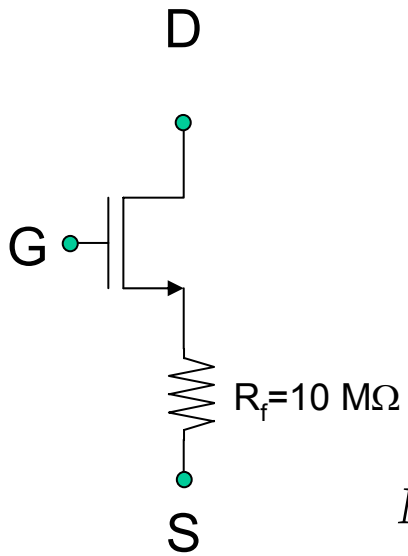
➔ ***Structural testing :***

- Tests targeting structural defects
- Based on the use of fault models
- CAD tools for test generation (ATPG, fault simulation)
- Does not test exhaustively for functionality
- Less expensive test
- Typically used for digital devices

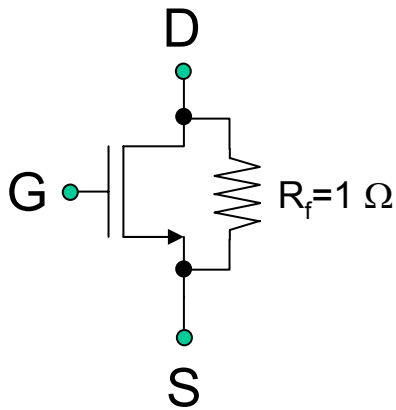


# 3 Structural and functional testing

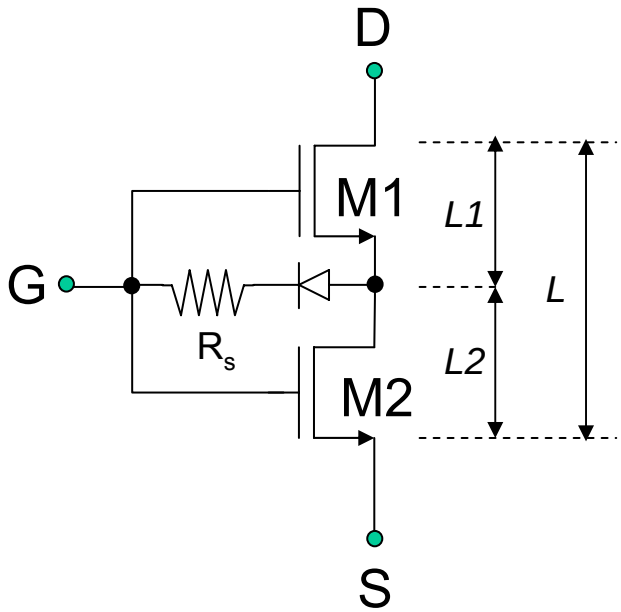
➔ ***Modeling of catastrophic faults : examples at circuit level***



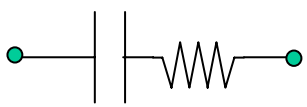

*MOS Source open*



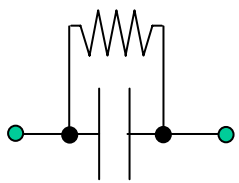

*MOS Drain-Source short*




*MOS Gate-Oxide short*



*Capacitor open*



*Capacitor short*

*Hierarchical faster fault simulation requires the use of higher level (behavioural) fault models*

# 4 Analog DFT/BIST techniques

## ➔ *Standards for IC testing:*

- 1149.1 Standard digital boundary-scan test (1990)
  - Aims to facilitate observability and controllability of IC signals, in particular transforming very difficult PCB testing problems into well structured ones easily solved by software
- 1149.4 Standard Mixed-Signal test bus to be used at device, sub-assembly and system levels (1999)
  - Aims to increase the observability and controllability of mixed-signal designs and support MS-BIST structures
- P1500 Standard test method for embedded cores (working group)
  - Focused on Standardized Core Test Language (CTL) and configurable & scalable test wrapper for easy core access

# 4 Analog DFT/BIST techniques

➔ ***BIST Principle***

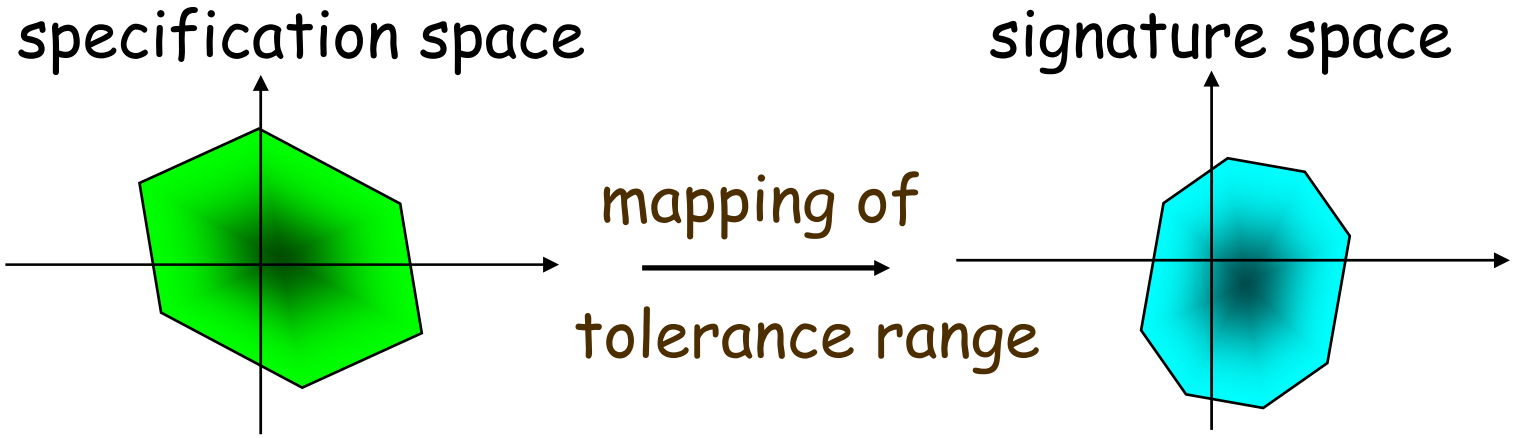
- ❑ On-chip analogue test signal generation
- ❑ On-chip analogue test response analysis

➔ ***Current trends***

- ❑ Enabling each element in an analog chain to be tested independently
- ❑ Reducing requirement for complex functional tests
- ❑ Improving test reuse
- ❑ Exploring the use of digital techniques (as much as possible) for stimulus generation and measurement

# 4 Analog DFT/BIST techniques

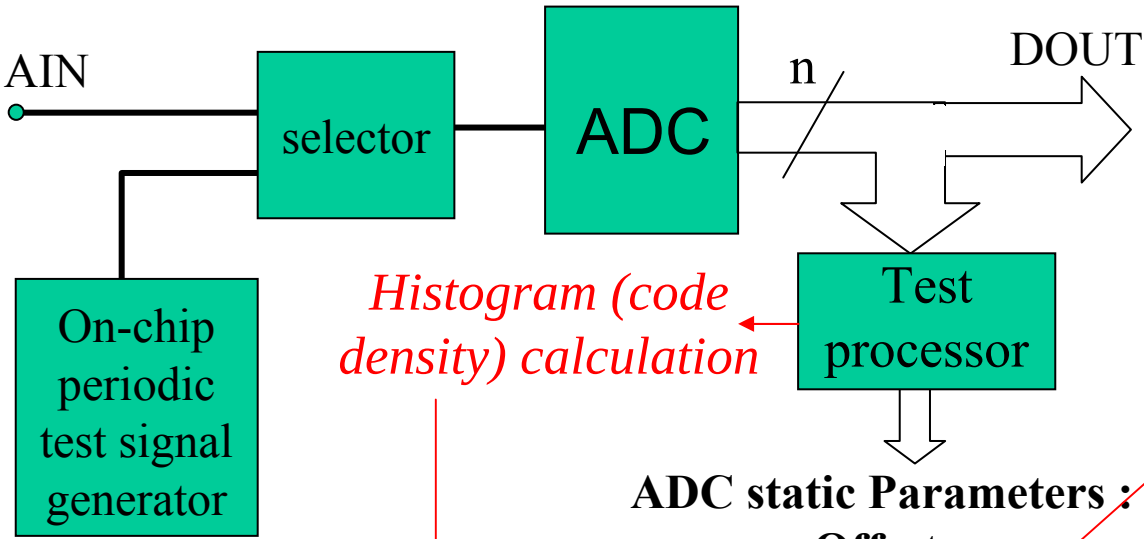
➔ ***BIST relies on accurate mapping of tolerance range***




- Perfect mapping may not be possible
  - Objective: minimize misclassification

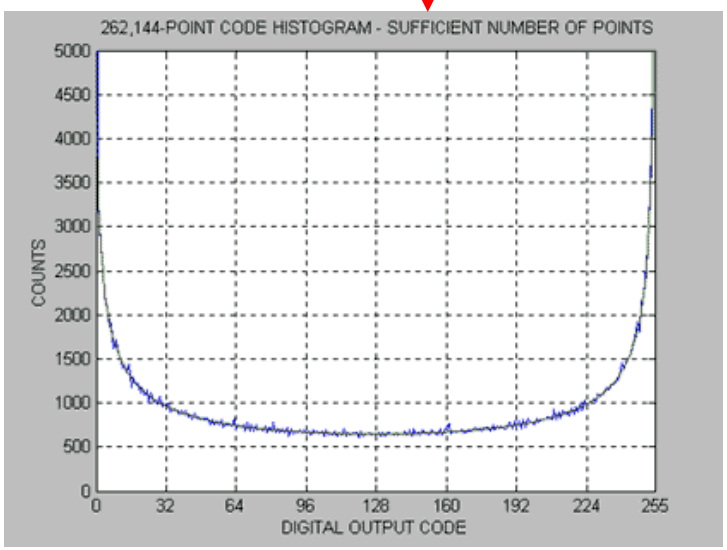
# 4 Analog DFT/BIST techniques

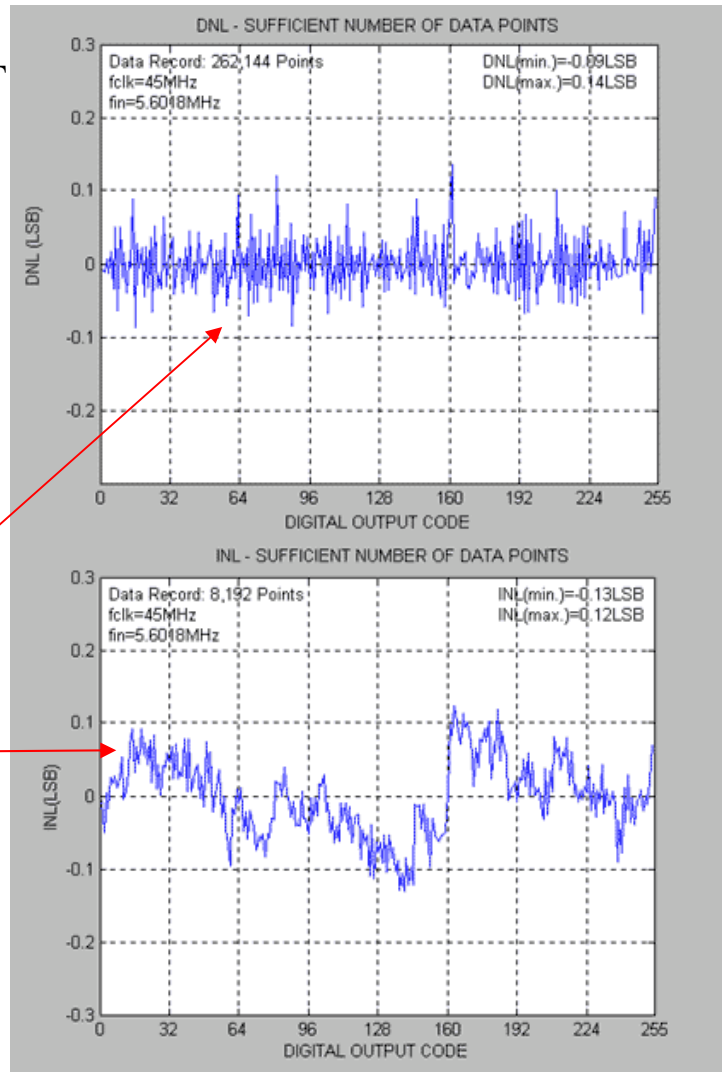
## ➔ Histogram (code density) BIST for ADCs :




**ADC static Parameters :**
**Offset,**
**Gain**
**DNL,**
**INL**

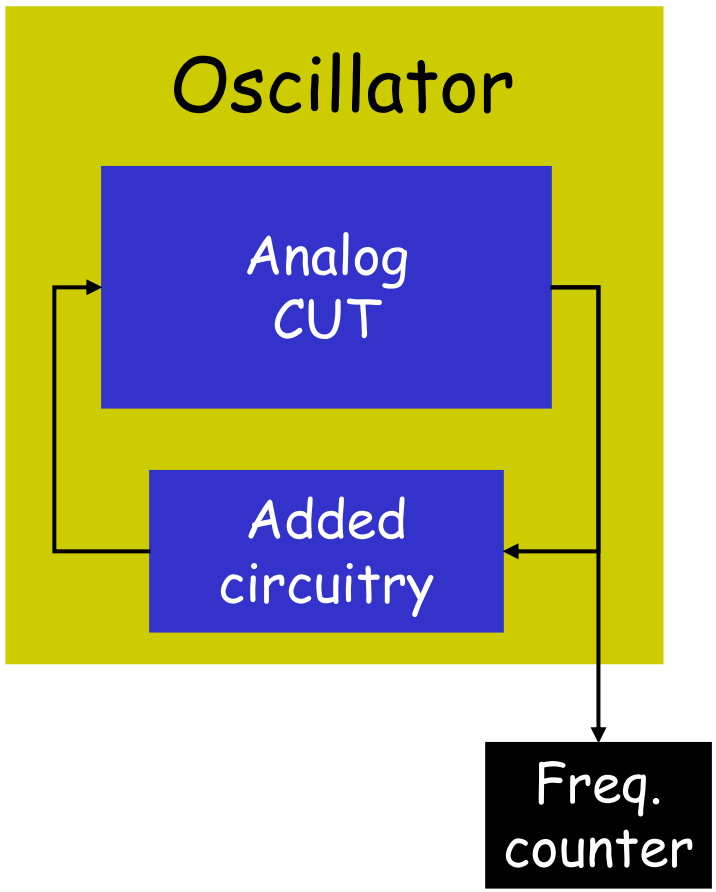
*Obtained by comparison with ideal histogram*



# 4 Analog DFT/BIST techniques

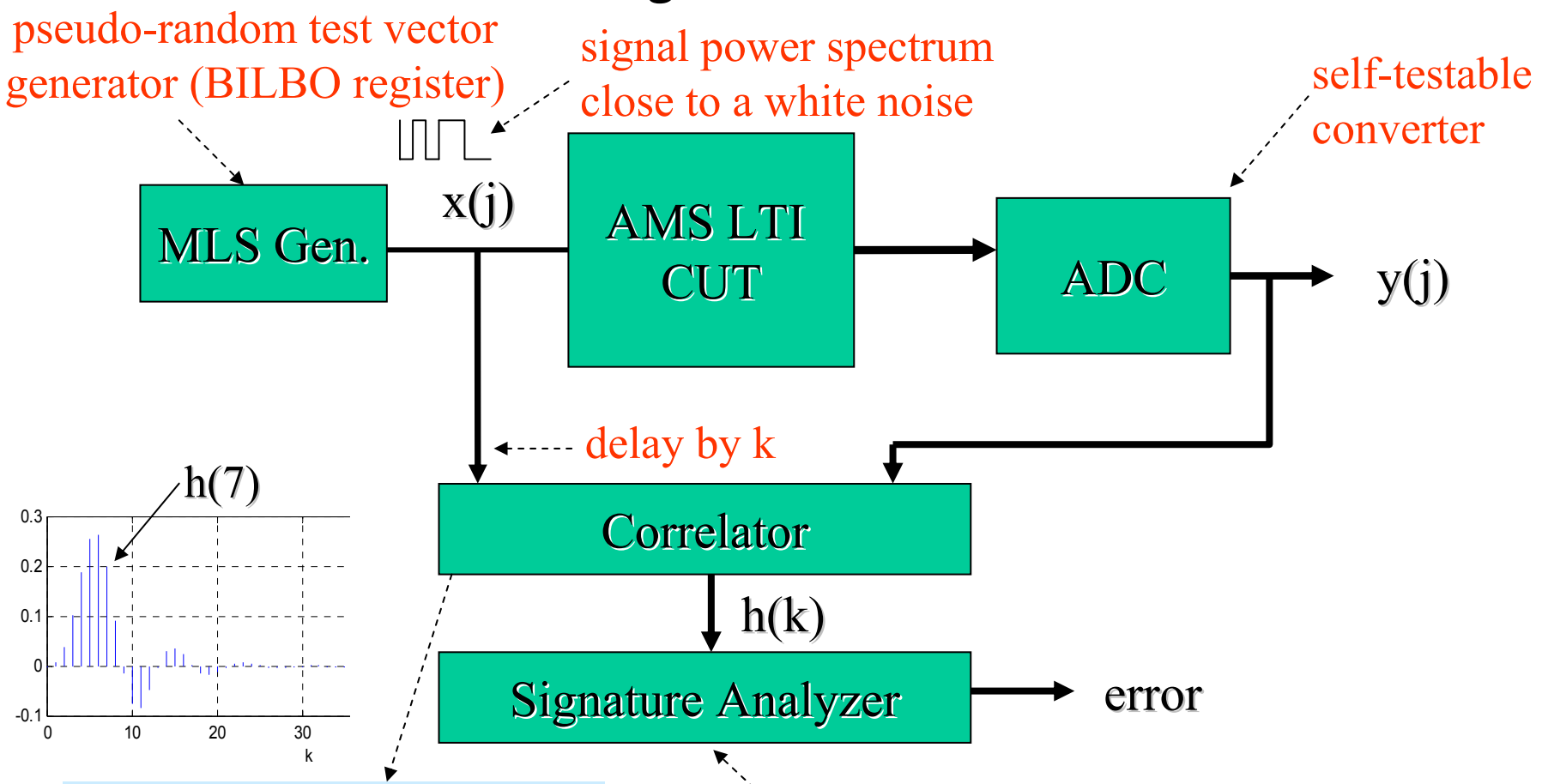
## ➔ Oscillation BIST




- Analog CUT plus added circuitry become an oscillator in test mode
  - Oscillation induced through positive feedback
- Defects cause deviations in
  - Oscillation frequency
  - Oscillation amplitude

# 4 Analog DFT/BIST techniques

## ➔ Pseudo-random testing of LTI circuits :




$$\phi_{xy}(k) = \frac{1}{N} \sum_{j=0}^{N-1} x(j-k)\, y(j)$$

Estimation of the CUT impulse response

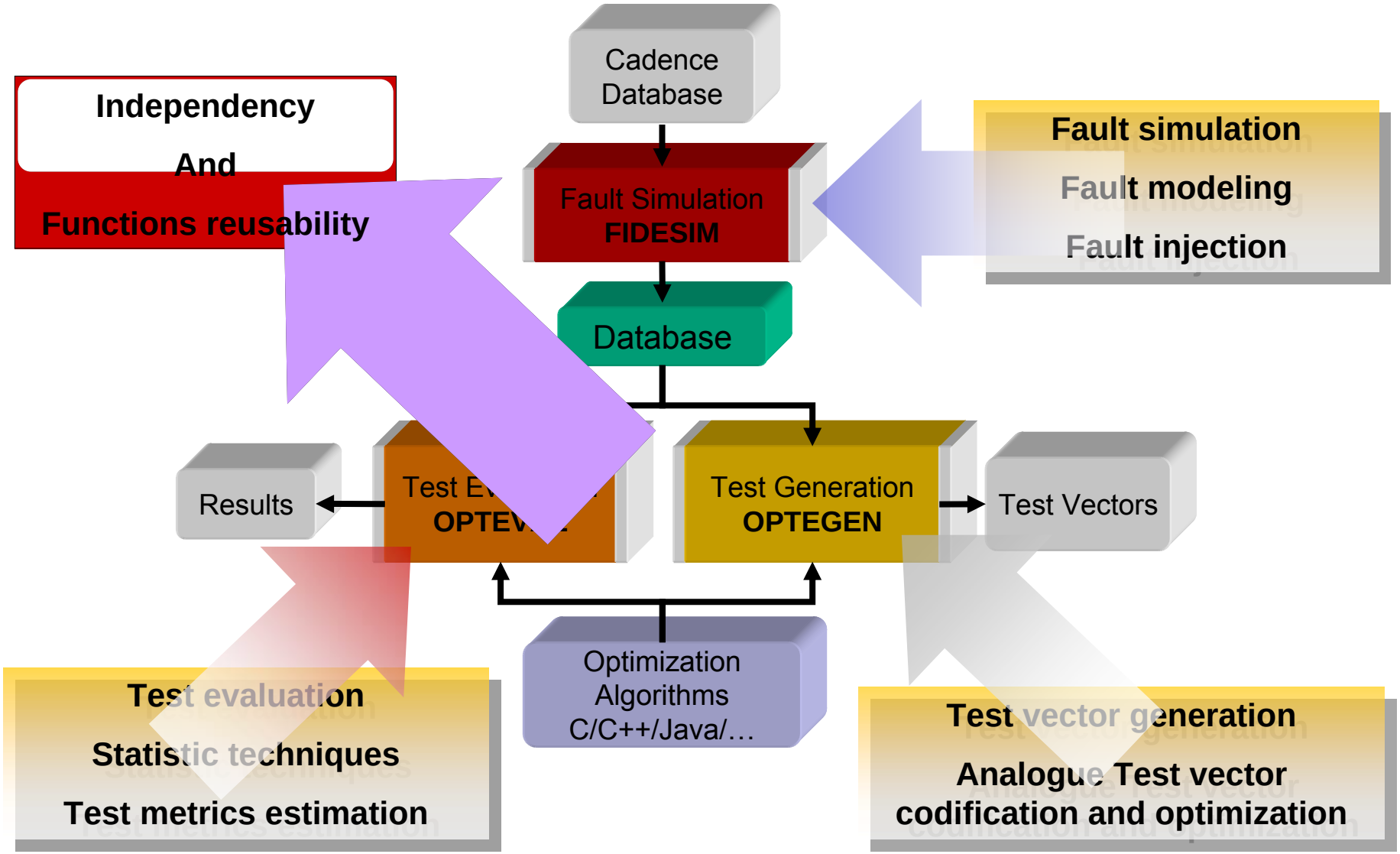
*Mapping the physical parameter space to the IR space; selection of optimal impulse response samples*

# 5 Computer-Aided Test (CAT)

➔ ***Computer aided testing :***

- ❑ Efficient design and test integration by using Computer-Aided Test (CAT) techniques
- ❑ Estimation of test metrics and setting of test limits
- ❑ Efficient determination of test patterns :
  - optimisation of functional tests
  - automatic generation of structural tests (ATPG)
- ❑ ATPG requires :
  - fault modelling techniques for analogue components
  - fault simulation of mixed-signal mixed-domain devices and calculation of fault coverage figures

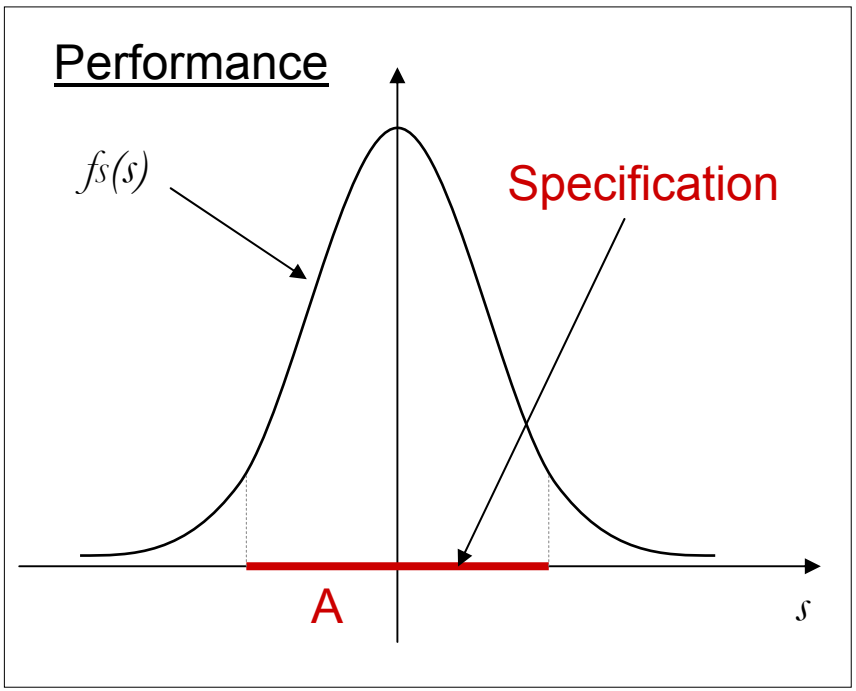
# 5 Computer-Aided Test (CAT)

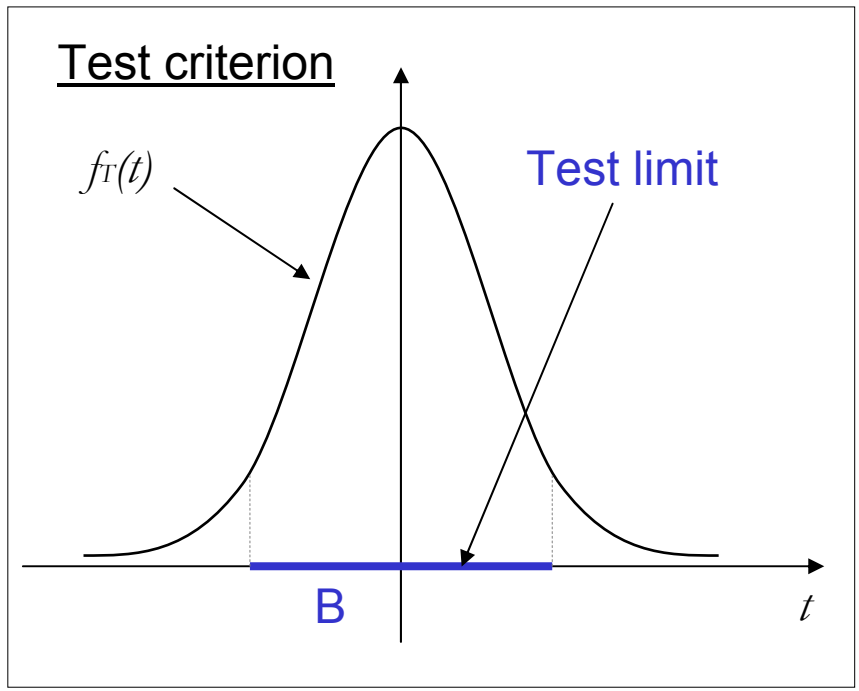


# 5 Computer-Aided Test (CAT)

## ➔ *Estimation of test metrics:*

- It is necessary to work out the relationship between performances and test criteria.
- The metrics are used in order to set test limits.




$P(\text{Functional}) = P(s \in A)$

$P(\text{Faulty}) = 1\text{-}P(\text{Functional}) = 1\text{-}P(s \in A)$

$P(\text{Pass}) = P(t \in B)$

$P(\text{Fail}) = 1\text{-}P(\text{Pass}) = 1\text{-}P(t \in B)$

# 5 Computer-Aided Test (CAT)

## ➔ *Estimation of test metrics:*

- Goal: find the joint Probability Density Function (PDF) between performances and test criteria

*Y = P(Functional)*

$$Y = \int_{A_1} \dots \int_{A_n} f_S(s_1, \dots, s_n)\ ds_1 \dots\ ds_n$$

*$Y_T$ = P(Pass)*

$$Y_T = \int_{B_1} \dots \int_{B_m} f_T(t_1, \dots, t_m)\ dt_1 \dots\ dt_m$$

$$P_{PF} = \int_{A_1} \dots \int_{A_n} \int_{B_1} \dots \int_{B_m} f_{ST}(s_1, \dots, s_n, t_1, \dots, t_m)\ ds_1 \dots\ ds_n\ dt_1 \dots\ dt_m$$

*$Y_C$ = P(Pass/Functional)*

$$Y_C = \frac{P_{PF}}{Y}$$

*D = P(Faulty/Pass)*
*= 1-P(Functional/Pass)*

$$D = 1 - \frac{P_{PF}}{Y_T}$$

*$P_{PF}$ = P(Pass and Functional)*

# 5 Computer-Aided Test (CAT)

➔ ***Estimation of test metrics using a multi-normal PDF between performances and test criteria***

***Multinormal PDF***

$$f(x) = \frac{1}{\sqrt{det(2\pi\Sigma)}} \cdot exp\left[-\frac{(x-\mu)^T\Sigma^{-1}(x-\mu)}{2}\right]$$

$$\Sigma = \begin{pmatrix} \sigma_1^2 & \cdots & COV(X_1, X_N) \\ \vdots & \ddots & \vdots \\ COV(X_N, X_1) & \cdots & \sigma_N^2 \end{pmatrix}$$

$x = (x_1, x_2, \ldots, x_N)$

$\mu = (\mu_1, \mu_2, \ldots, \mu_N)$

$$COV(X_1, X_2) = \frac{\sum_{i=1}^{N} X_1^i \cdot X_2^i}{N} - \mu_1\mu_2$$

$$P(A) = \frac{1}{\sqrt{det(2\pi\Sigma)}} \int_{A_1} \cdots \int_{A_p} exp\left[-\frac{(x-\mu)^T\Sigma^{-1}(x-\mu)}{2}\right] dx_1 dx_2 \cdots dx_p$$

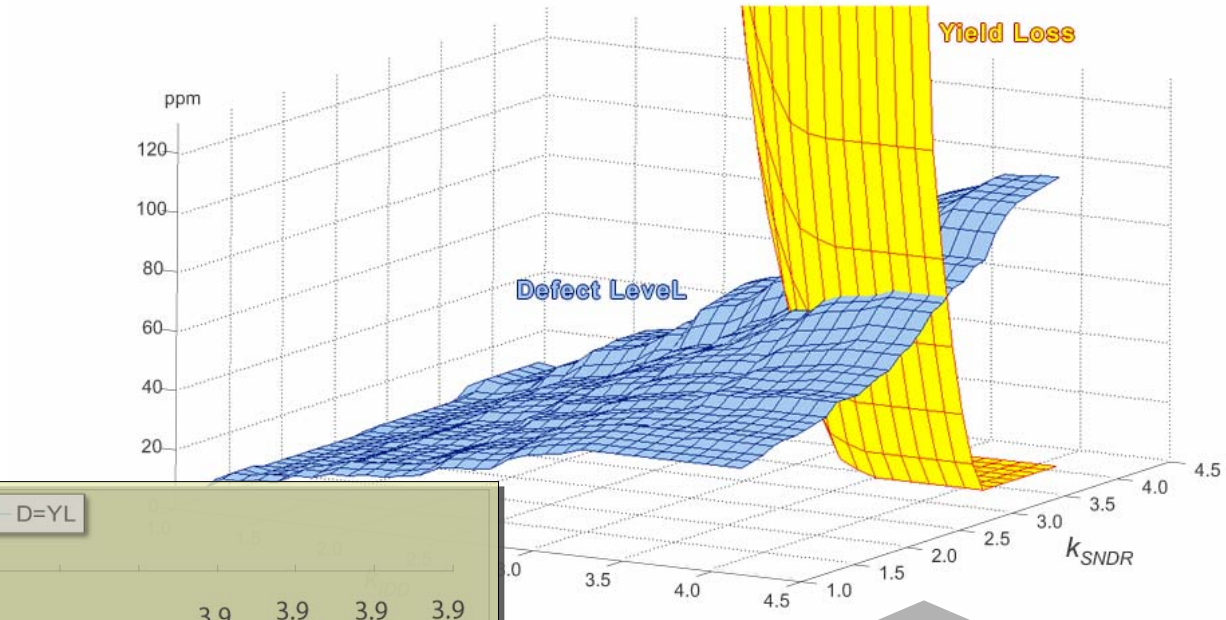
Run 1000 Monte Carlo circuit simulations → Calculate multinormal PDF parameters ($\mu$ and $\Sigma$) → Generate millions of circuit samples from the multinormal law (using Matlab, R, …)

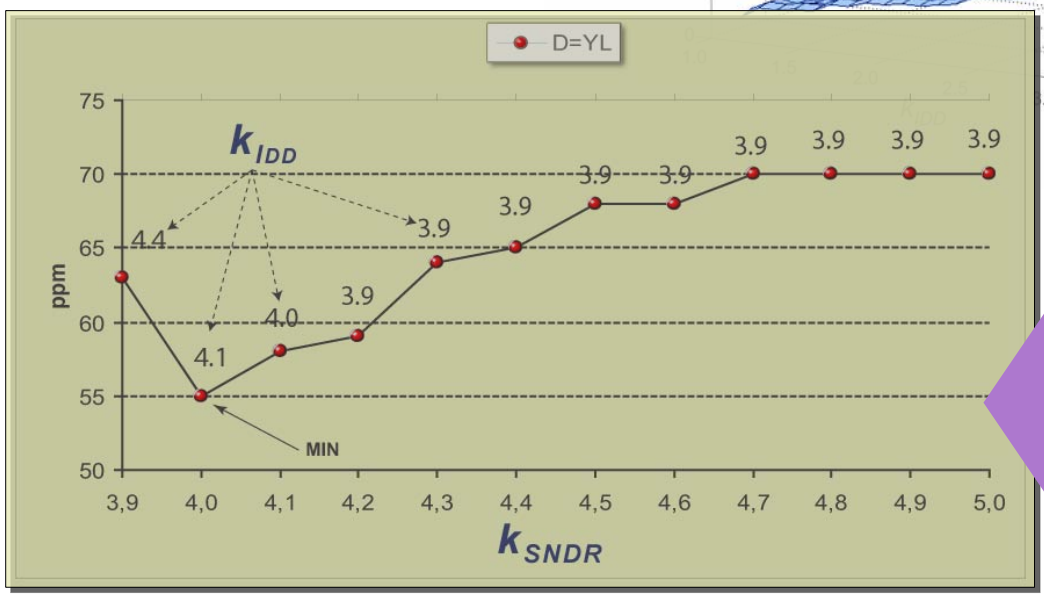
# 5 Computer-Aided Test (CAT)

➔ ***Setting test limits as a function of test metrics:***

SNDR
[ μ-4.0σ , μ+4.0σ ]

IDD
[ μ-4.1σ , μ+4.1σ ]

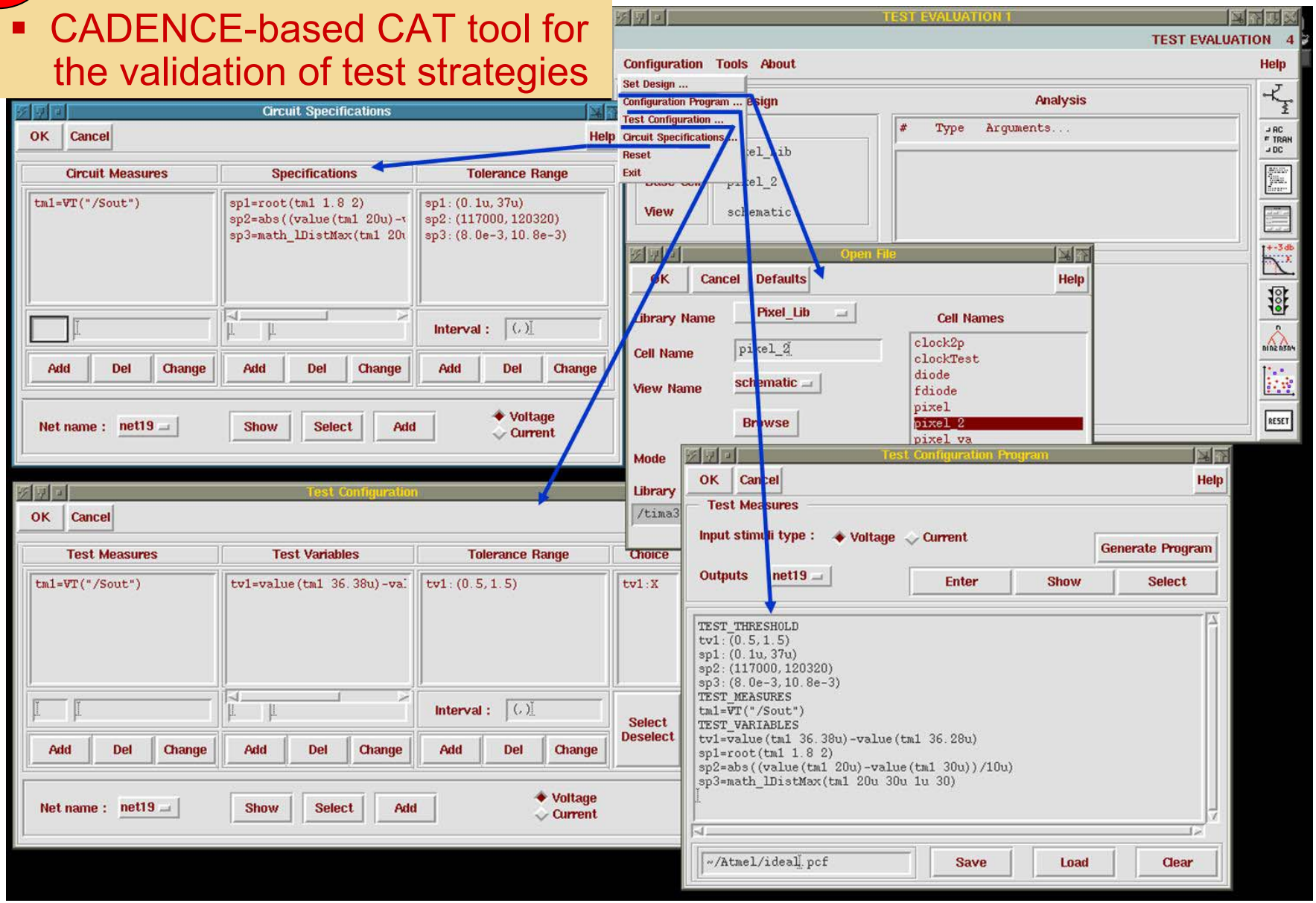



**55 ppm**

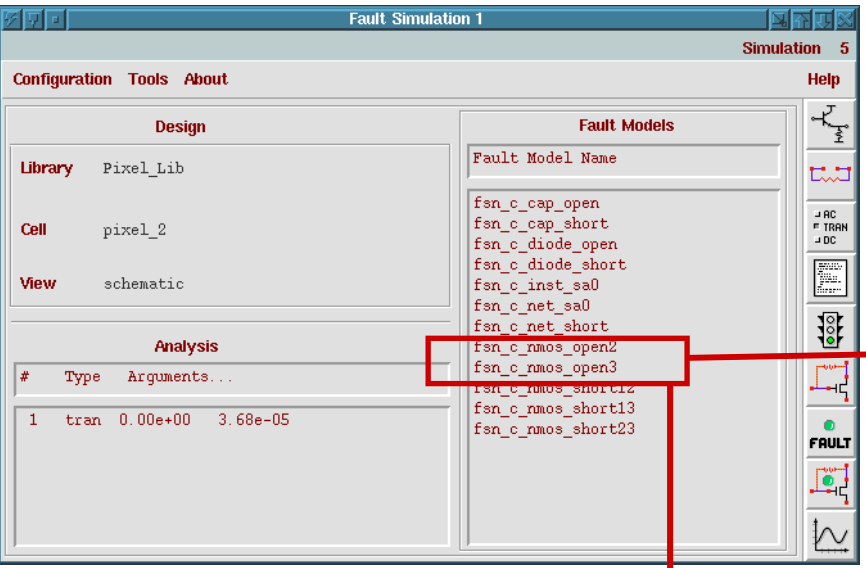
# 5 Computer-Aided Test (CAT)

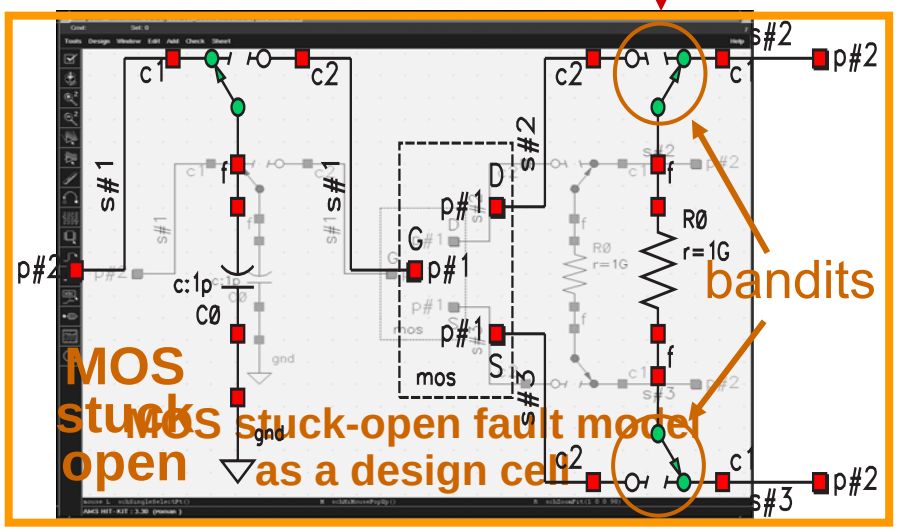
- CADENCE-based CAT tool for the validation of test strategies




**Fault modelling, injection and simulation tool**

# 5 Computer-Aided Test (CAT)



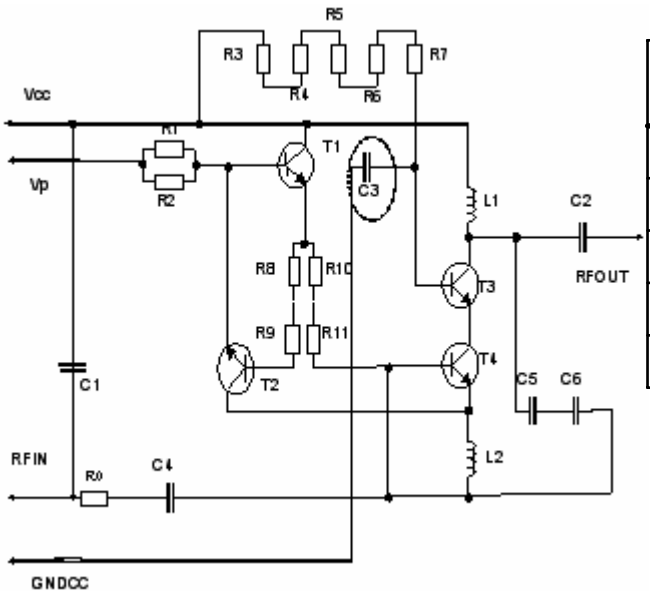

```
/* Code sample for the fault model:
 * "MOS transistor stuck open" */
;# Design Under Test CellView
dsc_DUT=dbOpenCellViewByType("FAULT_DEMO"
        "THPixel" "schematic" nil "r")
;# Finding locations to inject faults
MOS=setof(X dsc_DUT->instances
         X->cellName=="nmos4" ||
         X->cellName=="pmos4")
;# List of all possible locations
LOC=dscGetInstSegsOnPins(MOS
         list("G" "D" "S"))
;# Specifying the current fault model
dsc_CURRENT_FAULT=list("FAULT_DEMO"
         "mosStuckOpen")
;# Building the fault scenario
LOCp1=dscLabelLocationsAs("concurrent" LOC)
LOCs=dscLabelLocationsAs("sequential"
         List(LOC LOCp1))

Dsc_FAULT_SCENARIO=dscBuildScenario(LOCs)
```

## Fault modelling & fault injection

- Integrated in CADENCE

# 5 Computer-Aided Test (CAT)

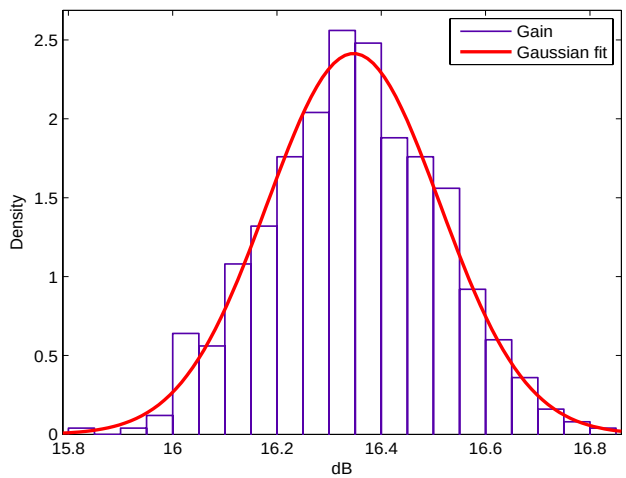
Test evaluation for an 0.25 µm BiCMOS ST Microelectronics LNA amplifier




| Performances @2.2GHz | µ | σ |
|---|---|---|
| NF (dB) | 1.6 | 0.08 |
| $S_{11}$ (dB) | -12.4 | 0.46 |
| $S_{12}$ (dB) | -21.9 | 0.19 |
| $S_{21}$ (dB) | 16.3 | 0.17 |
| $S_{22}$ (dB) | -15.5 | 1.28 |

| Test measurements | µ | σ |
|---|---|---|
| $I_{rms}$ (mA) | 5.2 | 0.02 |
| $I_{pp}$ (mA) | 3.6 | 0.14 |
| $V_{rms}$ (mV) | 44.8 | 0.89 |
| $V_{pp}$ (mV) | 129.3 | 2.29 |
| $I_0$ (mA) | 15.5 | 0.05 |
| $Z_1$ (Ω) @2.2GHz | 64.0 | 1.71 |
| $Z_2$ (Ω) @2.2GHz | 69.1 | 2.72 |

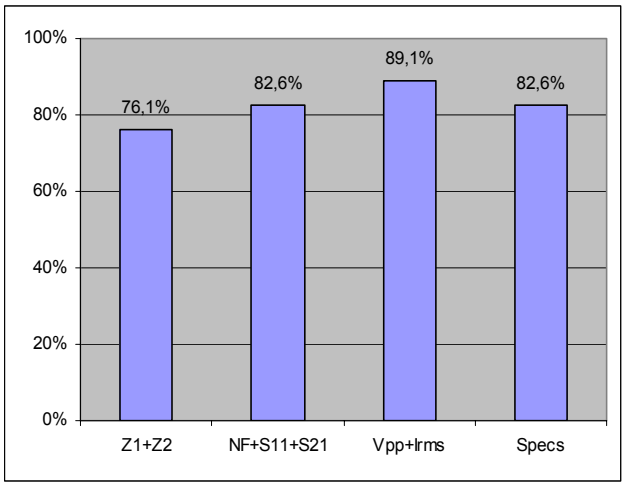
| Test Limits | Min | Max |
|---|---|---|
| $I_{rms}$ (mA) | 5.1 | 5.3 |
| $I_{pp}$ (mA) | 3.1 | 4.1 |
| $V_{rms}$ (mV) | 41.6 | 48.0 |
| $V_{pp}$ (mV) | 121.0 | 137.6 |
| $I_0$ (mA) | 15.3 | 15.7 |
| $Z_1$ (Ω) @2.2GHz | 57.9 | 70.1 |
| $Z_2$ (Ω) @2.2GHz | 59.4 | 78.8 |




LNA Gain Distribution with Gaussian fitting

# 5 Computer-Aided Test (CAT)

## Test evaluation for an LNA amplifier




Fault coverage evaluation for catastrophic faults considering performances (specs) and test measurements: LNA output voltage (Vpp) and current consumption (Irms) achieve high fault coverage than circuit performances

| Test N° | Test criteria | Defects | F | Y | YT | Yc | D |
|---|---|---|---|---|---|---|---|
| 1 | $I_{rms}$ | 1, 3, 6 | 9.2% | 89.9% | 99.0% | 100% | 9.2% |
| 2 | $I_{pp}$ | None | 0% | 89.9% | 100% | 100% | 10.0% |
| 3 | $V_{rms}$ | 1, 3, 6, 8, 9 | 58.7% | 89.9% | 92.1% | 98.0% | 4.3% |
| 4 | $V_{pp}$ | 1, 3, 6, 8, 9 | 60.6% | 89.9% | 88.9% | 94.7% | 4.1% |
| 5 | $I_0$ | 3, 6 | 12.8% | 89.9% | 98.6% | 100% | 8.8% |
| 6 | $Z_1$ | 1, 3, 6, 7, 8, 9 | 63.5% | 89.9% | 80.4% | 86.0% | 3.8% |
| 7 | $Z_2$ | 1, 3, 6, 7, 8, 9 | 16.9% | 89.9% | 94.4% | 96.1% | 8.4% |
| 8 | All test criteria | 1, 3 ,6, 7, 8, 9 | 64.2% | 89.9% | 77.3% | 82.7% | 3.7% |

Fault coverage for most probable single parametric faults has been considered. Measuring of input impedance (Z1) is necessary in addition to Vpp and Irms to have at least partial coverage of all faults

# 6 Conclusions

- Test techniques for digital circuits (including DFT, BIST) are today well established.
- For analogue and mixed-signal circuits, much research is still required.
- The nature of analogue signals, the variety of analogue circuits and performances, the difficulty to provide fault models with wide acceptance, the difficulty to evaluate the quality of the tests, make mixed-signal testing a difficult topic.
- The basic analogue test approaches have been presented and DFT/BIST techniques introduced.
- Analogue testing techniques are largely multidisciplinary: techniques from signal processing, statistics, optimisation, machine learning, … are required.