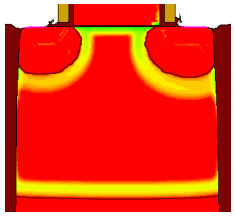
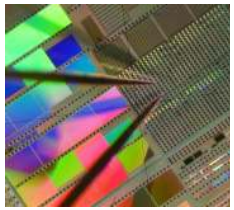
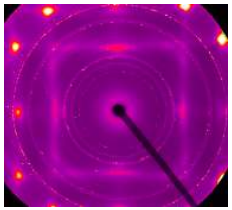
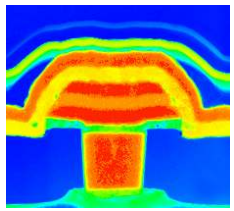


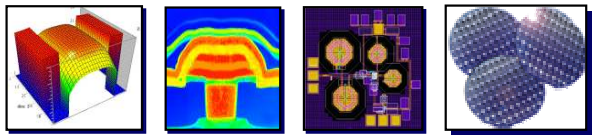




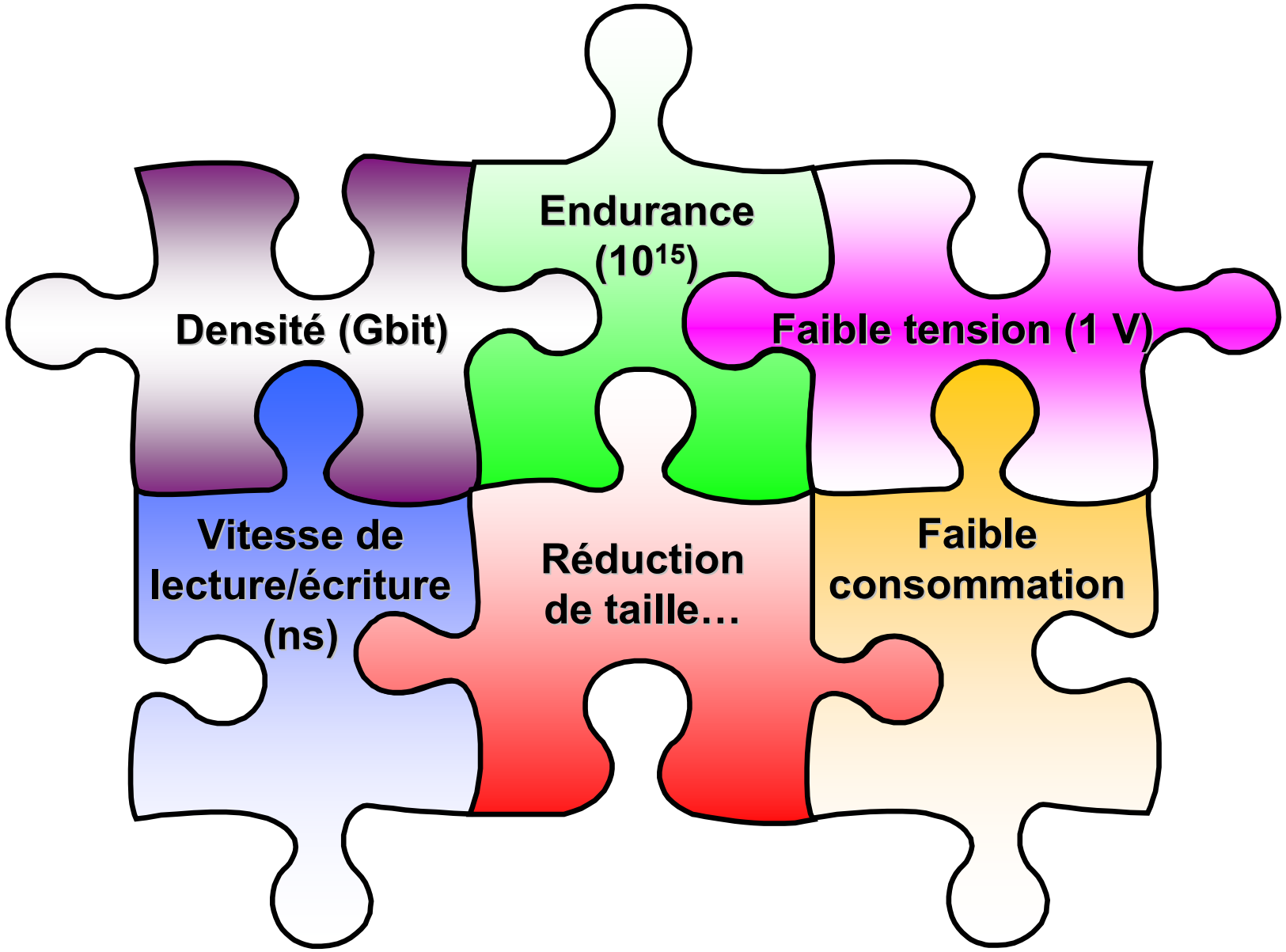


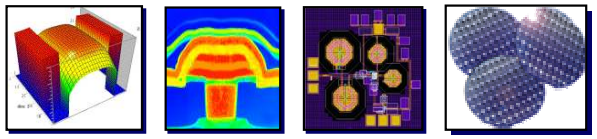
Vers des "nano-mémoires" en microélectronique…

Ch. Muller
Laboratoire Matériaux et Microélectronique de Provence (L2MP), UMR CNRS 6137
Bâtiment R – Université du Sud Toulon Var – BP 20132
F–83957 La Garde Cedex
e-mail : christophe.muller@l2mp.fr



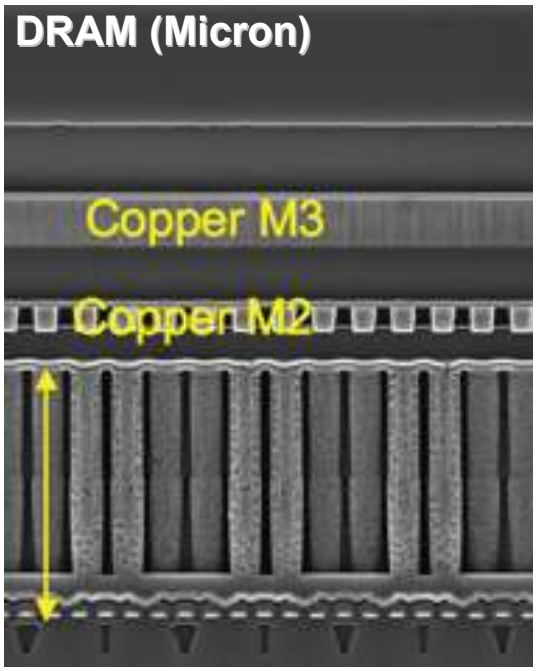
Quelle est la mémoire idéale ?

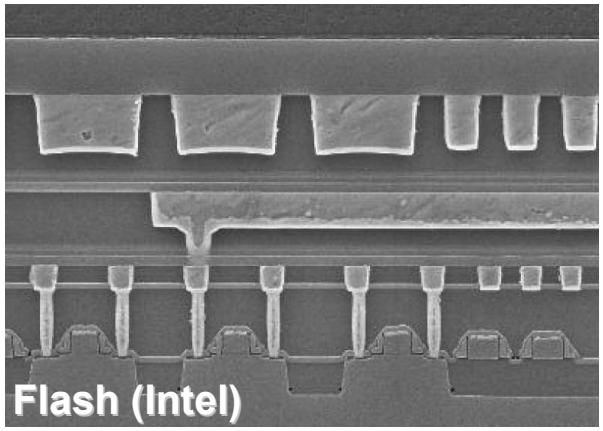


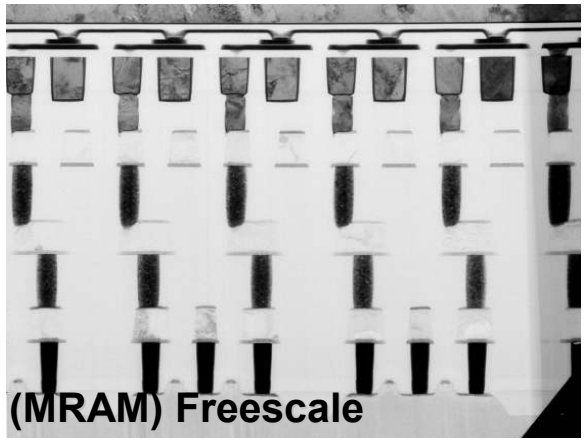


Classification

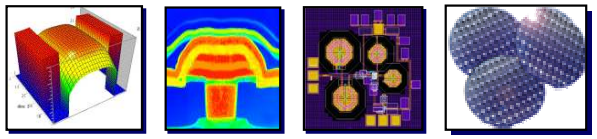
Mémoires

- **Volatiles**
  - 

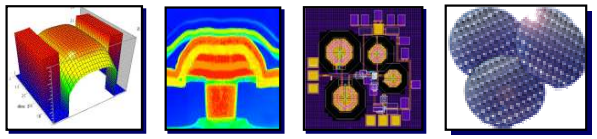
  - **SRAM**
    DRAM
- **Non volatiles**
  - **Stockage de charge**
    - 

    - **EEPROM**
      Flash
      Nano–Si
  - **Résistances high/low**
    - 

    - **MRAM**
      PCRAM
      ReRAM

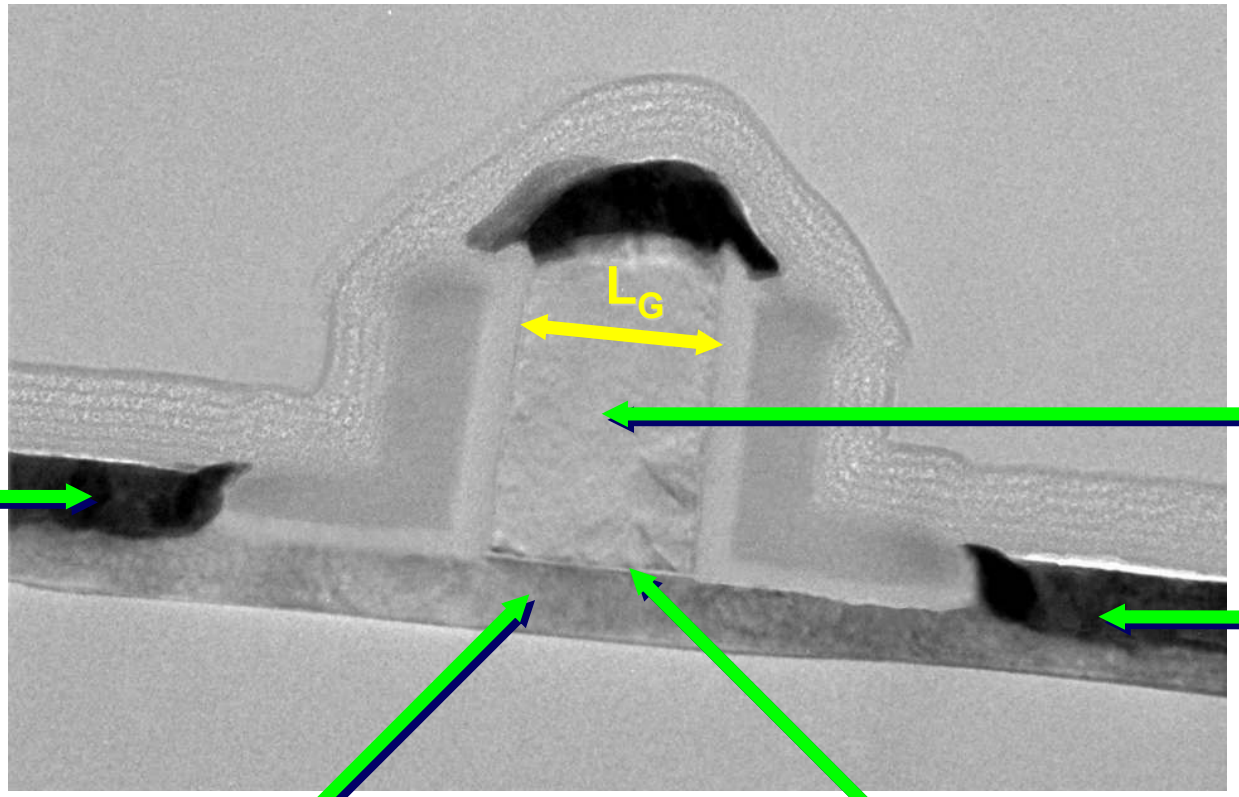


Evolution des technologie MOS pour les mémoires volatiles SRAM et DRAM

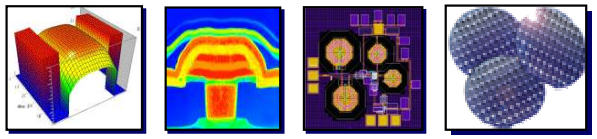


Transistor MOS = brique élémentaire

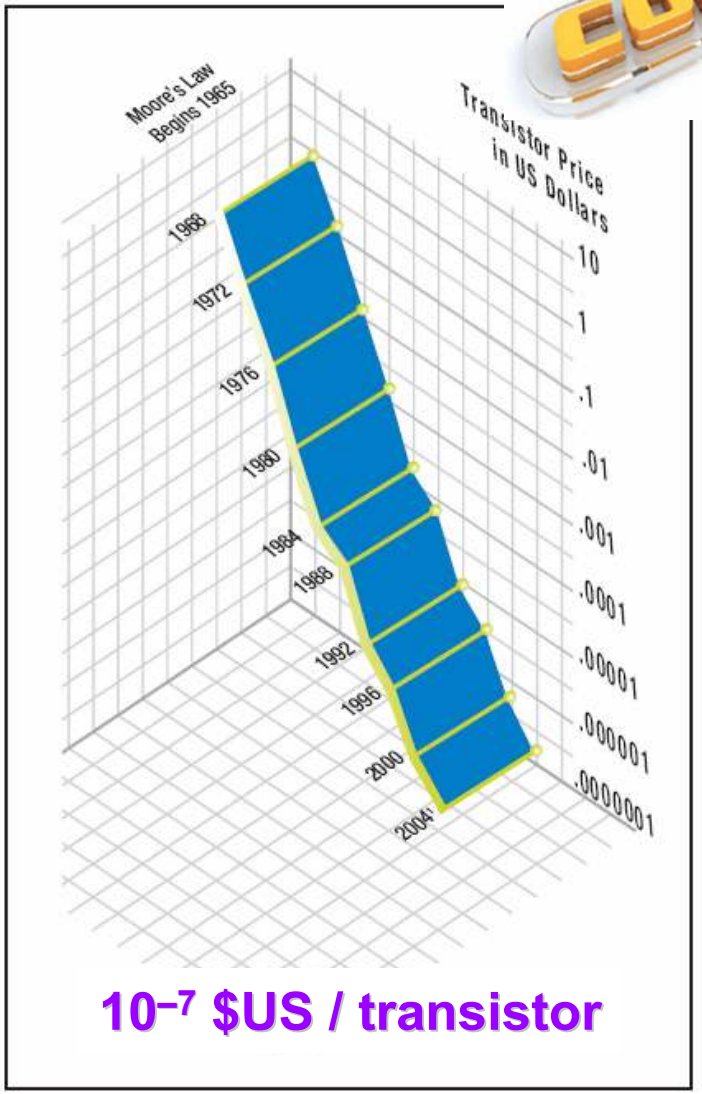
MOSFET = Metal – Oxide – Semiconductor Field Effect Transistor



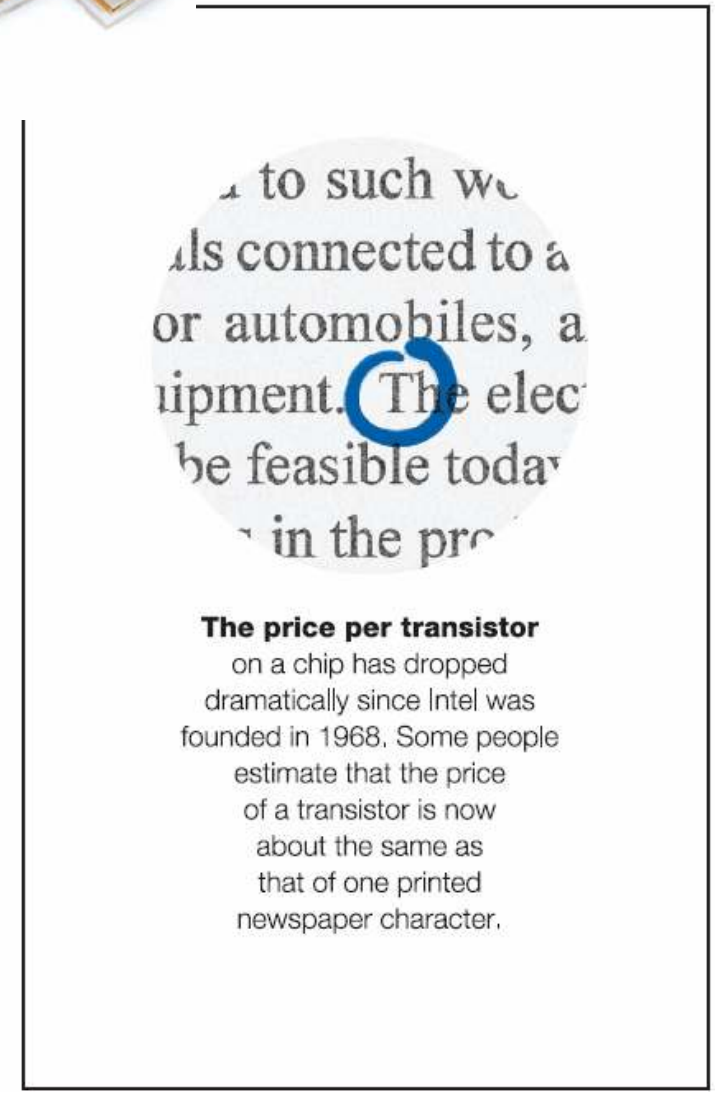
Vitesse de la technologie $\propto 1 / L_G^2$



Le prix baisse aussi vite que la taille !



10^{-7} $US / transistor



to such we
ils connected to a
or automobiles, a
uipment. The elec
be feasible toda
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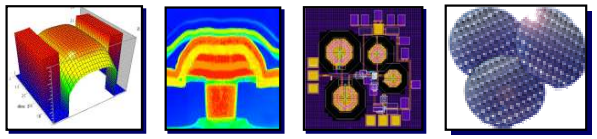
The price per transistor on a chip has dropped dramatically since Intel was founded in 1968. Some people estimate that the price of a transistor is now about the same as that of one printed newspaper character.

www.intel.com



Roadmap du MOSFET selon Intel

90 nm
2003

65 nm
2005

45 nm
2007

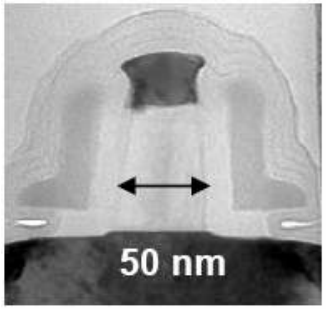
32 nm
2009

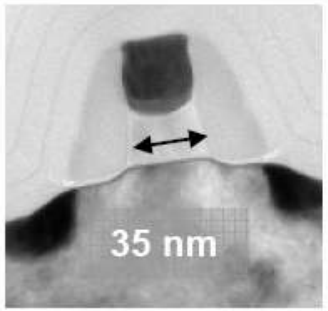
> 2011

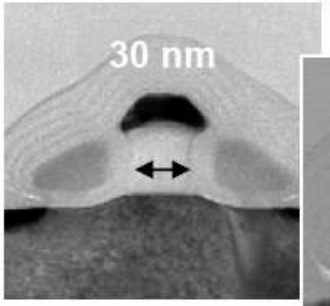
Production

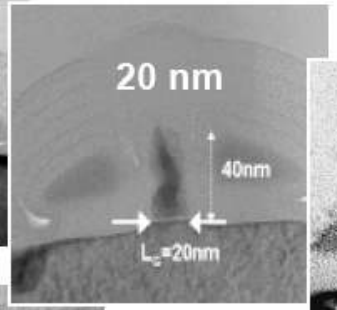
Développement

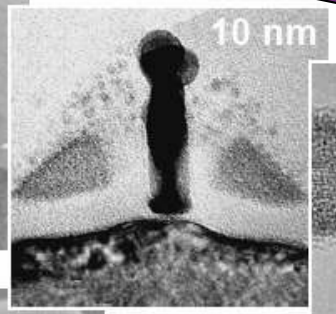
Recherche

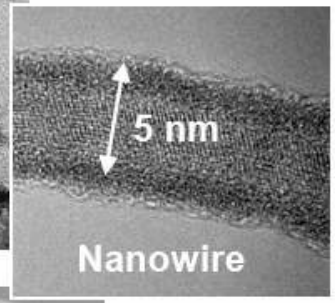


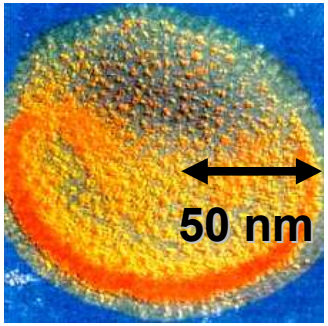




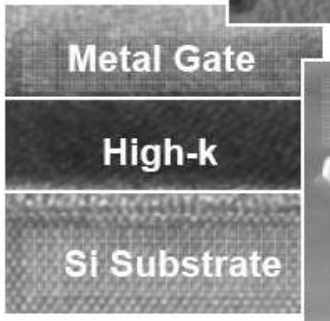


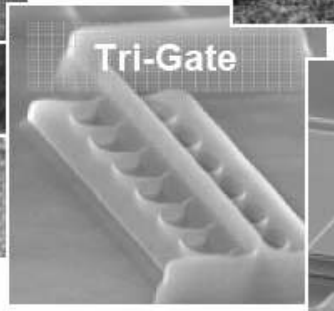


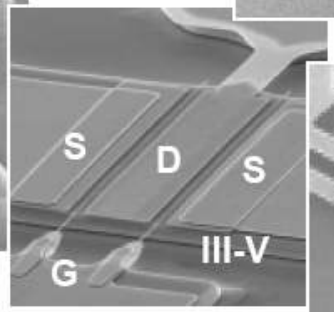


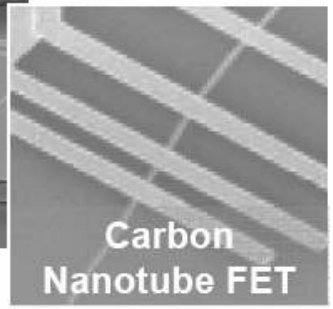


Virus de la grippe

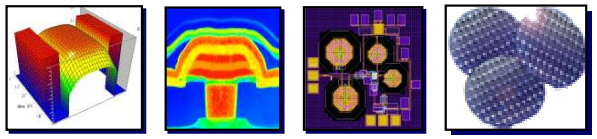








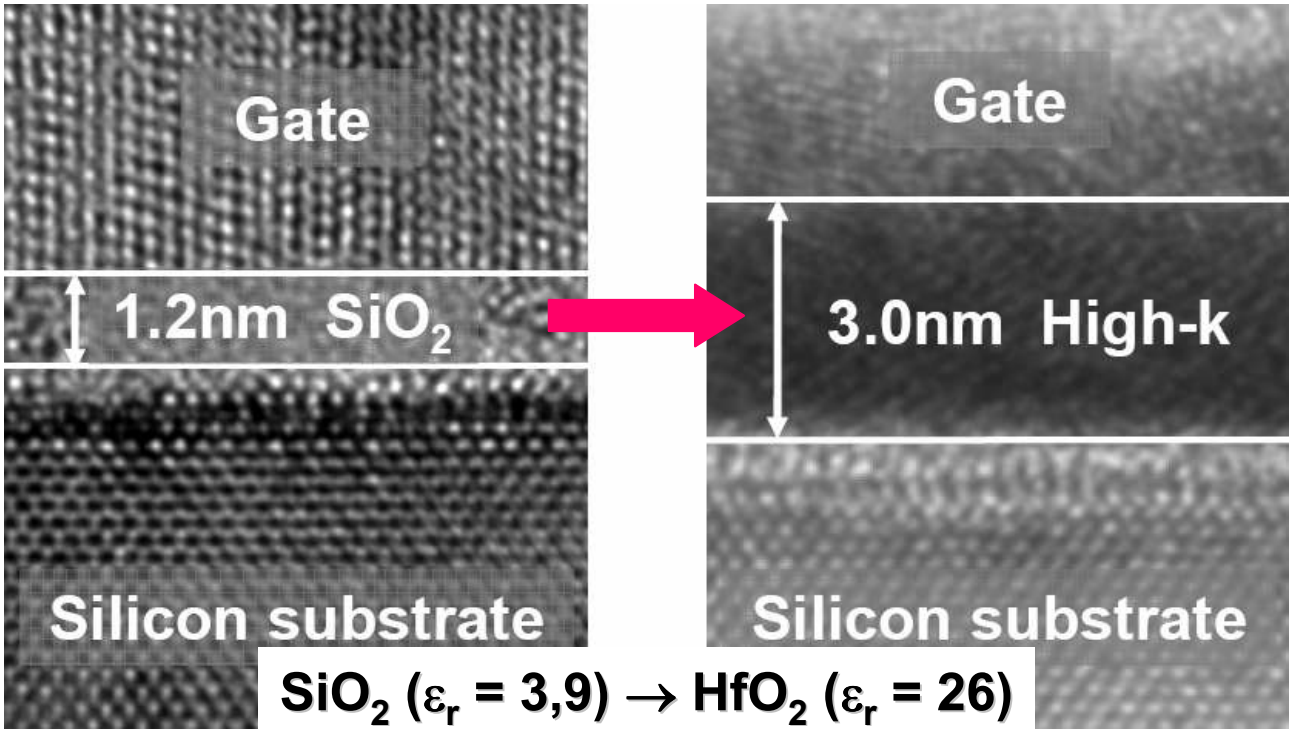
"Intel's Silicon R&D Pipeline", Intel Developer Forum
Mark Bohr, Intel Senior Fellow



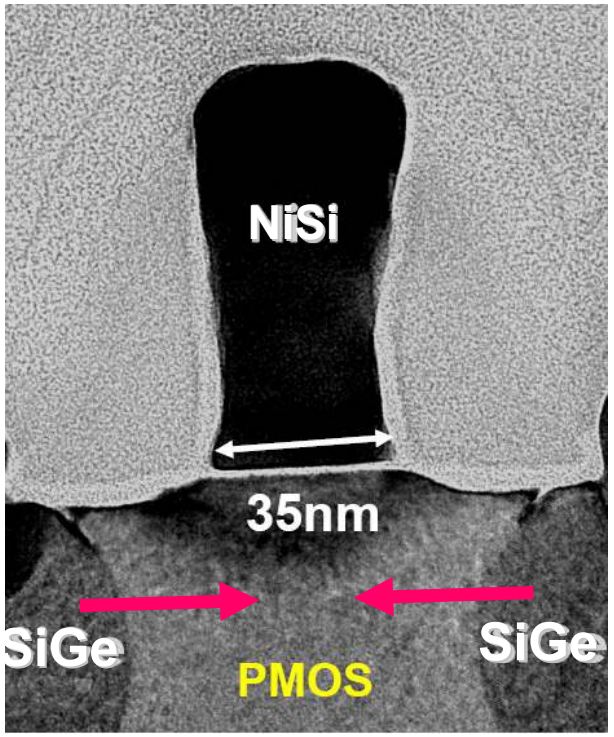
Intégration de "nouveaux" matériaux

$$I_D^{Sat} \propto \frac{W}{L} \times \boxed{\mu \times Q_{inv}}$$

Courant à saturation dans un canal de largeur W et de longueur L



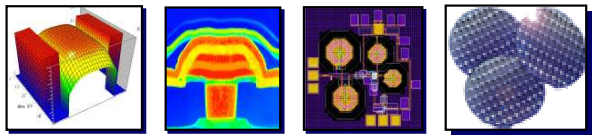
SiO_2 (ε_r = 3,9) → HfO_2 (ε_r = 26)



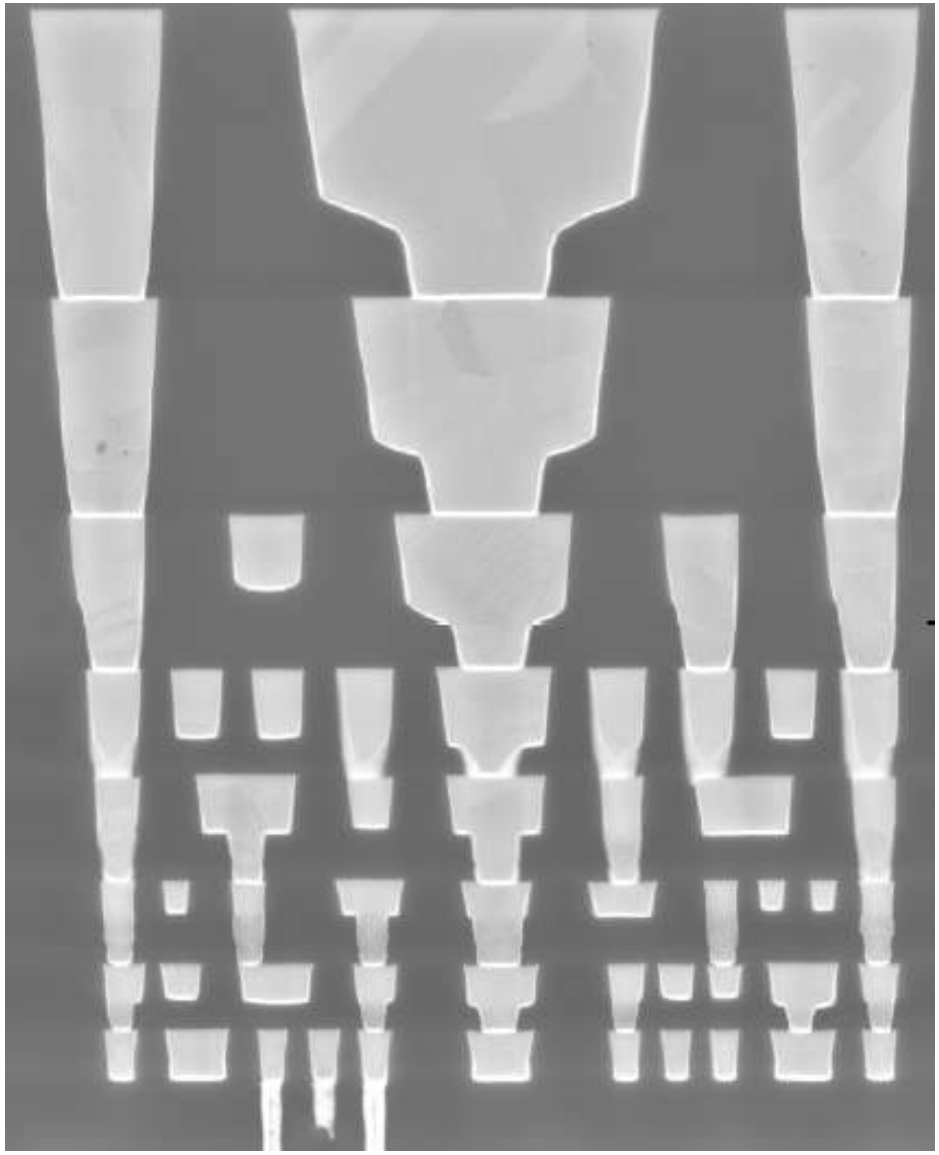
SiO_2 → Diélectrique "high-κ" (Q_{inv})

Poly–Si → NiSi (Q_{inv})
Si → Canal contraint (μ)

"Intel's Silicon R&D Pipeline", Intel Developer Forum
Mark Bohr, Intel Senior Fellow

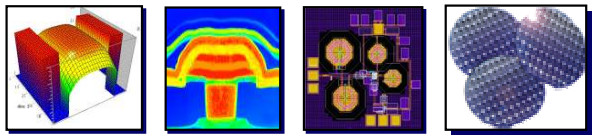


Idem pour les interconnexions



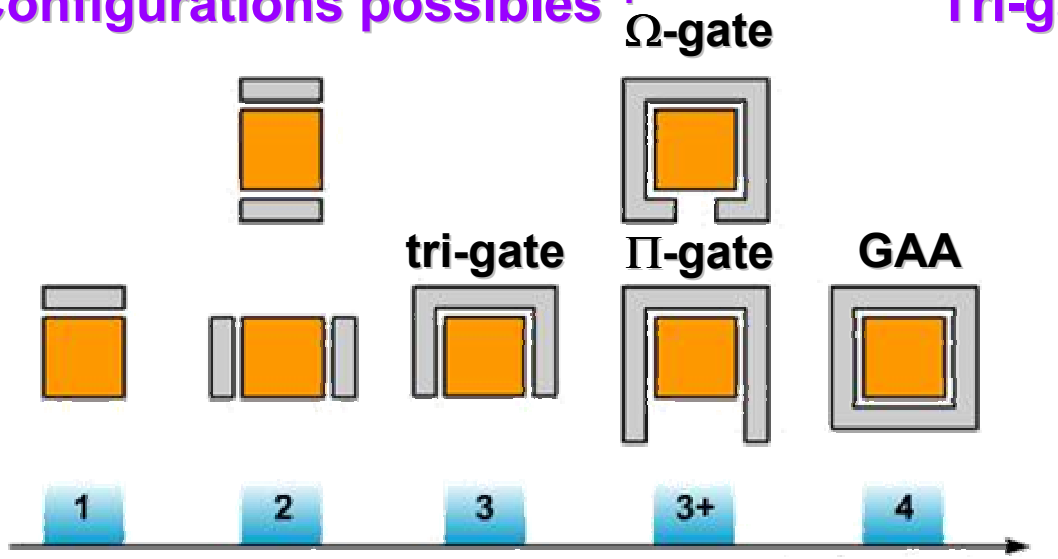
- Technologie 65 nm (L_G = 35 nm)
  - 8 niveaux de métal
  - Passage Al → Cu
    - ✓ ↓ Résistivité
    - ✓ ↓ Electromigration
    - ✓ Barrière de diffusion (migration du cuivre)
  - Matériaux "low-κ" (CDO = Carbon Doped Oxide)
    - ✓ ↓ Capacités parasites entre les lignes d'interconnexion
    - ✓ ↑ Performances
    - ✓ ↓ Consommation

"Intel's Silicon R&D Pipeline", Intel Developer Forum
Mark Bohr, Intel Senior Fellow

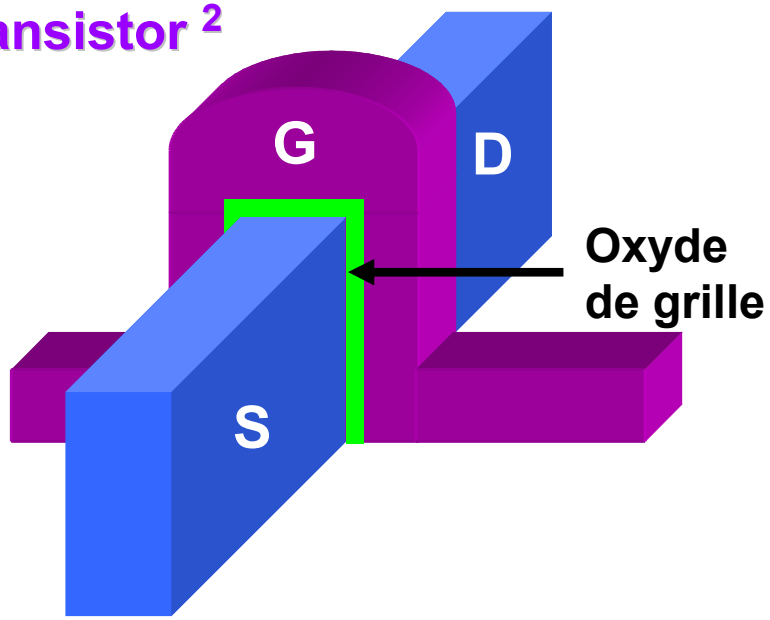


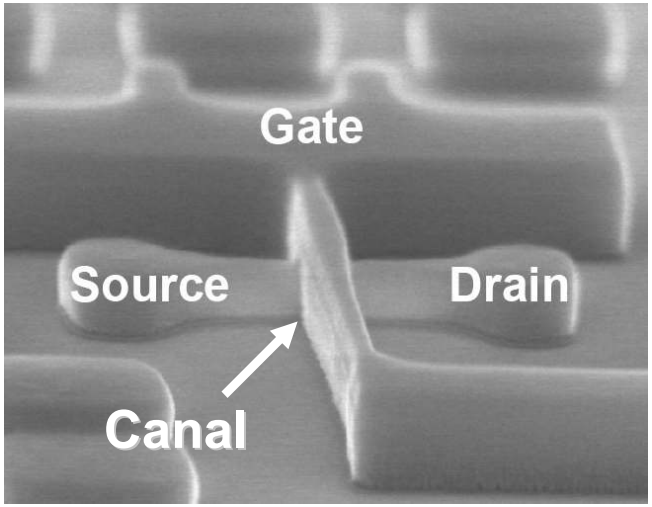
Vers des dispositifs multi-grilles…

Configurations possibles [1]

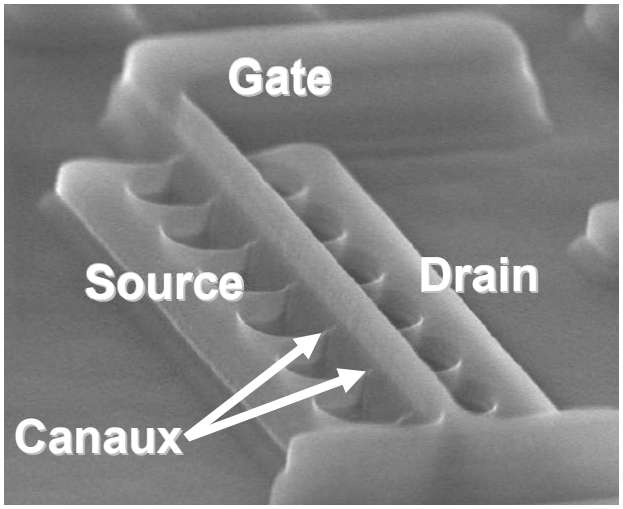


Tri-gate transistor [2]

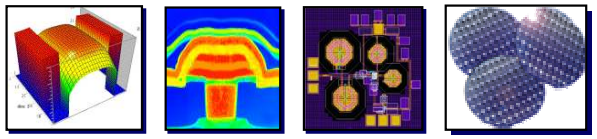




Single-L_G → Multi-L_G

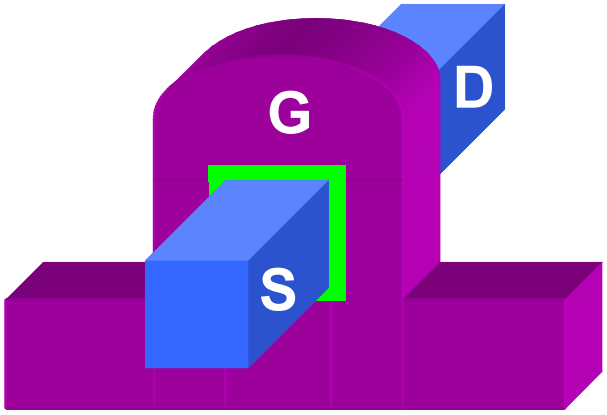


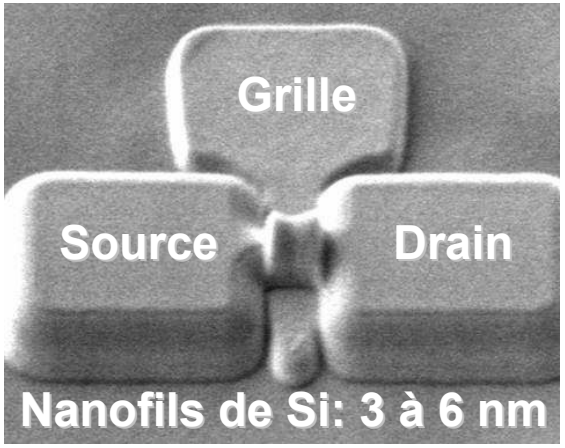
[1] Autran *et al.*, Revue de l'Electricité et de l'Electronique, à paraître, 2007
[2] Kavalieros *et al.* (Intel), VLSI 2006



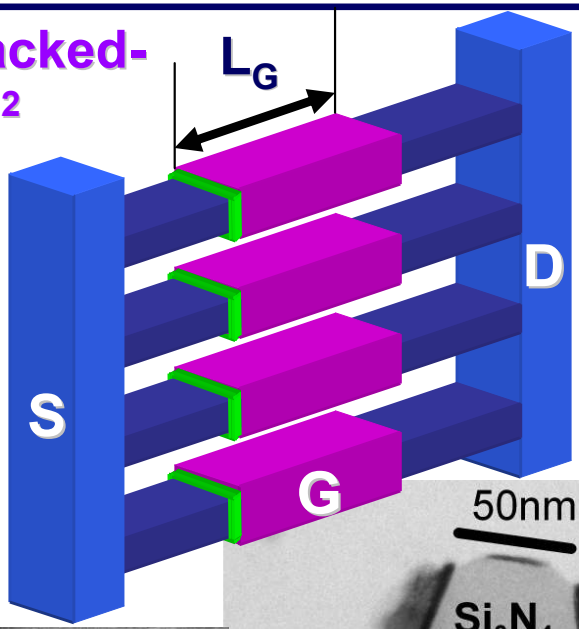
Multi-grilles et nanofils !

GAA = Gate All Around [1]

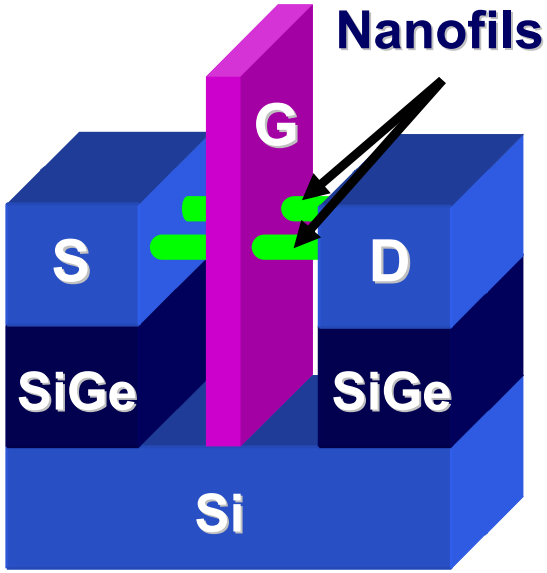


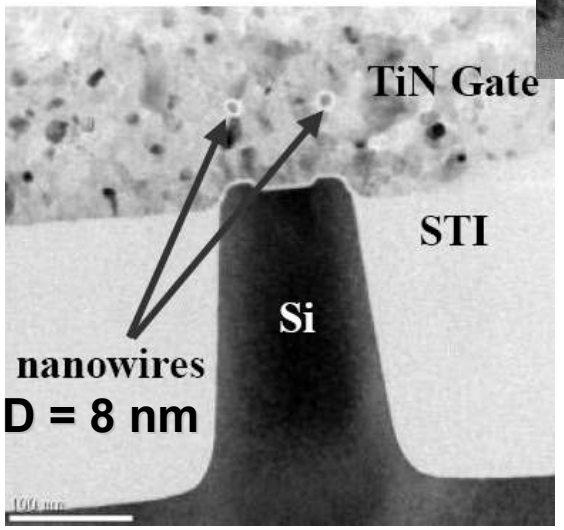


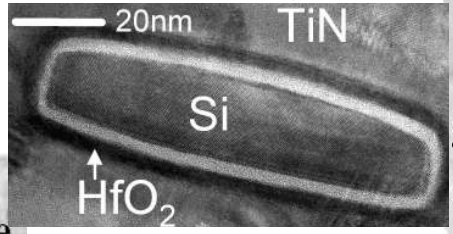
Nano-Beam Stacked-Channels GAA [2]

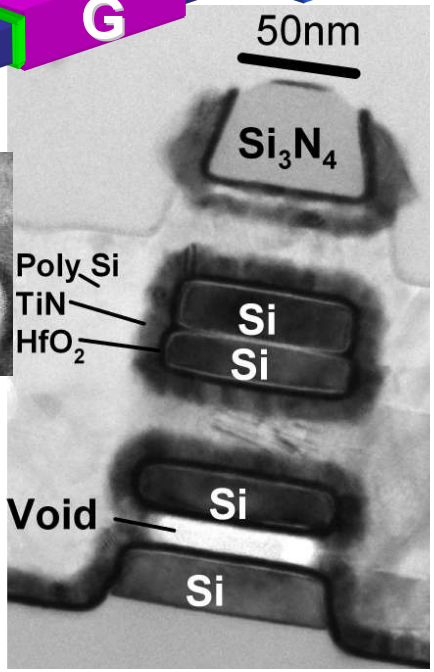


TSNWFET : Twin Silicon NanoWire FET [3]

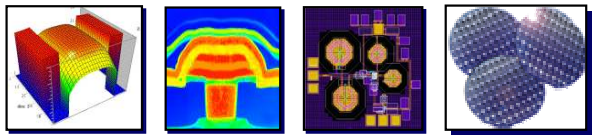




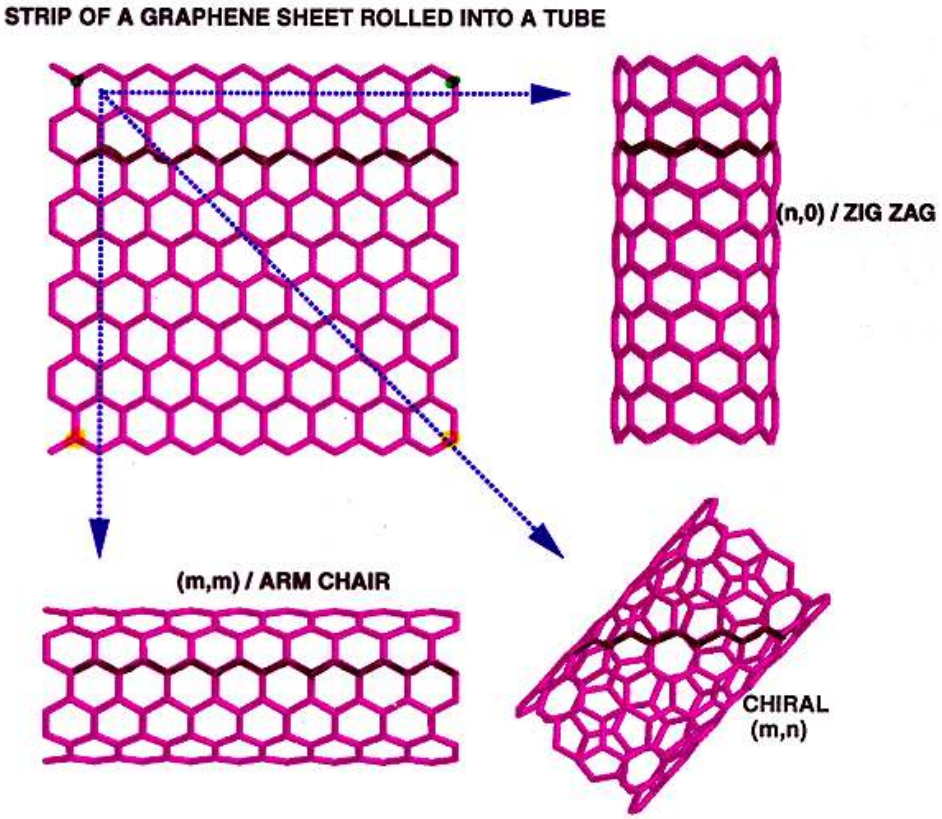


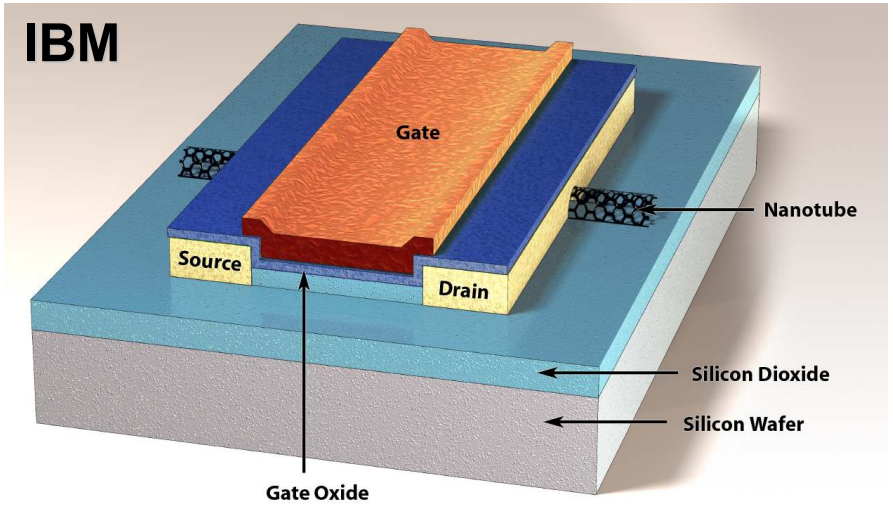


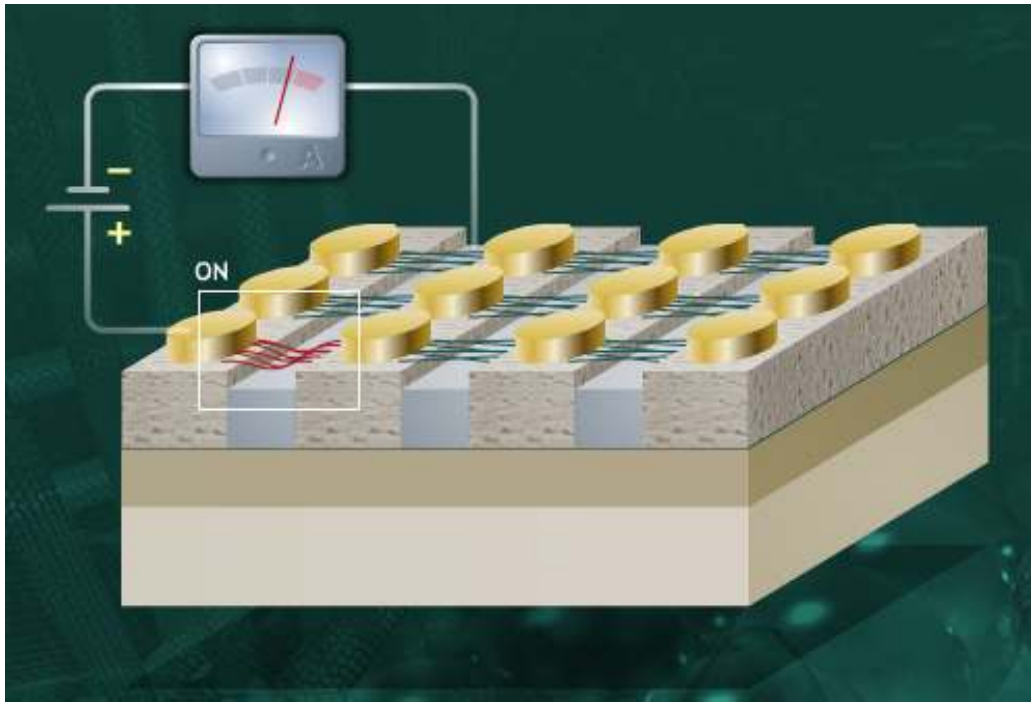
[1] Singh *et al.*, IEDM 2006
[2] Ernst *et al.* (CEA–LETI), IEDM 2006
[3] Yeo *et al.*, IEDM 2006



Nanotubes de carbone

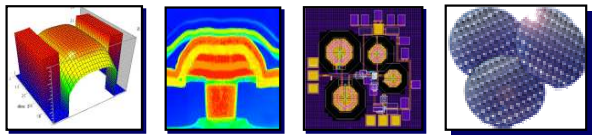




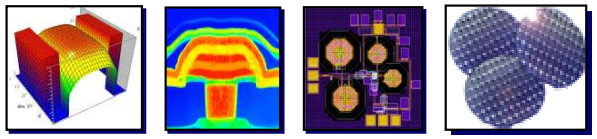


- **Propriété mécanique**
  - **Torsion, flexibilité**
- **Propriétés électriques**
  - **Métallique ou semiconducteur**

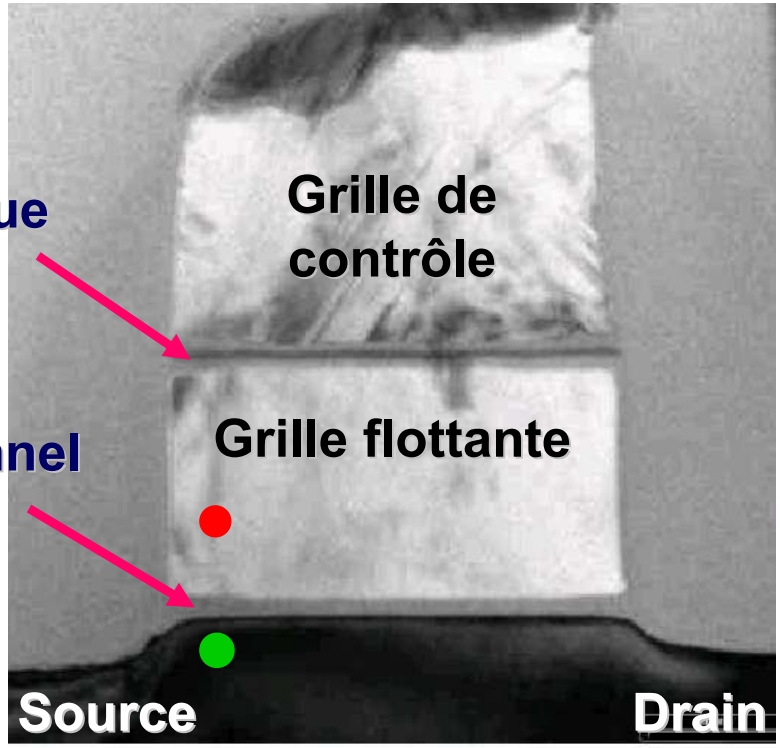
Source : http://www.nantero.com



Et du côté des mémoires non volatiles ?

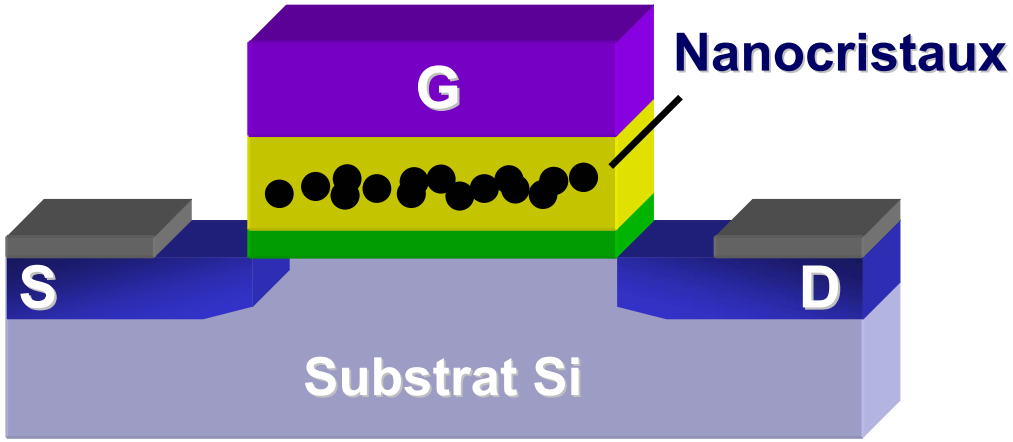


Mémoires Flash



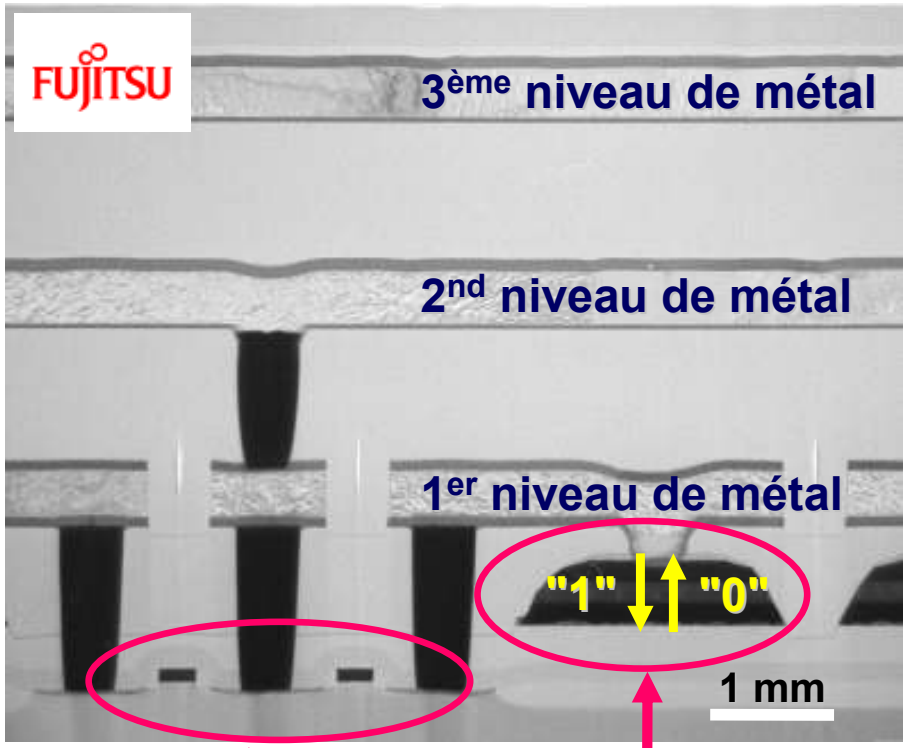
Mémoires à nanocristaux ("Discrete charge trapping")

- Deux "saveurs" de mémoires Flash
  - NOR Flash
    - ✓ Téléphonie mobile…
  - NAND Flash
    - ✓ Stockage de masse



Mémoires ferroélectriques FeRAM

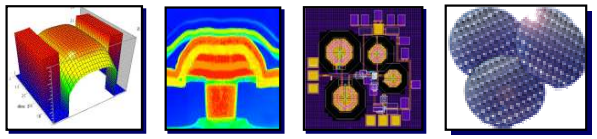
Architecture similaire à celle d'une mémoire DRAM



Transistors

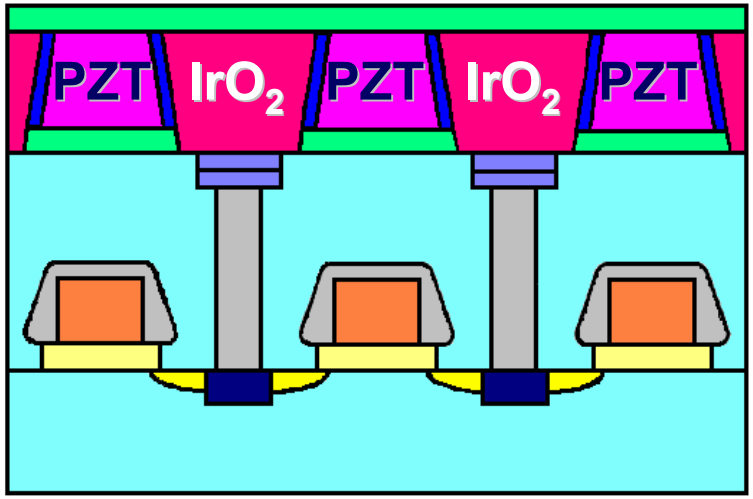
Condensateur ferroélectrique

- Ramtron FM22L16
  - 4 Mbit FeRAM
  - Technologie CMOS 130 nm designée par Texas Instruments
  - Temps d'accès : 55 ns

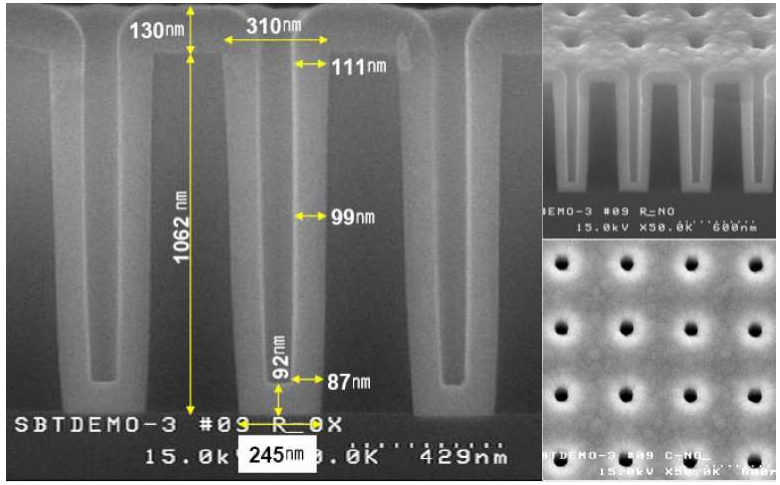


Pour prolonger leur "vie"... ⇒ 3D

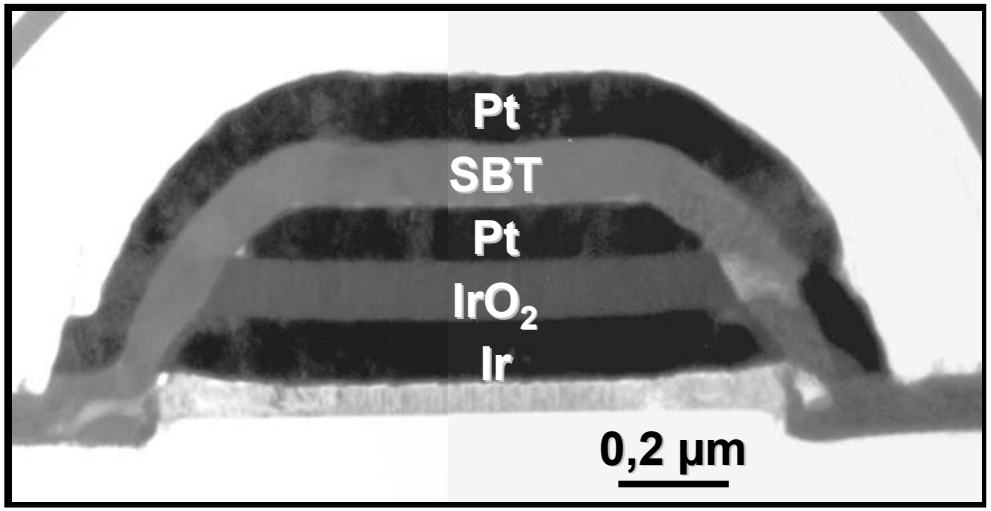
"Vertical" capacitors
Infineon/Toshiba [1,2]



"Trenched" capacitors
Samsung/TIT [3]

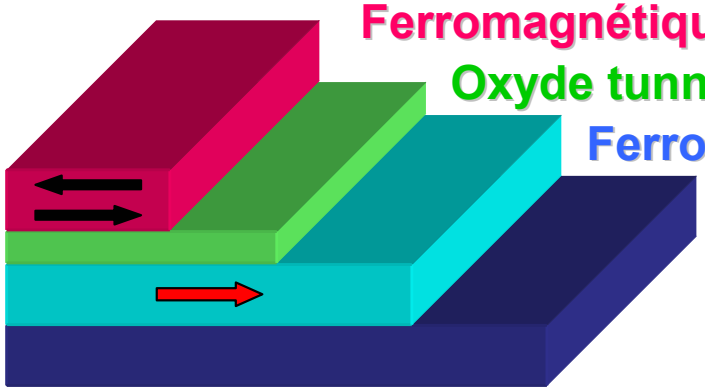


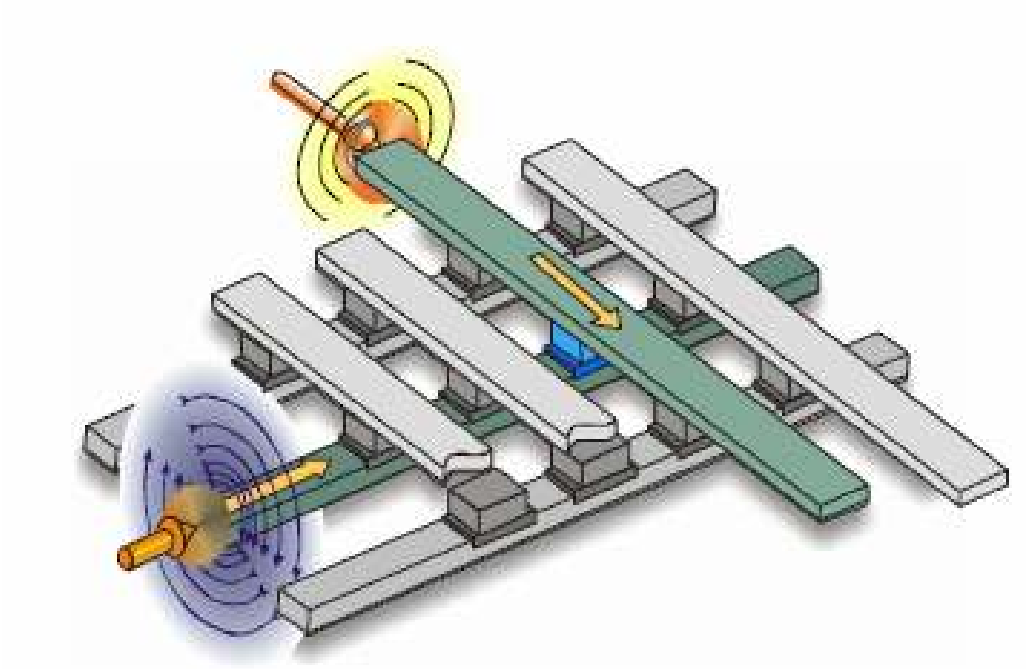
"Pin-shaped" capacitors
IMEC/STMicroelectronics/L2MP [4,5]

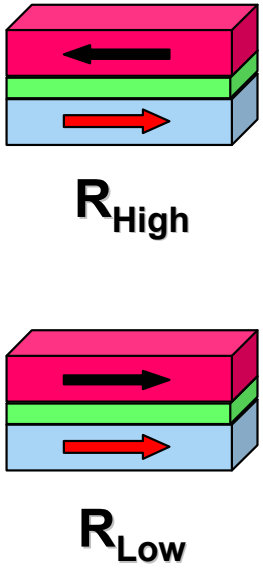


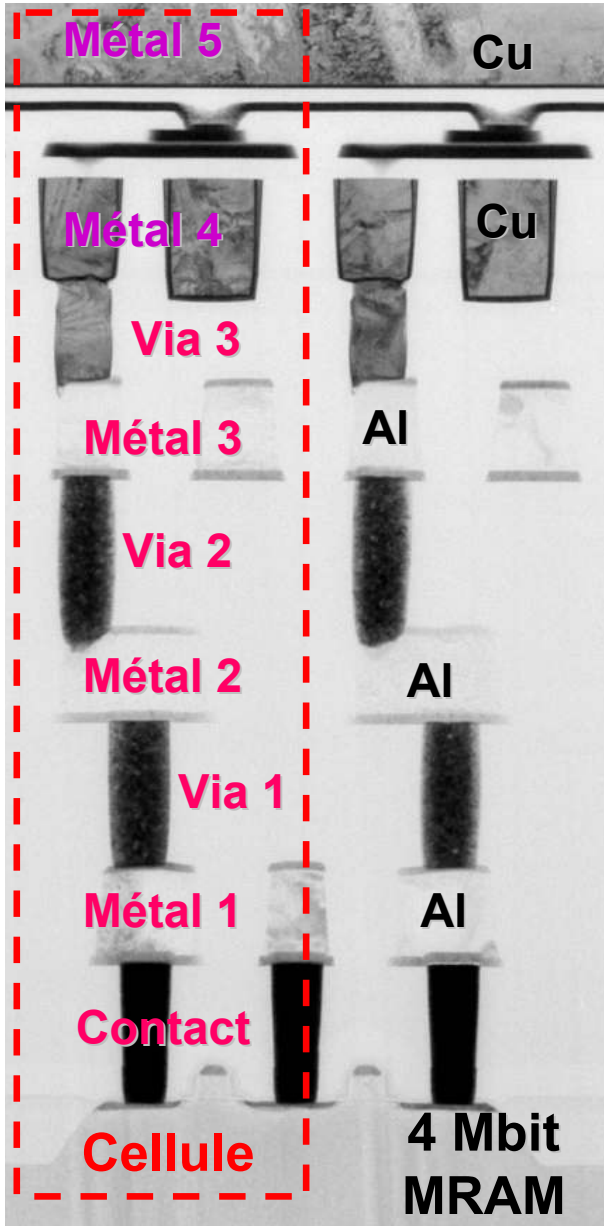
[1] Patent WO 2005/031816 (Infineon)
[2] Nagel *et al.*, VLSI Tech. Dig., p. 146, 2004
[3] Funakubo *et al.*, Integr. Ferroelectrics, vol. 81, p. 219, 2006
[4] Goux *et al.*, IEEE Trans. Elec. Dev., vol. 52, no. 4, p. 447, 2005
[5] Menou *et al.*, Appl. Phys. Lett., vol. 87, no. 7, p. 073502, 2005

Jonction Magnétique Tunnel (JMT)

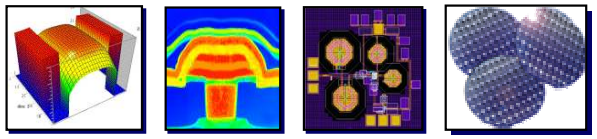






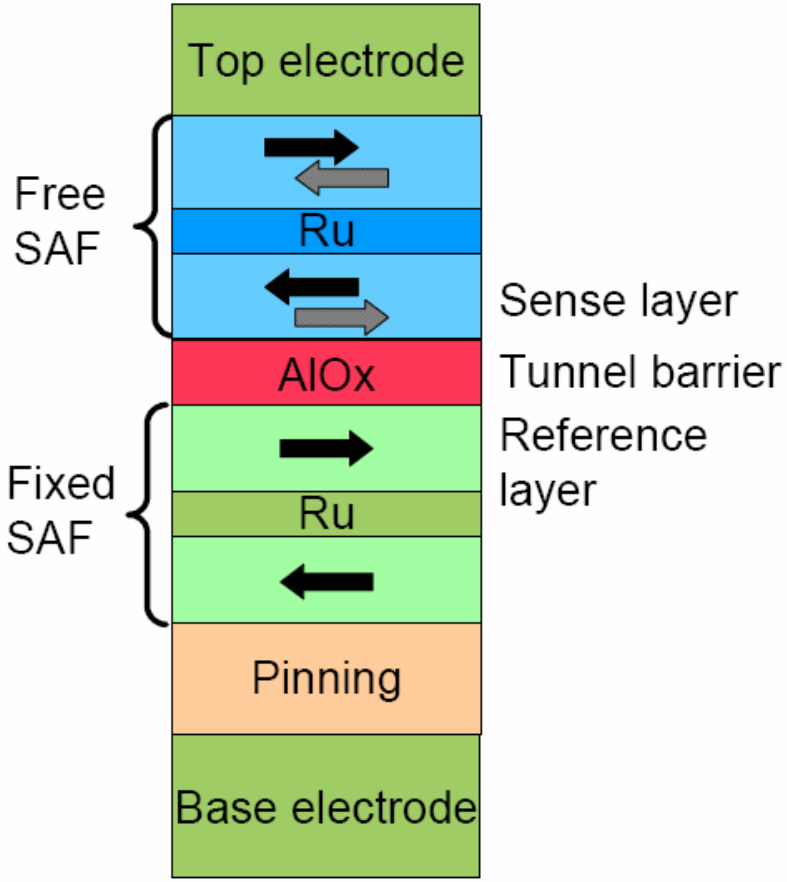


Tehrani *et al.* (Freescale), IEDM 2006

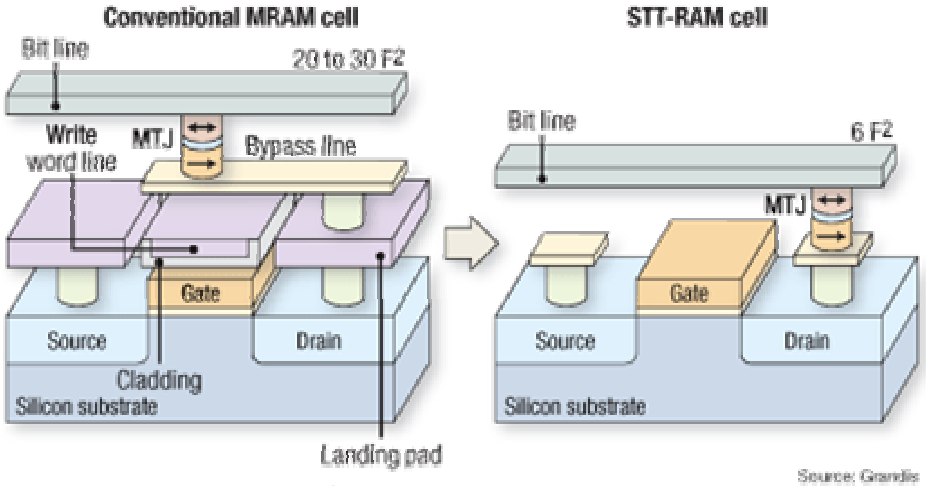


Les innovations ?

Toggle MRAM [1]

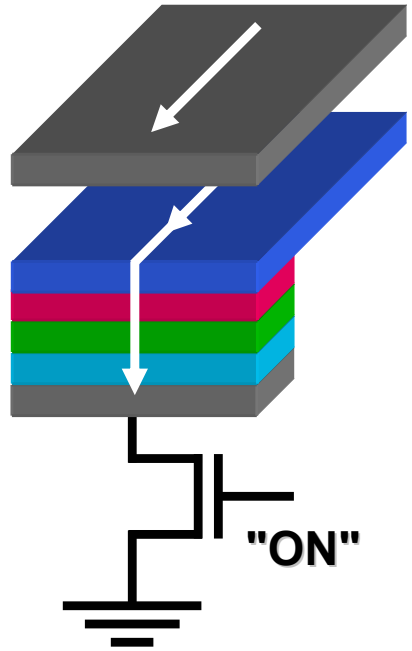


Spin Torque Transfer STT-MRAM [2]

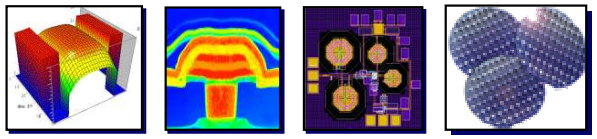


- **1 Mbit STT-RAM test chip**
- **Standalone @ nœud 45 nm**
- **Embedded @ nœud 65 nm**

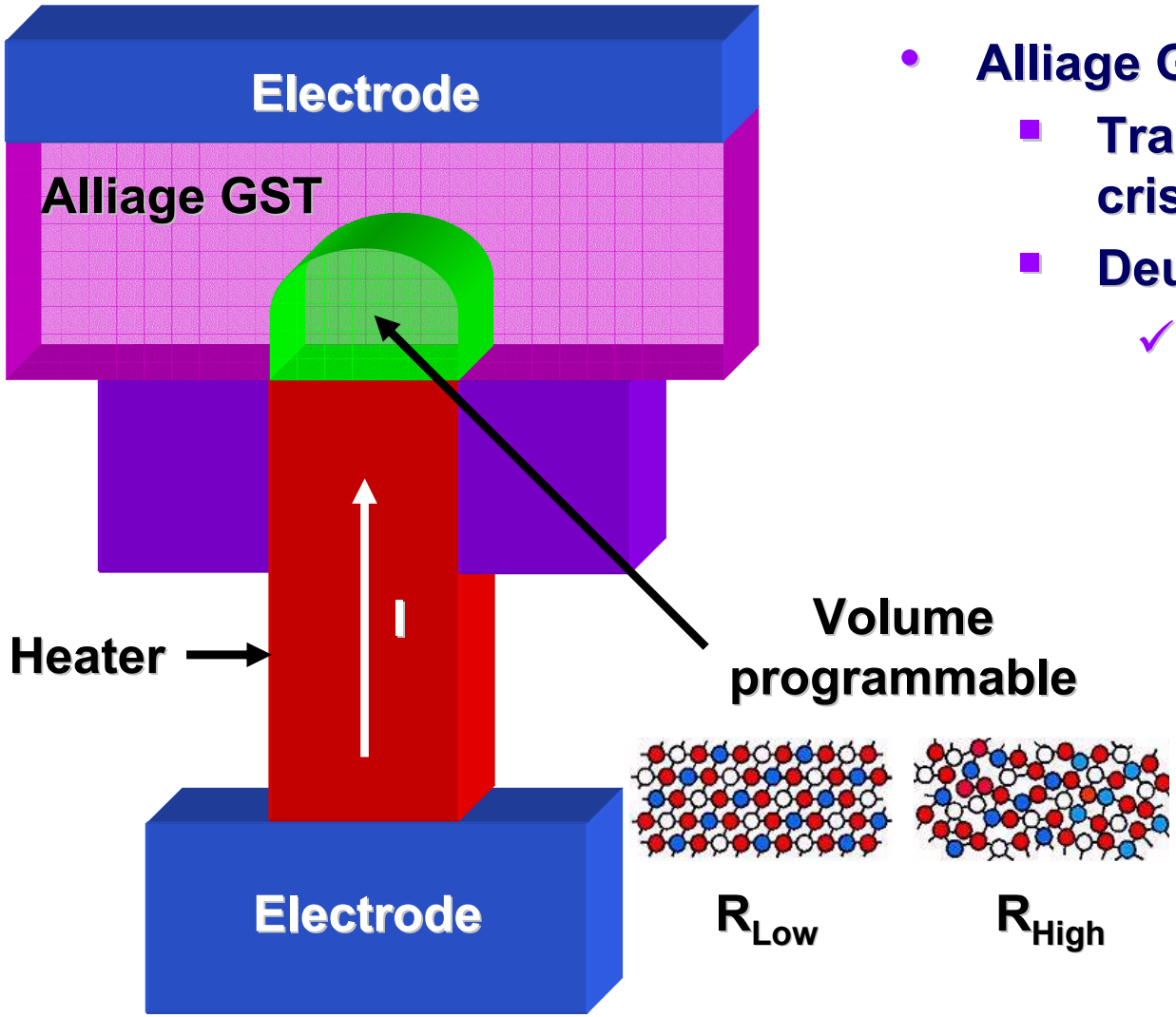
Cellule TAS-MRAM [3]



[1] Nahas *et al.*, IEEE J. Solid State Circuits, vol. 40, no. 1, 2005
[2] Association Renesas Technology et Grandis
[3] http://www.crocus–technology.com

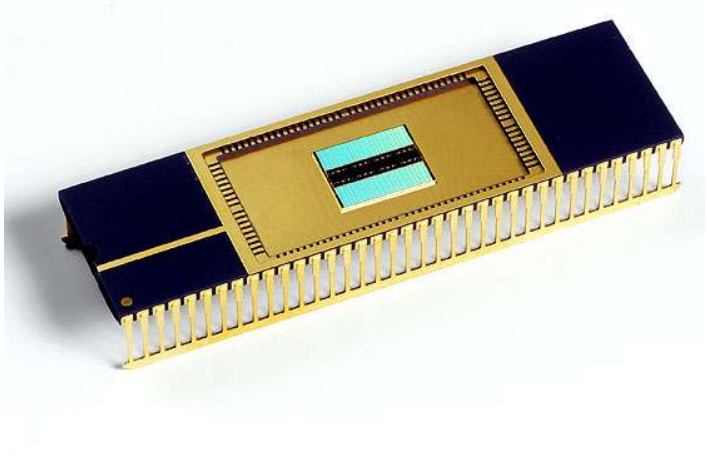


Phase Change RAM (PCM)

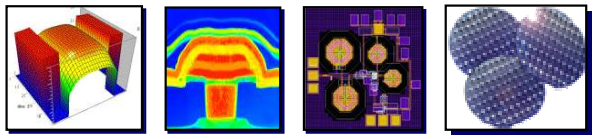


- Alliage GST : $Ge_2Sb_2Te_5$
  - Transition réversible entre un état cristallisé et un état amorphe
  - Deux états de résistance
    - ✓ $R_{Low} \leftrightarrow R_{High}$

Samsung : 512 Mbit PCM en technologie CMOS 90 nm

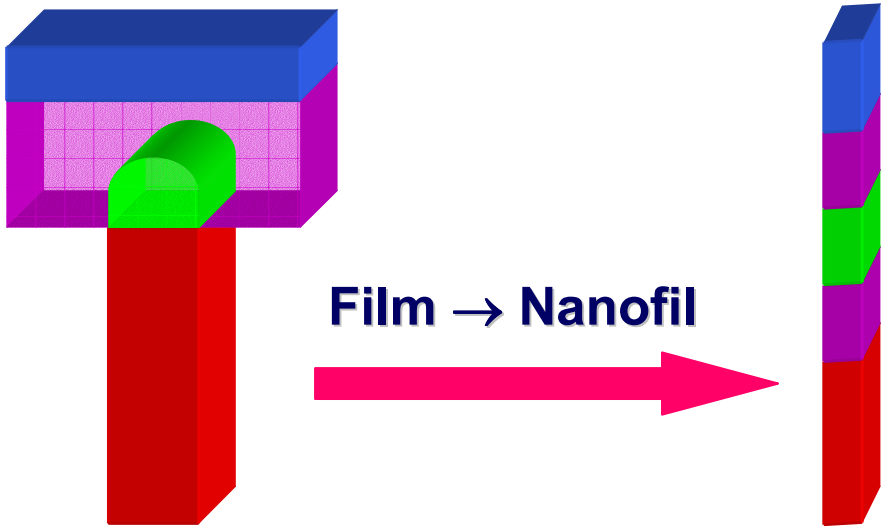


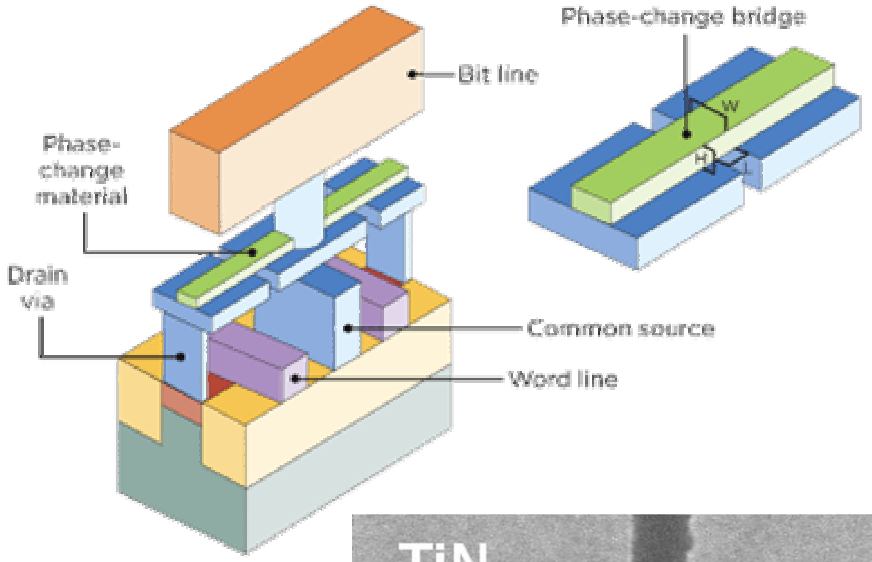
Cho *et al.*, IEEE J. Solid State Circuits, vol. 40, p. 293, 2005



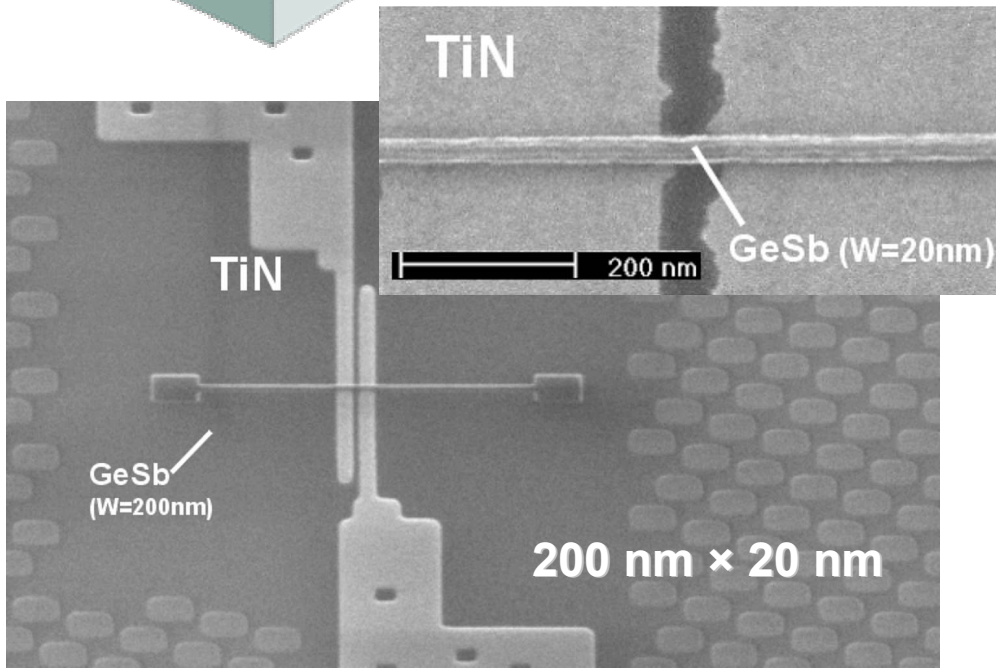
Vers des "PCM nanowires"...

2D PCM **1D PCM**

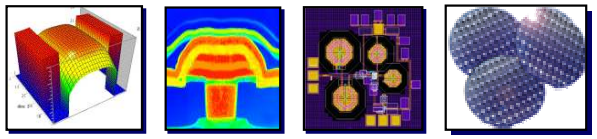




- **Avantages**
  - ↓ Température de fusion en 1D
  - ↓ Volume programmable
- **"Scalabilité"**
  - ↓ Jusqu'à W = 3 nm (S = 60 nm²)
  - ↓ Courant/tension/puissance
  - ↑ Immunité aux perturbations

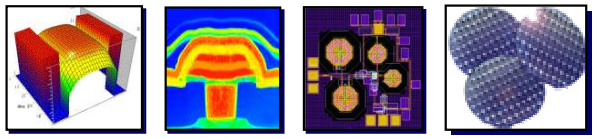


Chen *et al.* (IBM–Qimonda–Macronix), IEDM 2006

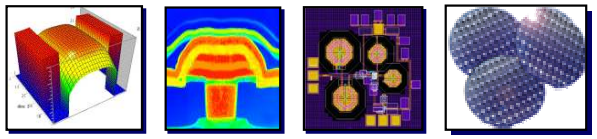


En résumé…

Taille de la cellule (F²)
40
30
20
10
0
MRAM
FeRAM
NOR Flash
NAND Flash
PCM
ReRAM ?
180
130
90
65
45
32
Technologie (nm)



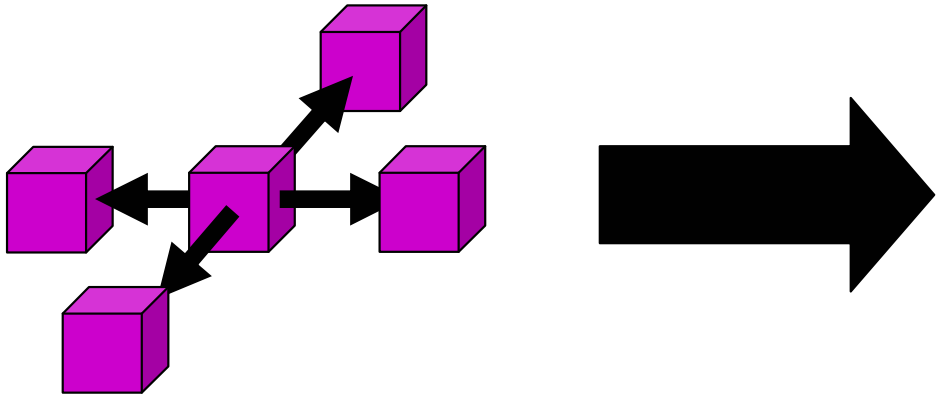
Les promesses des mémoires Resistive RAM…



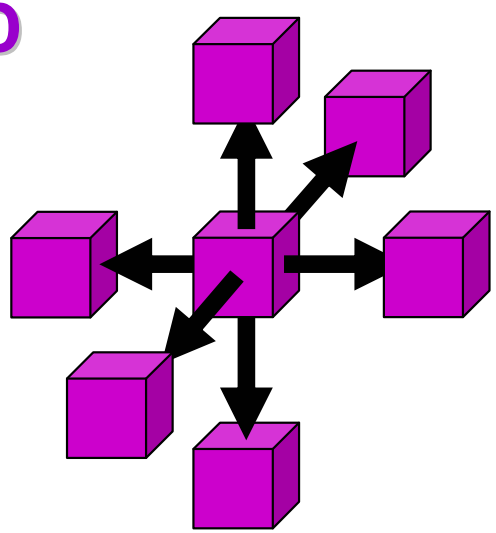
Enjeu des ReRAM

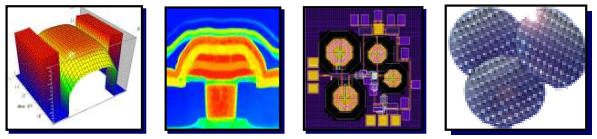
= cellule mémoire

Configuration planaire

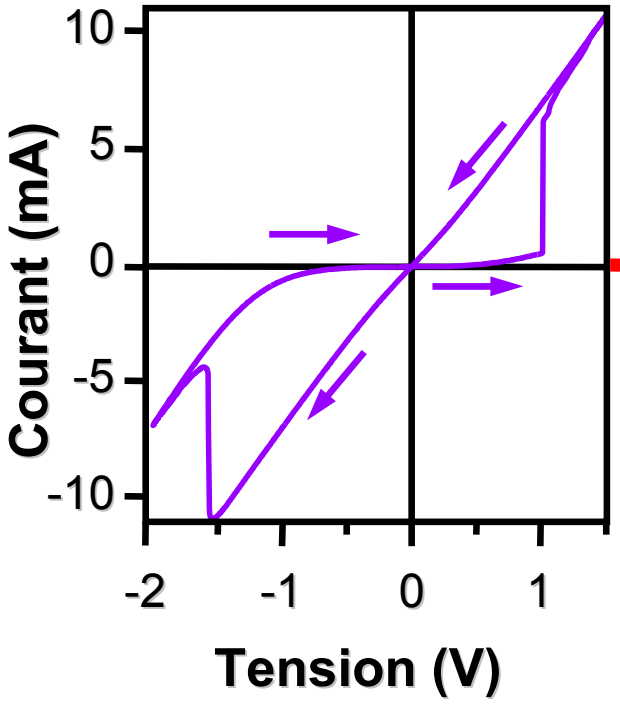


Configuration 3D

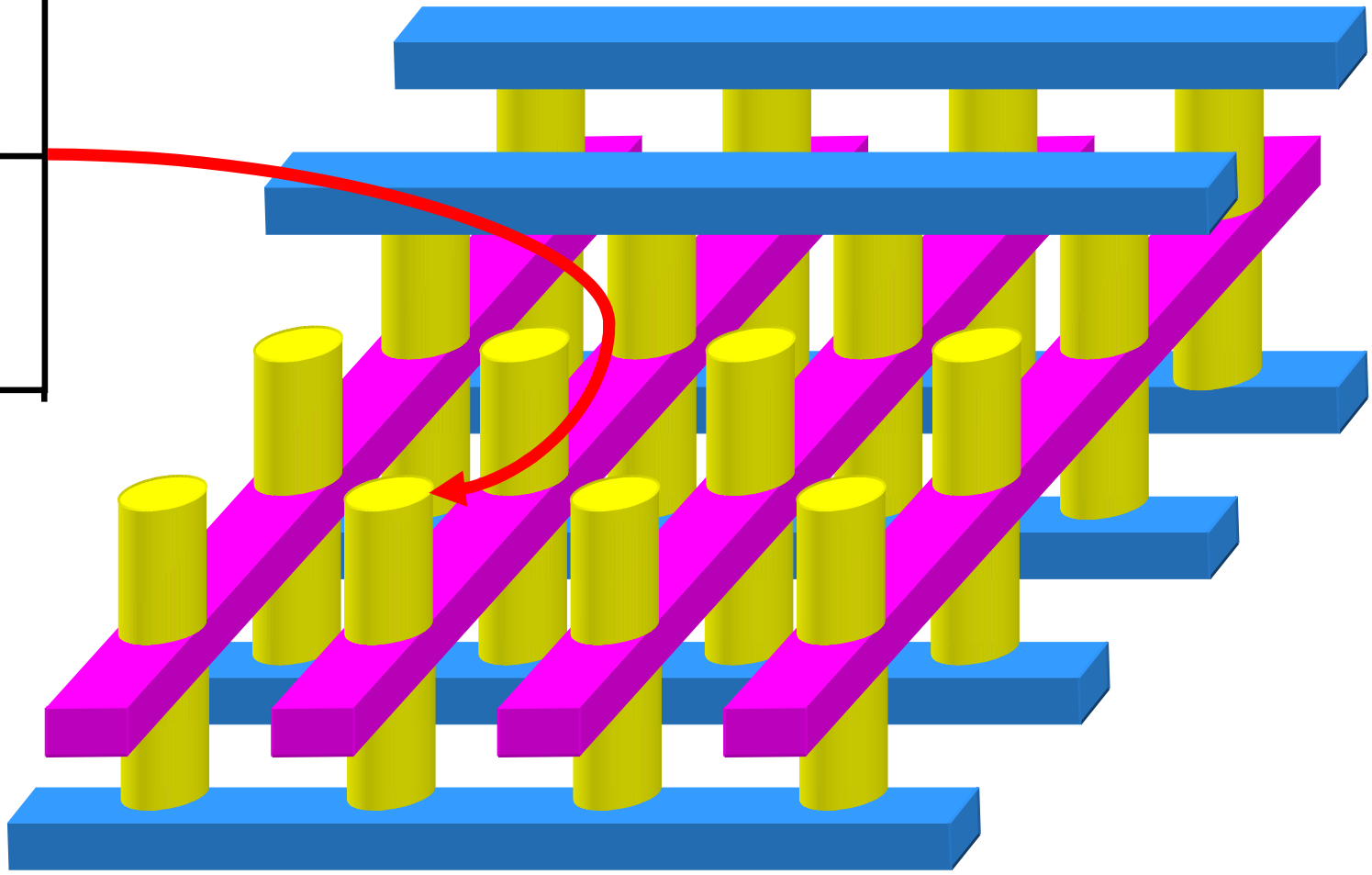




Mémoires à commutation de résistance



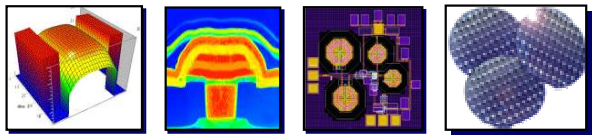
Intégration du point mémoire dans une interconnexion



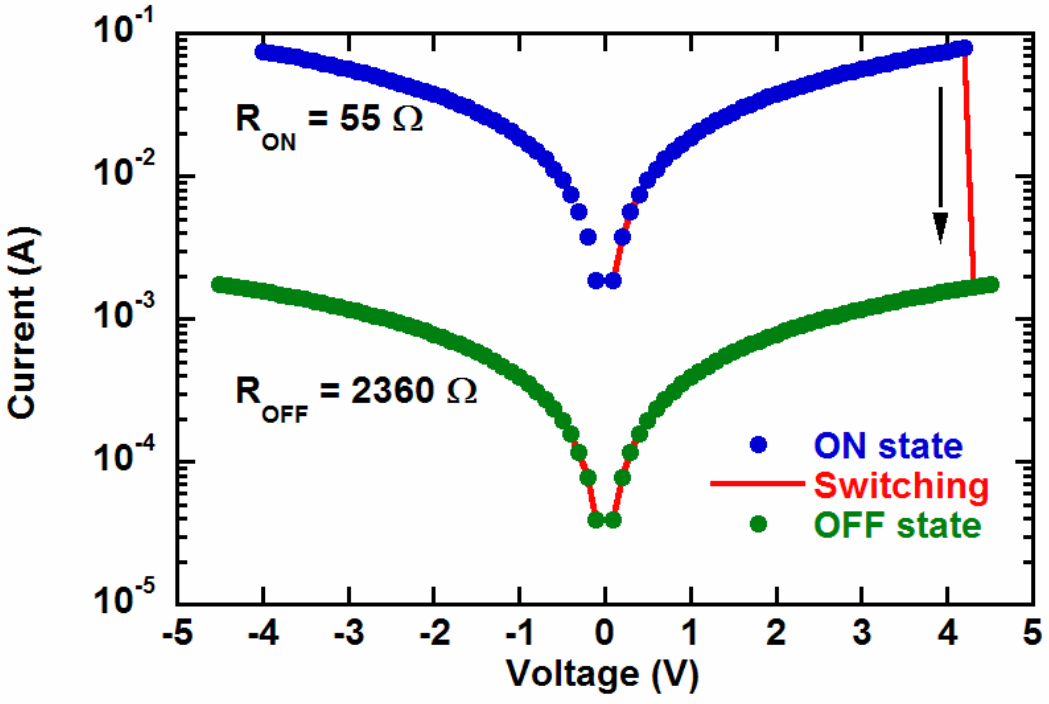
EMMA

"Emerging Materials for Mass-storage Architectures", FP6 IST no. 33751

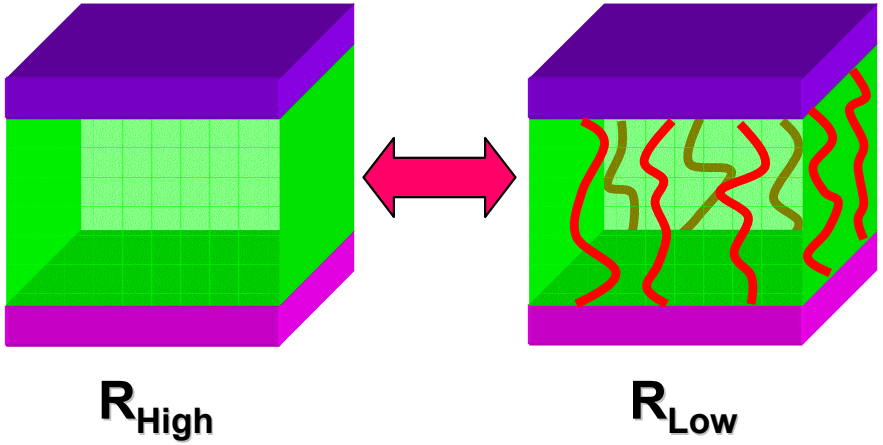
Partenaires : IMEC (B, leader), STMicroelectronics (I), MDM (I), RWTH–Aachen (D), IUNET (I), L2MP (F)

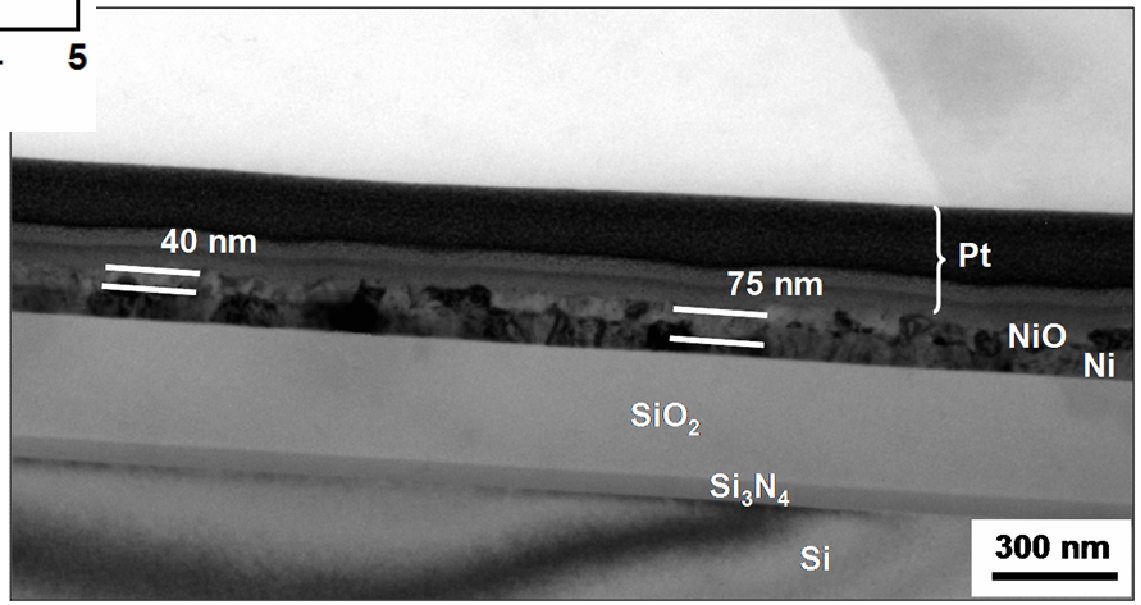


Mémoires OxRRAM

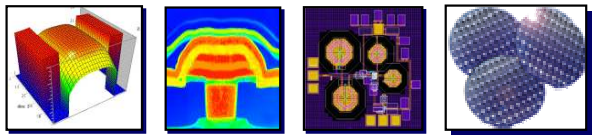


- OxRRAM = Oxide Resistive RAM
- Oxydes bi-stables (NiO, CuO_x, TiO_2…)
- NiO obtenu par oxydation contrôlée d'une couche de Ni
  - Compatibilité avec le process CMOS standard
  - Cu, Ta, Ti, W…

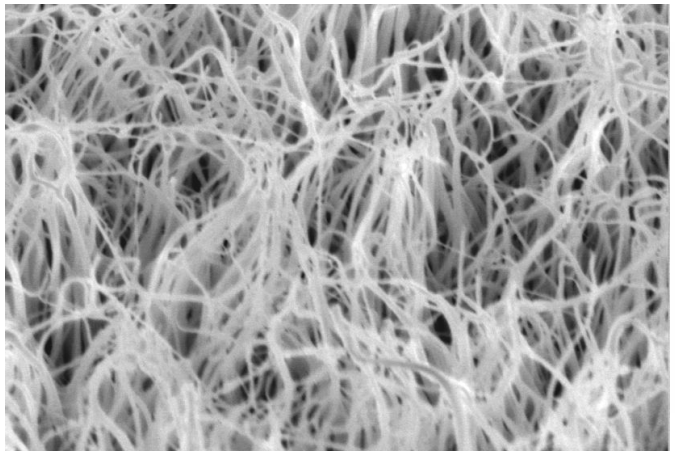


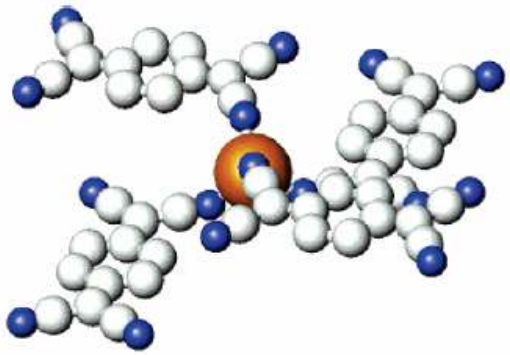


Courtade *et al.*, IEEE Proceedings of NVMTS, p. 94–99, 2006

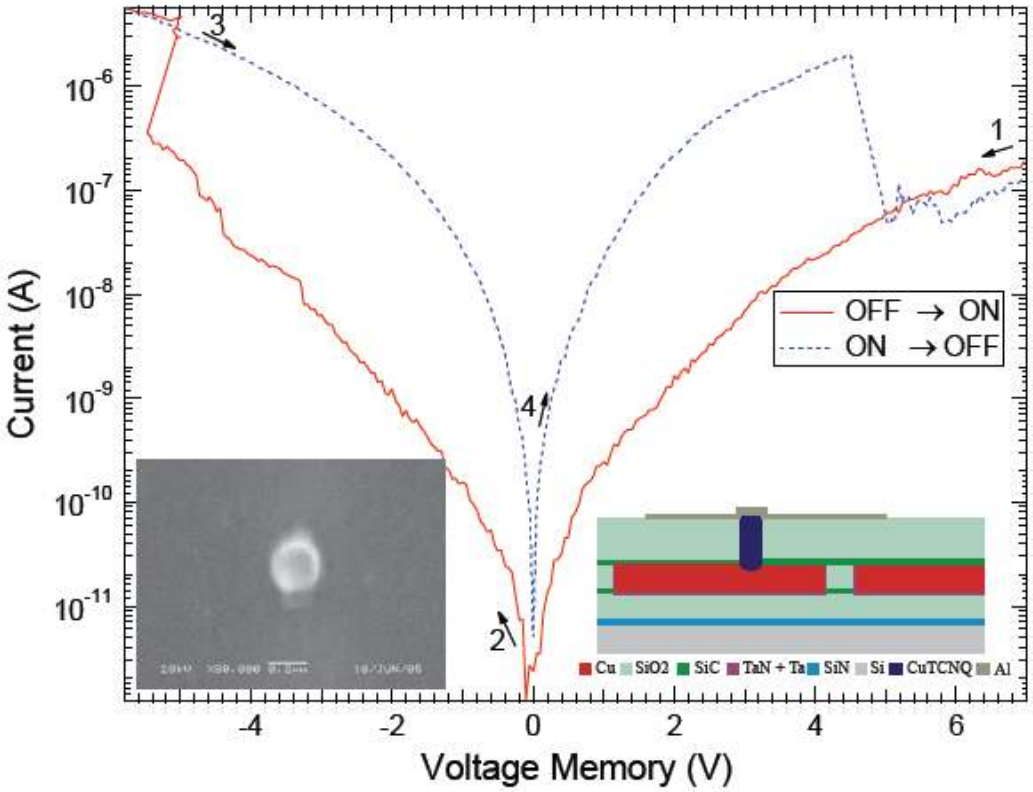


Mémoires Cu-TCNQ

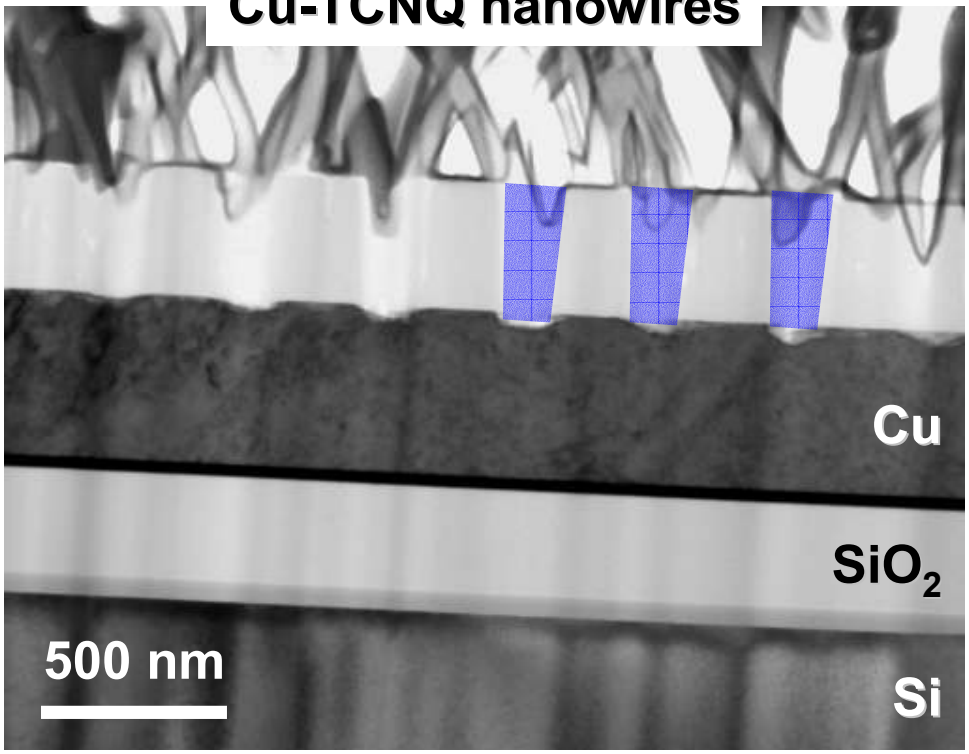




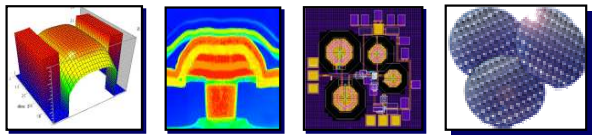
- Complexe organométallique à transfert de charge
- Cu-TCNQ = Cu-Tétracyano quinodiméthane



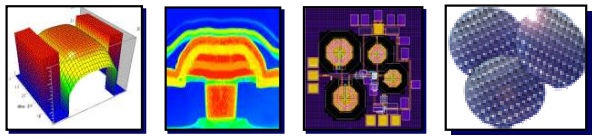
Cu-TCNQ nanowires



Müller *et al.*, Appl. Phys. Lett., vol. 90, p. 063503, 2007

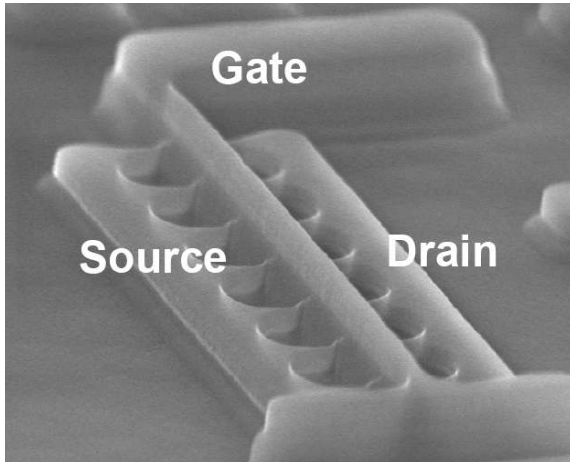
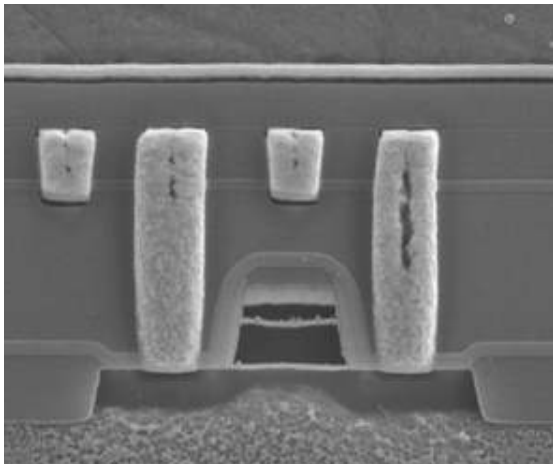
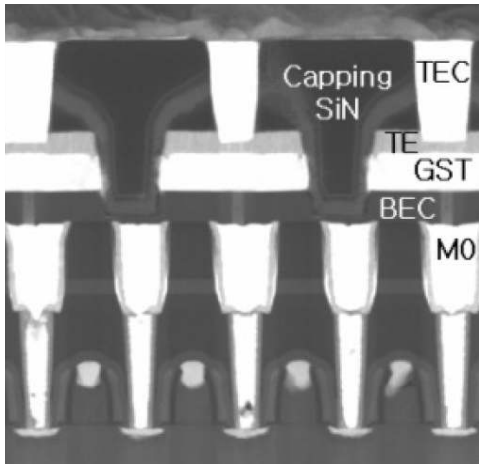


Conclusion

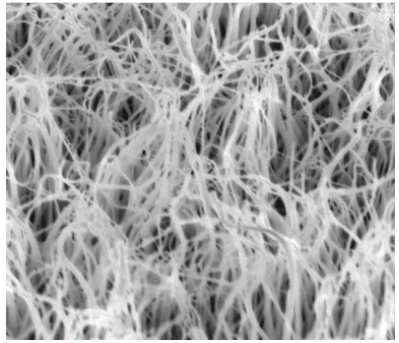


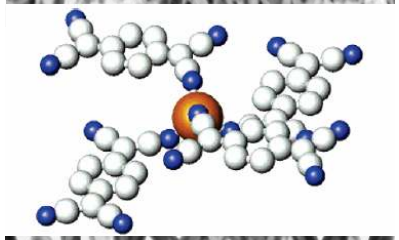
Conclusion

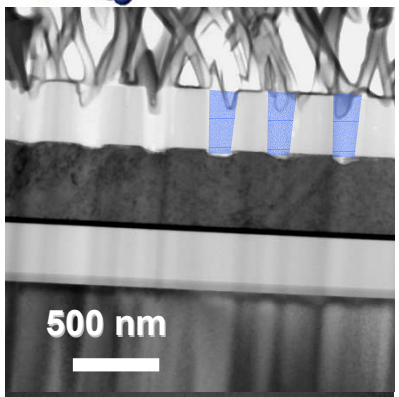
Propriétés des matériaux
Rôle des interfaces

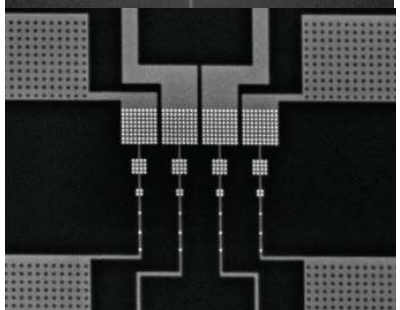
MOSFET	Flash	Mémoires émergentes
		
Nouvelles architectures **Nouveaux matériaux**	**Nouveaux concepts** **Nouveaux matériaux**	**Nouveaux concepts** **Matériaux fonctionnels**

Architecture de la cellule mémoire ← *Downscaling* → **Performances électriques**









EMMA

Stage postdoctoral CNRS

Caractérisation électrique de mémoires à commutation de résistance (OxRRAM, CuTCNQ et PMC)

- Projet européen EMMA (http://www.imec.be/EMMA)
  - "Emerging Materials for Mass-storage Architectures"
- Finalité du projet
  - Nouvelles mémoires non volatiles très haute densité
  - Mémoires à commutation de résistance (Low R ⇔ High R)
- Systèmes sélectionnés
  - Organométallique : CuTCNQ
  - Oxydes : NiO, WO_3, MoO_3…
- Rôle du candidat
  - Caractérisation électrique et analyse de la fiabilité
  - Développement de tests d'accélération du vieillissement
  - Compréhension des mécanismes physiques de commutation
- Nature du contrat
  - CDD d'un an renouvelable
  - Date de démarrage : ASAP

Laboratoire Matériaux et Microélectronique de Provence
UMR CNRS 6137 – Marseille/Toulon (France)