FIRST CALL FOR PAPERS

PATMOS 2006

Sixteenth International Workshop on Power and Timing Modeling, Optimization and Simulation

13 -15 September 2006, Montpellier, France

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PATMOS 2006 is the sixteenth in a series of international workshops. The PATMOS meeting has evolved into an important European event, where industry and academia meet to discuss power and timing aspects in modern integrated circuit and system design. PATMOS 2006 is organized by *LIRMM*.

Montpellier has for centuries been a city where different cultures meet. Today, it is a dynamic economy in which art and science go hand in hand with advanced technology and the superb Mediterranean style-life. Part of the great European Medieval City tradition, open to the world, linked as much to the Mediterranean as to northern Europe, it is forever welcoming and assimilating new ideas, a melting pot of all that is best in today's civilisation. Montpellier is both a city dedicated to building a new Europe, and one of the southern Europe's main metropolies. There has been a university in Montpellier since the middle age. The medical faculty was founded in 1222, followed by humanities and law. The Montpellier science faculty was set up in 1808.
By plane: 10km from the Montpellier Méditerranée Airport with about 10 flights/day with Paris airports.
By car: about 2 hours from Nice Sophia/Antipolis, or Grenoble or Toulouse.

The PATMOS objective is to provide a forum to discuss and investigate the emerging challenges in methodologies and tools for the design of upcoming generations of integrated circuits and systems. The technical program will focus on timing, performance and power consumption as well as architectural aspects with particular emphasis on modelling, design, characterization, analysis and optimization. The emphasis of the workshop is on, but not limited to, the following topics:

- **Power Consumption**
  - o Design techniques for low power circuits and systems at all levels of abstraction;
  - o Methods and tools for analysis, characterization, design and optimization of the power consumption;
  - o Low Power architectures and libraries;
  - o Special power related topics, e.g.: low voltage, leakage power, power grid, interconnect power, clock tree power, power aware test pattern generation.
- **Timing and Performance**
  - o Methodologies and tools for the analysis, design and verification of timing and performance properties of integrated circuits and systems at all levels of abstraction;
  - o Special timing or performance related topics include: crosstalk, synchronization, GALS.
- **Design Experience and Cases Studies**
  - o Examples, test cases, benchmarks or design studies which present innovative solutions for timing, performance or power consumption related design challenges.

Contributions are invited for regular presentations and discussion sessions. Perspective authors are invited to submit their complete paper, no later than **March 26, 2006**, including a 100-word abstract and illustrations, in A4 camera-ready format, not exceeding 10 pages or 5000 words. Electronic submission is required and should follow the style for the final publication. Submitted papers will be reviewed formally and anonymously by several reviewers. The PATMOS 2006 proceedings will be published by Springer in the series "Lecture Notes in Computer Science (LNCS)."

Selected papers will be included in special issues of Journals, as e.g. The Journal of Low Power Electronics.

Proposals for panel sessions and special sessions are encouraged and must be received no later than March 26, 2006.

More information can be found on the PATMOS 2006 website: http://www.lirmm.fr/patmos06

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