SETS'26 Program

Session 1 – Tuesday, March 10, 08:30

Fault Resilience in AI and Embedded Systems

Moderator: Rolf Drechsler, Univ. Bremen

Adaptive Fault Resilience for Early-Exit DNNs
Rama Mounika Kodamanchili, TalTech

A Distributed Architecture for Runtime Fault Management in RISC-V based edge-AI SoCs
Ashwin Santhosh, TalTech / Testonica Lab / Infineon

Exploiting Spatial and Temporal Consistency for Fault Detection in Semantic Segmentation NN
Lorenzo Fezza, Politecnico di Torino

Session 2 – Tuesday, March 10, 17:30

Advances in Cell-Aware Modeling

Moderator: Maksim Jenihhin, TalTech

Optimizing Cell-Aware Test Runtime via Functional Fault Correlations
Reza Khoshzaban, Politecnico di Torino / LIRMM / STMicroelectronics

A Defect-Detection Graph-Based Methodology for Cell-Aware Model Generation (TrUnDeL)
Gianmarco Mongelli, STMicroelectronics / LIRMM

A Hierarchical Graph Neural Network-Based Methodology for SRAM Cell-Aware Model Generation
S. Riabi, STMicroelectronics / LIRMM

Session 3 – Wednesday, March 11, 08:30

Memory Testing / Diagnostic and Neuromorphic Hardware Architectures

Moderator: Riccardo Cantoro, Politecnico di Torino

A Digital Approach for Testing Analog Memories
D. Ronga, LIRMM

On Using Graph Theory and Machine Learning to Improve SRAMs Diagnosis Accuracy and Quality
D. Chaves Vieira, LIRMM / STMicroelectronics

Neuromorphic Hardware Architectures for Energy-Efficient and Fault-Tolerant Embedded AI
Liam Friel, TIMA

Session 4 – Thursday, March 12, 08:30

Hardware Security and Side-Channel Analysis

Moderator: Paolo Bernardi, Politecnico di Torino

Improving RO-PUFs on FPGAs: A Filtering Approach for Improved Reliability and Entropy
Vasilii Kulagin, TIMA

Mitigating Optical Probing at Circuit and Layout Levels
Sajjad Parvin, Univ. Bremen / DFKI

Secret Key Extraction by BIKE flipping
Tarick Welling, Univ. Stuttgart

Session 5 – Thursday, March 12, 17:30

Test Generation and Virtual Prototyping

Moderator: Gianmarco Mongelli, LIRMM

New Techniques for STL generation for Vector Processing Units
Gustavo Vilar de Farias, Politecnico di Torino

Exploring the Limits of LLMs for System-Level Test Program Generation: Can LLaMas Outrun Darwin?
Denis Schwachhofer, Univ. Stuttgart / Advantest

Using Virtual Prototypes for Causal Fault Explanations at System Level
Caroline Dominik, Univ. Bremen / DFKI