Polytech'Montpellier – ERII 4
M2 EEA – Systèmes Microélectroniques

Analog IC Design

Chapter I
Introduction to Microelectronics Technology

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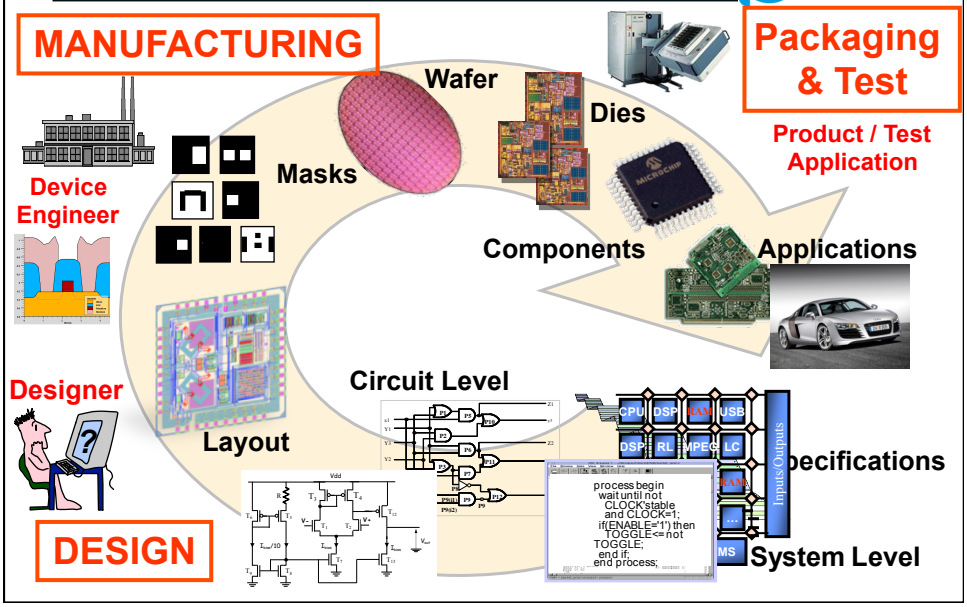
Analog IC Design for MEA4

- Semester 7:
  - 37.5 hours: 7 integrated lectures / 3 evals / 4 tutored HW
  - Personal investment: 15 to 20 hours minimum
  - Group project (60h): design, layout, fabrication…
  - Outline
    - → Introduction to Microelectronics Technology
    - → Small-signal modeling and analysis
    - → Voltage and current sources
    - → Voltage amplifiers
    - → Trans-conductance amplifiers
    - → Operational amplifiers
- Semester 8:
  - 30 hours of integrated lectures
    - Advanced performances: variability, offset, CMRR, PSRR, noise…
    - Advanced amplifiers…
  - Group project (60h): design, layout, fabrication…

Microelectronics: life cycle and associated jobs



Profile of a Microelectronics Circuits Designer

- A scientist
  - Physics, Electronics, Computer Engineering, Automation control
  - Basic knowledge of fabrication process
- An engineer
  - Analog and digital circuits
  - System design and architecture
  - EDA tools
    - Schematic, Electrical simulation, Analysis
    - HDL language, synthesis
    - Layout, P&R, LVS, post-layout analysis

Outline

- History: five decades of innovations
- Overview of Microelectronics technology
- Elementary process steps
- CMOS process at a glance
- Layout basics and design rules
- Homework
- References

1.1. History: genesis

- 1833 - First Semiconductor Effect is Recorded
  - Michael Faraday describes the "extraordinary case" of his discovery of electrical conduction increasing with temperature in silver sulfide crystals. This is the opposite to that observed in copper and other metals.

In a chapter entitled "On Conducting Power Generally" in his book *Experimental Researches in Electricity* Faraday writes "I have lately met with an extraordinary case … which is in direct contrast with the influence of heat upon metallic bodies … On applying a lamp … the conducting power rose rapidly with the heat … On removing the lamp and allowing the heat to fall, the effects were reversed."

1.1. History: genesis

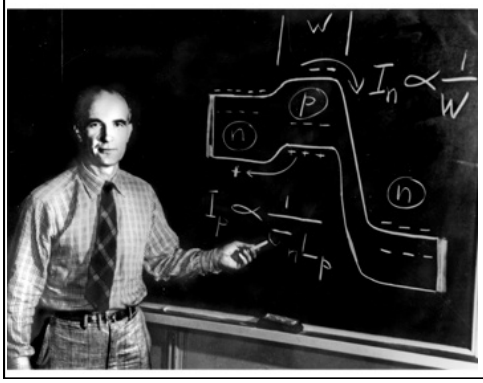
- 1940 - Discovery of the *p-n* Junction
  - Russell Ohl (Bell Telephone labs) discovers the p-n junction and photovoltaic effects in silicon that lead to the development of junction transistors and solar cells.

Ohl and colleague Jack Scaff found a separation of silicon into regions containing distinct kinds of impurities. One impurity, phosphorus, yielded a slight excess of electrons in the sample while the other, boron, led to a slight deficiency (later recognized as "holes"). They called the regions *n*-type and *p*-type; the surface or "barrier" where these regions met became known as a "*p-n* junction." Light striking this junction stimulated electrons to flow from the *n*-side to the *p*-side, resulting in an electric current. Ohl had discovered the photovoltaic effect that powers today's solar cells (1954).

Russell Ohl (bow tie) with Jack Scaff (dark hair) at Bell Laboratories

1.1. History: genesis

- 1948 - Conception of the Junction Transistor
  - William Shockley (Bell Labs physicist) conceives a transistor structure based on a theoretical understanding of the p-n junction effect.



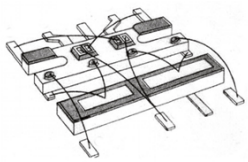
After Bardeen and Brattain's December 1947 invention of the point-contact transistor, he conceived a distinctly different transistor based on the *p-n* junction. He claimed that positively charged holes could also penetrate through the bulk germanium material - not only trickle along a surface layer. Called "minority carrier injection," this phenomenon was crucial to operation of his junction transistor, a three-layer sandwich of *n*-type and *p*-type semiconductors separated by *p-n* junctions. This is how all "bipolar" junction transistors work today.

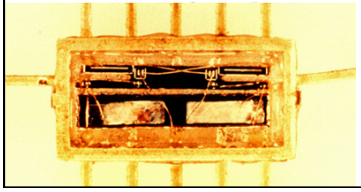
1.1. History: genesis

- 1954 - William Shockley left Bell Labs to start its own company in Palo Alto, CA.
  → Silicon Valley
  - Young people, such as G. E. Moore and R. N. Noyce, joined Shockley Company
- 1957 - Moore and Noyce to set-up Fairchild
- 1959 - Invention of the "Planar" Manufacturing Process
  - Jean Hoerni (Fairchild) develops the planar process to solve reliability problems of solid-state transistors, thereby revolutionizing semiconductor manufacturing.

1.1. History: genesis

- **1958 - All semiconductor "Solid Circuit" is demonstrated**
  - **Jack Kilby (Texas Instruments) produces a microcircuit with both active and passive components fabricated from semiconductor material.**

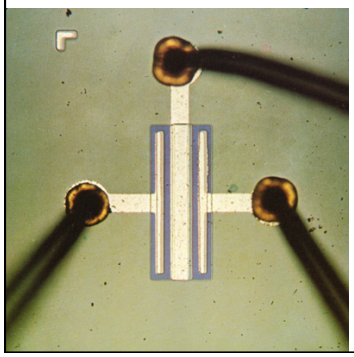




On September 12, 1958, Jack Kilby built a circuit using germanium mesa *p-n-p* transistor slices he had etched to form transistor, capacitor, and resistor elements. Using fine gold "flying-wires" he connected the separate elements into an oscillator circuit. One week later he demonstrated an amplifier. T.I. announced Kilby's "solid circuit" concept in March 1959 and introduced its first commercial device in March 1960, the Type 502 Binary Flip-Flop priced at $450 each.

1.1. History: genesis

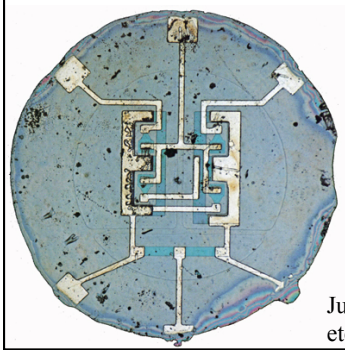
- 1960 - Metal Oxide Semiconductor (MOS) Transistor Demonstrated
  - John Atalla and Dawon Kahng fabricate working transistors and demonstrate the first successful MOS field-effect amplifier (Bell Labs).



The MOS transistor conducting region is either *p*-type (making it a "*p*-channel" device) or *n*-type ("*n*-channel" device) material. The latter are faster than *p*-channel but are more difficult to make. MOS devices hit the commercial market in 1964. General Microelectronics (GME 1004) and Fairchild (FI 100) offered *p*-channel devices for logic and switching applications; RCA introduced an *n*-channel transistor (3N98) for amplifying signals.

1.1. History: early days

- 1960 - First Planar Integrated Circuit is Fabricated
  - Jay Last (Fairchild) leads development of the first commercial IC based on Hoerni's planar process and Noyce's monolithic approach.

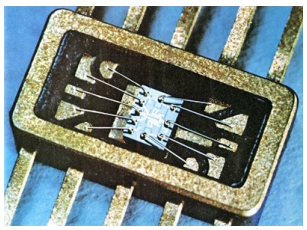


Under the trade name µLogic (Micrologic), the type "F" flip-flop function was announced to the public in March 1961 via a press conference at the IRE Show in New York and a photograph in LIFE magazine. Five additional circuits, including the type "G" gate function, a half adder, and a half shift register, were introduced in October.

Junction-isolated version of the type "F" flip-flop. The die were etched to fit into a round TO-18 transistor package

1.1. History: early days

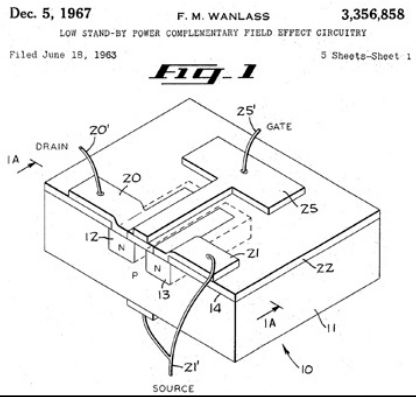
- **1962 – First applications for ICs in computers (Aerospace systems)**
  - The first ICs replaced only a handful of components, and sold for many times the price of their discrete transistor counterparts. In 1961, Jack Kilby's colleague Harvey Cragon built a demonstration Computer for the US Air Force to show that 587 TI ICs could replace 8,500 transistors and other components.



NASA's Apollo Guidance Computer (AGC) was the most significant early project. Designed by MIT in 1962 and built by Raytheon, each system used about 4,000 "Type-G" (3-input NOR gate) circuits. Consuming 200,000 units at $20-30 each, the AGC was the largest user of ICs through 1965.

1.1. History: early days

- **1963 - Complementary MOS Circuit Configuration is Invented**
  - **Frank Wanlass invents the lowest power logic configuration.**



In a 1963 conference paper C. T. Sah and Frank Wanlass of the Fairchild R & D Laboratory showed that logic circuits combining *p*-channel and *n*-channel MOS transistors in a complementary symmetry circuit configuration drew close to zero power in standby mode. Wanlass patented the idea that today is called CMOS.

1.1. History: early days

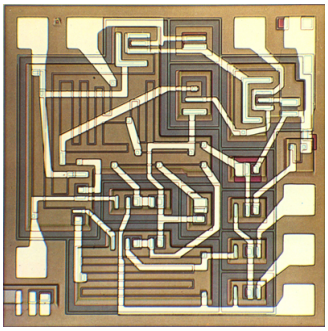
- 1964 - First Commercial MOS IC Introduced
  - General Microelectronics uses a Metal-Oxide-Semiconductor (MOS) process to pack more transistors on a chip than bipolar ICs and builds the first calculator chip set using the technology.

General Microelectronics introduced the first commercial MOS integrated circuit in 1964 when Robert Norman used a 2-phase clock scheme to design a 20-bit shift register using 120 p-channel transistors. GMe designed 23 custom ICs for the first MOS-based electronic calculator for Victor Comptometer in 1965.

The prototype Victor Comptometer EC-3900 calculator and board with 23 custom MOS chips and six 100-bit shift registers for serial memory

1.1. History: early days

- 1964 - The First Widely-Used Analog Integrated Circuit is Introduced
  - David Talbert and Robert Widlar at Fairchild kick-start a major industry sector by creating commercially successful ICs for analog applications.

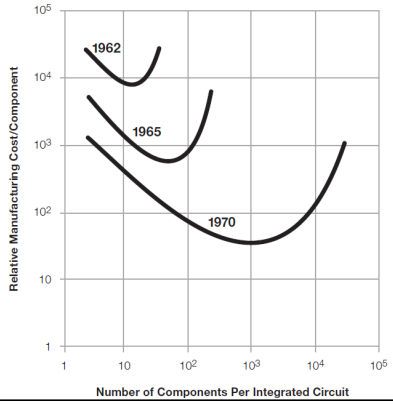


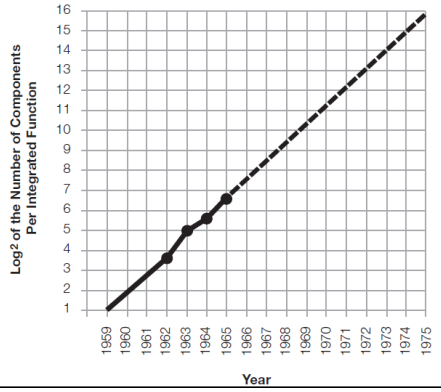
Fairchild µA702 op amp, created in 1964 by the team of process engineer Dave Talbert and designer Robert Widlar, was the first widely-used commercial product. Their 1965 successor, the µA709, established a mass market for analog ICs. Talbert and Widlar moved to Molectro (later acquired by National) in late 1965 where they built a linear dynasty beginning with the LM101. Then in 1968 Dave Fullagar of Fairchild one-upped the LM101 by adding an internal compensating capacitor to deliver the µA741, the most popular op-amp of all time.

Talbert and Widlar's µA709 high-performance operational amplifier (1965)

1.1. History: early days

- 1965 – Gordon Moore Law is born…
  - Co-founder of Fairchild (1957), Moore, Director R&D, publishes a prospective paper (Electronics, Volume 38, Number 8, April 19, 1965)





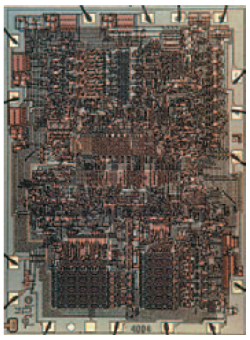
1.1. History: early days

- 1963 - Standard Logic IC Families introduced
  - Diode Transistor Logic (DTL) families create a high-volume market for digital ICs
  - Transistor Transistor Logic (TTL) as the most popular standard logic configuration by the late 1960s.
- 1968 - Silicon Gate Technology Developed for ICs
- 1968 - Noyce and Moore leave Fairchild to launch their own company Intel
- 1971 - Microprocessor Integrates CPU Function onto a Single Chip

1.1. History: manufacturing era

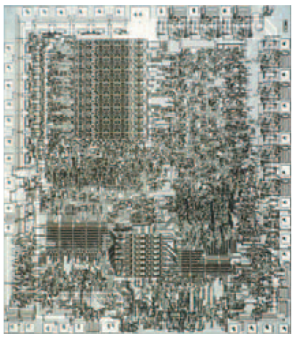
- Intel's manufacturing from 1971 till now…

1971



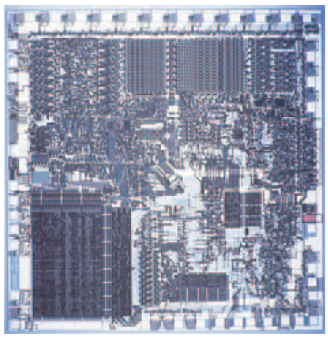
Intel® 4004 processor
Initial clock speed: 108KHz
Transistors: 2,300
Manufacturing technology: 10 micron

1974



Intel® 8080 processor
Initial clock speed: 2MHz
Transistors: 4,500
Manufacturing technology: 6 micron

1978

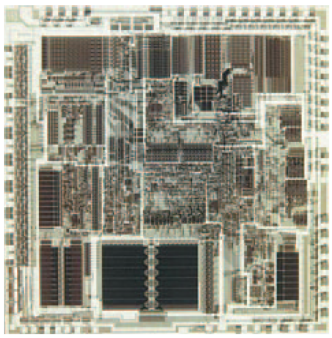


Intel® 8086 processor
Initial clock speed: 5MHz
Transistors: 29,000
Manufacturing technology: 3 micron

1.1. History: manufacturing era

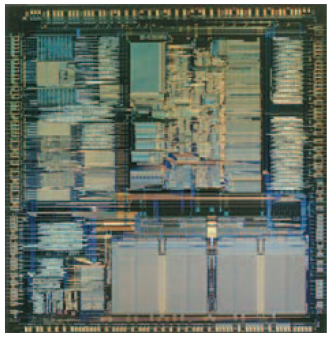
- Intel's manufacturing from 1971 till now…

1982



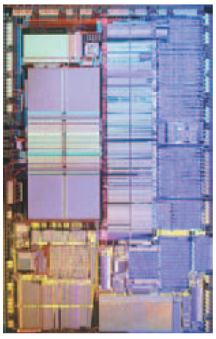
Intel® 286 processor
Initial clock speed: 6MHz
Transistors: 134,000
Manufacturing technology: 1.5 micron

1985



Intel386™ processor
Initial clock speed: 16MHz
Transistors: 275,000
Manufacturing technology: 1.5 micron

1989

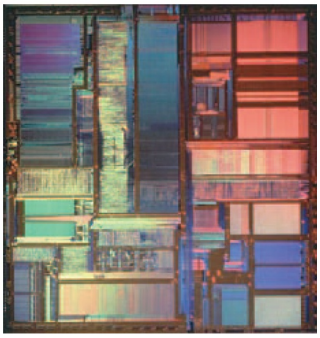


Intel486™ processor
Initial clock speed: 25MHz
Transistors: 1.2 million
Manufacturing technology: 1 micron

1.1. History: manufacturing era

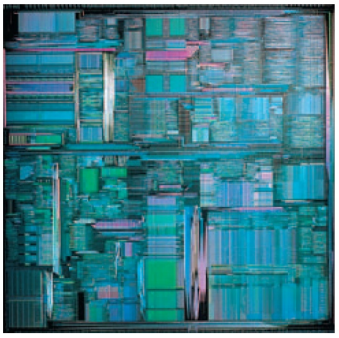
- Intel's manufacturing from 1971 till now…

1993



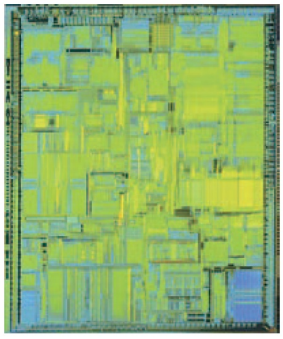
Intel® Pentium® processor
Initial clock speed: 66MHz
Transistors: 3.1 million
Manufacturing technology: 0.8 micron

1995



Intel® Pentium® Pro processor
Initial clock speed: 200MHz
Transistors: 5.5 million
Manufacturing technology: 0.35 micron

1999



Intel® Pentium® III processor
Initial clock speed: 600MHz
Transistors: 9.5 million
Manufacturing technology: 0.25 micron

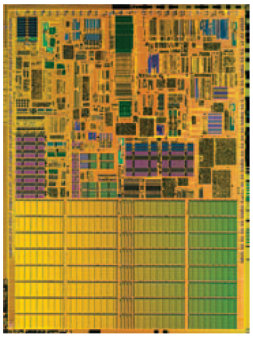
1.1. History: manufacturing era

- Intel's manufacturing from 1971 till now…

2000

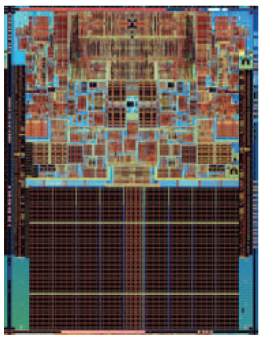
Intel® Pentium® 4 processor
Initial clock speed: 1.5GHz
Transistors: 42 million
Manufacturing technology: 0.18 micron

2003



Intel® Pentium® M processor
Initial clock speed: 1.7GHz
Transistors: 55 million
Manufacturing technology: 90nm

2006

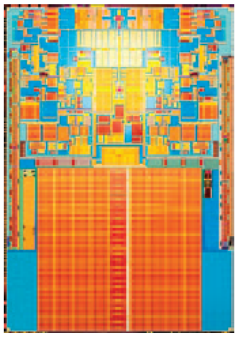


Intel® Core™2 Duo processor
Initial clock speed: 2.66GHz
Transistors: 291 million
Manufacturing technology: 65nm

1.1. History: manufacturing era

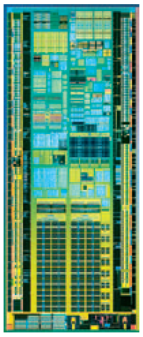
- Intel's manufacturing from 1971 till now…

2008



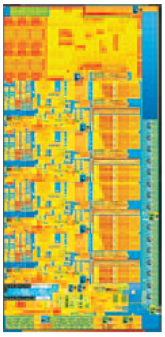
Intel® Core™2 Duo processor
Initial clock speed: 2.4GHz
Transistors: 410 million
Manufacturing technology: 45nm

2008



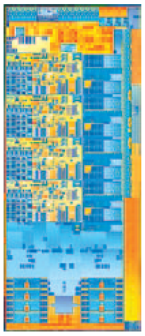
Intel® Atom™ processor
Initial clock speed: 1.86GHz
Transistors: 47 million
Manufacturing technology: 45nm

2010



2nd generation Intel® Core™ processor
Initial clock speed: 3.8GHz
Transistors: 1.16 billion
Manufacturing technology: 32nm

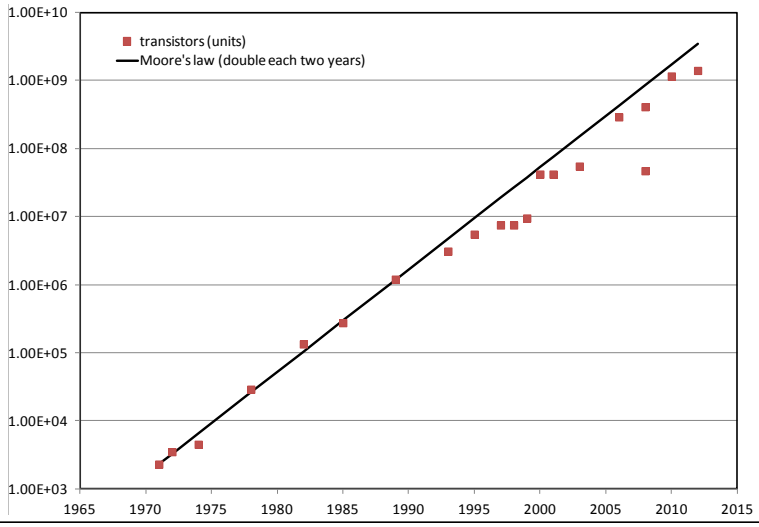
2012



3rd generation Intel® Core™ processor
Initial clock speed: 2.9GHz
Transistors: 1.4 billion
Manufacturing technology: 22nm

1.1. History: manufacturing era

- Intel's manufacturing from 1971 till now…



1.1. History: manufacturing era

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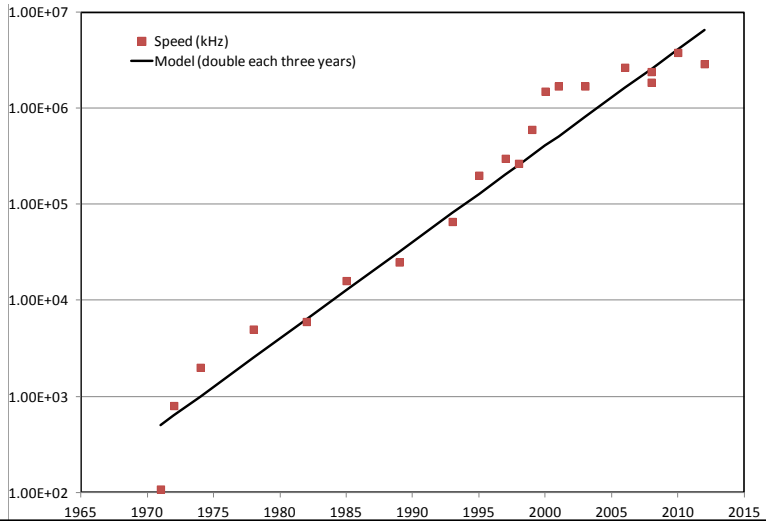
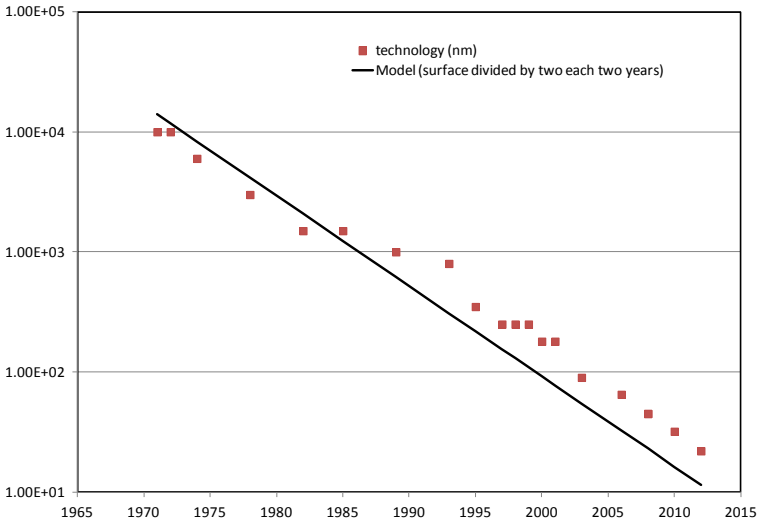


1.1. History: manufacturing era

- Intel's manufacturing from 1971 till now…



1.1. History: manufacturing era

- 1999 — Hitachi and NEC merged their DRAM businesses → **Elpida Memory**.
- 2001 — Hyundai and LG Sem. merged their semiconductor operations (**Hynix**).
- 2003 — Hitachi merged its Semiconductor & IC Division with Mitsubishi's System LSI Division to create **Renesas Technology**.
- 2003 —Mitsubishi's DRAM joined **Elpida Memory**.
- 2003 — **Matsushita** began emphasizing Panasonic as its main global brand name. Previously, Panasonic, National, Quasar, Technics, and JVC. In 2008, the company changed its name and the branding of products to Panasonic.
- 2004 —Motorola spun off its Semiconductor Products Sector (SPS) and the business was named **Freescale Semiconductor**.
- 2006 — Philips Semiconductor was renamed **NXP Semiconductors** after being spun out of Royal Philips Electronics as an independent company.
- 2010 — NEC merged with Renesas Technology to become **Renesas Electronics**.
- 2013 — Elpida is bought by **Micron Technology**.

1.1. History: manufacturing era

- Consumer electronics companies
- Integrated Device Manufacturer
- Foundries and fabless companies

Worldwide Semiconductor Sales Leaders ($B)

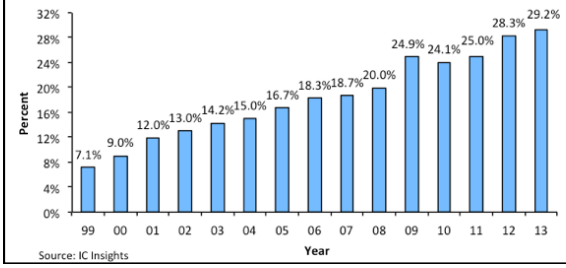
Rank	1985		1990		1995		2000		2006	
1	NEC	2.1	NEC	4.8	Intel	13.6	Intel	29.7	Intel	31.6
2	TI	1.8	Toshiba	4.8	NEC	12.2	Toshiba	11.0	Samsung	19.7
3	Motorola	1.8	Hitachi	3.9	Toshiba	10.6	NEC	10.9	TI	13.7
4	Hitachi	1.7	Intel	3.7	Hitachi	9.8	Samsung	10.6	Toshiba	10.0
5	Toshiba	1.5	Motorola	3.0	Motorola	8.6	TI	9.6	ST	9.9
6	Fujitsu	1.1	Fujitsu	2.8	Samsung	8.4	Motorola	7.9	Renesas	8.2
7	Philips	1.0	Mitsubishi	2.6	TI	7.9	ST	7.9	Hynix	7.4
8	Intel	1.0	TI	2.5	IBM	5.7	Hitachi	7.4	Freescale	6.1
9	National	1.0	Philips	1.9	Mitsubishi	5.1	Infineon	6.8	NXP	5.9
10	Matsushita	0.9	Matsushita	1.8	Hynudai	4.4	Philips	6.3	NEC	5.7
Top 10 Total ($B)		13.9		31.8		86.3		108.1		118.2
Semi Market ($B)		23.3		54.3		154		218.6		264.6
Top 10 % of Total Semi Mrkt		60%		59%		56%		49%		45%

Source: IC Insights

1.1. History: manufacturing era

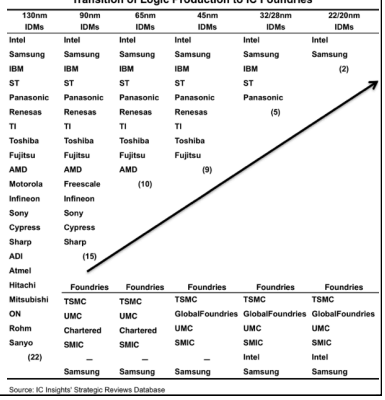
- An **Integrated Device Manufacturer (IDM)** is a semiconductor company which designs, manufactures, and sells integrated circuit (IC) products.
- A **Fabless** semiconductor company outsources production to a third-party (a **Foundry**) which manufactures IC products.

Fabless Company IC Sales as a Percent of Worldwide IC Sales (1999-2013)



Source: IC Insights

Transition of Logic Production to IC Foundries



Source: IC Insights' Strategic Reviews Database

1.1. History: manufacturing era

- **Fabless IC Suppliers**

Fall 2012	Amounts in US$M			
	2011	2012	2013	2014
Discrete S/C	21.387	19.303	20.351	21.540
Optoelectronics	23.092	25.989	27.775	29.477
Sensors	7.970	7.934	8.518	9.132
Integrated Circuits	247.073	236.710	246.410	258.618
Analog	42.338	39.683	41.120	43.521
Micro	65.204	60.316	62.075	64.959
Logic	78.782	80.543	85.461	90.375
Memory	60.749	56.167	57.754	59.764
Total Products	299.521	289.936	303.053	318.766

2013 Top 25 Fabless IC Suppliers

2013 Rank	2012 Rank	Company	Headquarters	2012 ($M)	2013 ($M)	% Change
1	1	Qualcomm	U.S.	13,177	17,211	31%
2	2	Broadcom	U.S.	7,793	8,219	5%
3	3	AMD	U.S.	5,422	5,299	-2%
4	5	MediaTek	Taiwan	3,366	4,587	36%
5	4	Nvidia	U.S.	3,965	3,898	-2%
6	6	Marvell	U.S.	3,144	3,352	7%
7	7	LSI	U.S.	2,506	2,370	-5%
8	8	Xilinx	U.S.	2,196	2,297	5%
9	9	Altera	U.S.	1,783	1,732	-3%
10	10	Avago	Singapore	1,479	1,619	9%
11	12	Novatek	Taiwan	1,256	1,398	11%
12	13	HiSilicon	China	1,178	1,355	15%
13	11	MStar	Taiwan	1,271	1,136	-11%
14	18	Spreadtrum	China	725	1,070	48%
15	14	CSR	Europe	1,025	961	-6%
16	15	Realtek	Taiwan	836	951	14%
17	16	Dialog	Europe	774	903	17%
18	19	Cirrus Logic	U.S.	714	772	8%
19	17	Himax	Taiwan	737	771	5%
20	21	Silicon Labs	U.S.	563	580	3%
21	22	MegaChips	Japan	553	577	4%
22	24	Semtech	U.S.	518	555	7%
23	23	PMC-Sierra	U.S.	531	508	-4%
24	25	IDT	U.S.	497	475	-4%
25	26	Microsemi	U.S.	450	433	-4%
		Top 25 Total	—	56,459	63,029	12%
		Other Total	—	15,650	14,882	-5%
		Total Fabless	—	72,109	77,911	8%

Source: Company reports, IC Insights' *Strategic Reviews* database

1.1. History: manufacturing era

2013 Top 20 Semiconductor Sales Leaders ($M, Including Foundries)

2013 Rank	2012 Rank	Company	Headquarters	2012 Tot IC	2012 Tot O-S-D	2012 Tot Semi	2013 Tot IC	2013 Tot O-S-D	2013 Tot Semi	2013/2012 % Change
1	1	Intel	U.S.	49,114	0	49,114	48,321	0	48,321	-2%
2	2	Samsung	South Korea	30,457	1,794	32,251	32,520	1,858	34,378	7%
3	3	TSMC*	Taiwan	16,951	0	16,951	19,850	0	19,850	17%
4	4	Qualcomm**	U.S.	13,177	0	13,177	17,211	0	17,211	31%
5	10	Micron***	U.S.	7,567	322	7,889	14,255	105	14,360	82%
6	8	SK Hynix	South Korea	9,057	0	9,057	12,970	0	12,970	43%
7	6	Toshiba	Japan	9,055	2,162	11,217	9,868	2,090	11,958	7%
8	5	TI	U.S.	11,376	705	12,081	10,794	680	11,474	-5%
9	11	Broadcom**	U.S.	7,793	0	7,793	8,219	0	8,219	5%
10	9	ST	Europe	6,227	2,137	8,364	5,847	2,167	8,014	-4%
11	7	Renesas	Japan	7,487	1,827	9,314	6,405	1,570	7,975	-14%
12	13	AMD**	U.S.	5,422	0	5,422	5,299	0	5,299	-2%
13	14	Infineon	Europe	3,078	1,850	4,928	3,402	1,858	5,260	7%
14	12	Sony	Japan	1,926	3,783	5,709	1,271	3,598	4,869	-15%
15	15	NXP	Europe	3,102	1,223	4,325	3,534	1,281	4,815	11%
16	22	MediaTek**	Taiwan	3,366	0	3,366	4,587	0	4,587	36%
17	17	GlobalFoundries*	U.S.	4,013	0	4,013	4,261	0	4,261	6%
18	19	Freescale	U.S.	3,180	571	3,751	3,371	636	4,007	7%
19	20	UMC*	Taiwan	3,730	0	3,730	3,959	0	3,959	6%

"Replacement" Top 20 Companies if Foundries are Excluded from the Ranking

2013 Rank	2012 Rank	Company	Headquarters	2012 Tot IC	2012 Tot O-S-D	2012 Tot Semi	2013 Tot IC	2013 Tot O-S-D	2013 Tot Semi	2013/2012 % Change
18	15	Fujitsu	Japan	3,805	357	4,162	3,210	299	3,509	-16%
19	23	Marvell*	U.S.	3,157	0	3,157	3,352	0	3,352	6%
20	20	Sharp	Japan	1,882	1,505	3,387	1,811	1,418	3,229	-5%

*Fabless

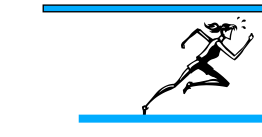
Source: Company reports, IC Insights' *Strategic Reviews* database

1.1. History: today and future…

- From Gordon Moore (1965):
  "There is no fundamental obstacle to achieving device yields of 100%. At present, packaging costs so far exceed the cost of the semiconductor structure itself that there is no incentive to improve yields, but they can be raised as high as is economically justified. It is not even necessary to do any fundamental research or to replace present processes. Only the engineering effort is needed."
- Was he right or wrong ? → So so…
  - Packaging costs are still higher than silicon bare die
  - Yield (at IC level) will never reach 100%
  - Yield (device level) is close to 100% (defects << ppm)
  - Process have been improved continuously for 50 years

→ Testing of manufactured dies is mandatory

1.1. History: today and future…



65 nm 45 nm 32 nm 22 nm ? nm → SOC

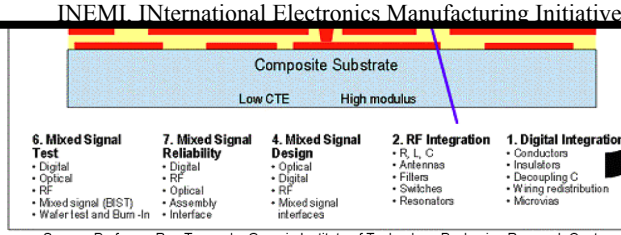
SIP/3D

MNEMS

3. Optical Integration 8. SIP 10. Thermal 9. SOC 5. Assembly Integration

«System in Package is characterized by any combination of more than one active electronic component of different functionality plus optionally passives and other devices like MEMS or optical components assembled preferred into a single standardpackage that provides multiple functions associated with a system or sub-system.»

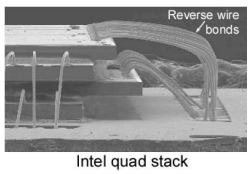
INEMI: INternational Electronics Manufacturing Initiative



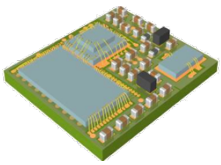
Source: Professor Rao Tummala, Georgia Institute of Technology-Packaging Research Center.

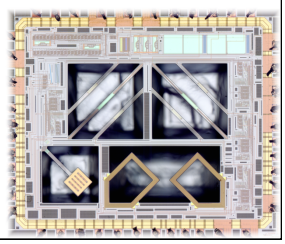
1.1. History: today and future…

- From electronic chips (SoC) towards embedded systems
  - Digital and Analog electronics
  - Software and Programmable hardware (FPGA)
  - Memory (both volatile and non-volatile)
  - RF and Non-electrical devices (sensors and actuators)
- Intensive integration → PCB, 3DIC, SiP, iMEMS…



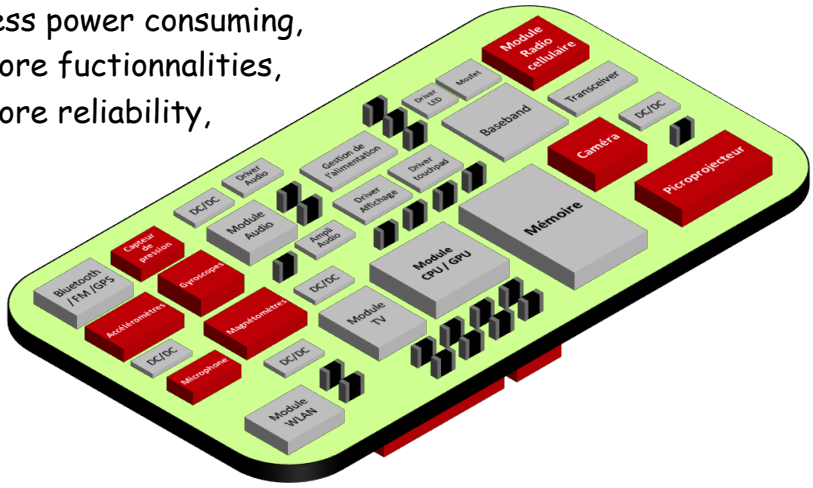
Intel quad stack





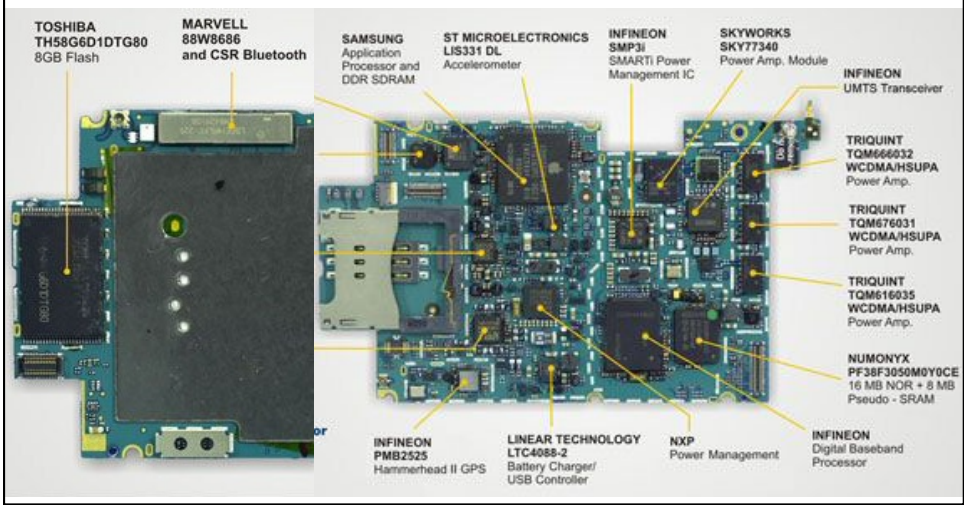
1.1. History: today and future…

- Roadmap for embedded systems
  - Always smaller and cheaper,
  - Less power consuming,
  - More fuctionnalities,
  - More reliability,
  - …
  -



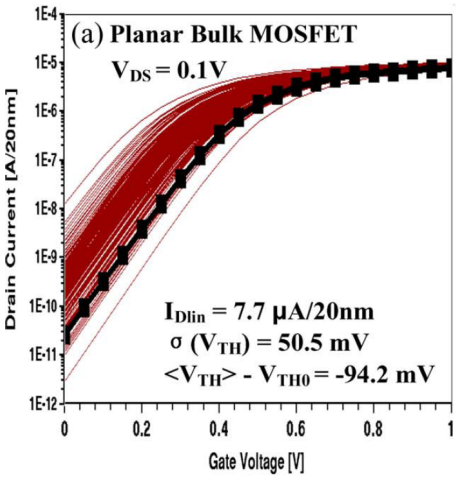
1.1. History: today and future…

- Embedded systems and market



1.1. History: today and future…

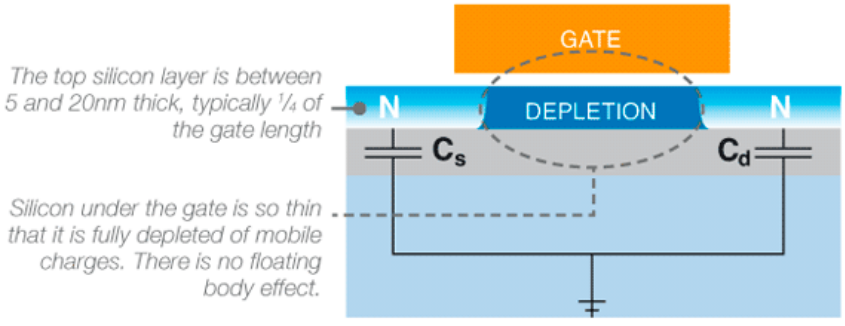
- Today: 22nm node
  - CMOS bulk with Na=10^{18} atoms/cm^3
  - What is the number of dopant in a minimum size channel?
  - Cubic volume of 22nm of side → 10^{-17} cm^3
  - 10 dopants !!!
    - Strong variability of the threshold voltage
    - Increase of leakage currents



"Study of Random-Dopant-Fluctuation (RDF) Effects for the Trigate Bulk MOSFET« , IEEE Trans. on Electron Devices, 56(7):1538-1542, July 2009.

1.1. History: today and future…

- Solutions for threshold voltage variability (and I_{on}/I_{off})
  - If substrate doping cannot be controlled then let's work with undoped silicon
  - Solution 1: SOITEC-ST Microelectronics → planar Fully-Depleted SOI (FD SOI)

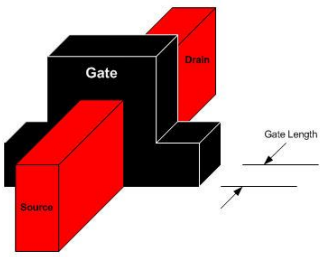


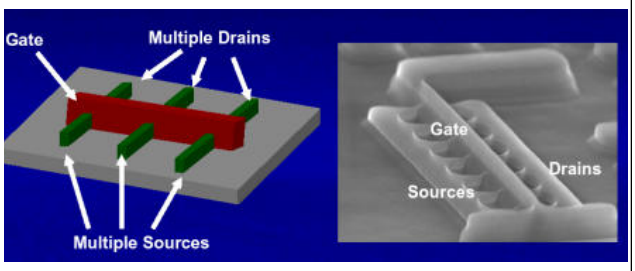
Fully depleted SOI MOS transistor cross-section

http://hothardware.com/News/SoiTec-Announces-New-SOI-Roadmap--Industry-Uptake-Remains-Unclear/

1.1. History: today and future…

- Solutions for threshold voltage variability (and I_{on}/I_{off})
  - If substrate doping cannot be controlled then let's work with undoped silicon
  - Solution 2: INTEL → 3D FinFETs or tri-gate transistors (Berkeley, 1999)





http://en.wikipedia.org/wiki/Multigate_device
https://eda360insider.wordpress.com/2011/06/19/are-finfets-inevitable-at-20nm-"yes-no-maybe"-says-professor-chenming-hu/

Outline

- History: five decades of innovations
- Overview of Microelectronics technology
- Elementary process steps
- CMOS process at a glance
- Layout basics and design rules
- Homework
- References

1.2. Microelectronic Technology: foundries, fabs and masks…

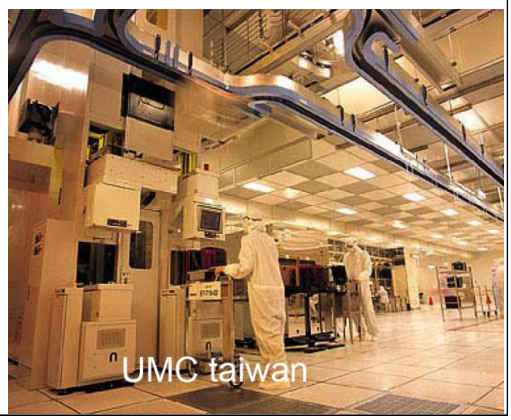
- Definitions (source Wikipedia, 2013)
  - An integrated circuit or monolithic integrated circuit (also referred to as an IC, a chip, or a microchip) is a set of electronic circuits on one small plate ("chip") of semiconductor material, normally silicon. This can be made much smaller than a discrete circuit made from independent components.
  - ICs can be made very compact, having up to several billion transistors and other electronic components in an area the size of a fingernail. The width of each conducting line in a circuit (the line width) can be made smaller and smaller as the technology advances; in 2008 it dropped below 100 nanometers and in 2013 it is expected to be in the tens of nanometers.
  - The front-end-of-line (FEOL) is the first portion of IC fabrication where the individual devices (transistors, capacitors, resistors, etc.) are patterned in the semiconductor. FEOL generally covers everything up to (but not including) the deposition of metal interconnect layers.

1.2. Microelectronic Technology: foundries, fabs and masks…

- Definitions (source Wikipedia, 2013)
  - The back end of line (BEOL) is the second portion of IC fabrication where the individual devices (transistors, capacitors, resistors, etc.) get interconnected with wiring on the wafer. BEOL generally begins when the first layer of metal is deposited on the wafer. BEOL includes contacts, insulating layers (dielectrics), metal levels, and bonding sites for chip-to-package connections.
  - After BEOL there is a "back-end process" (also called post-fab), which is done not in the cleanroom, often by a different company. It includes wafer test, wafer backgrinding (thickness reduction), die separation, die tests, IC packaging and final test.

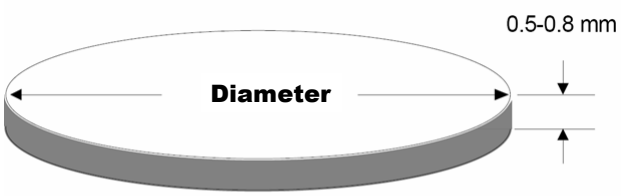
1.2. Microelectronic Technology: foundries, fabs and masks…

- An integrated circuit is obtained from a highly reliable process:
  - Batch fabrication
  - Reproducible
  - Large volumes
  - Automated
- This process makes use of photo-lithography:
  - Masks control the process



1.2. Microelectronic Technology: foundries, fabs and masks…

- Microelectronic Technology is based on a silicon wafer: the substrate that can contain hundreds of elementary chips



n-type: 3-5 Ω-cm

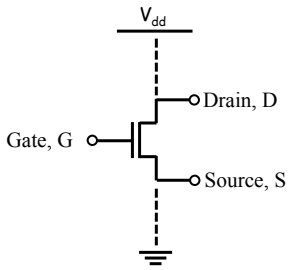
p-type: 14-16 Ω-cm

4" ⇒ 8" ⇒ 12"

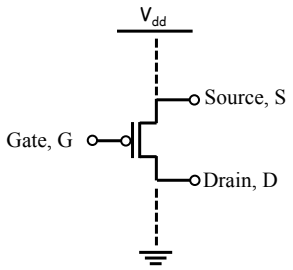
8" = 200mm ➔ 300mm ➔ 450mm

1.2. Microelectronic Technology: elementary devices in CMOS (1/2)

- N-channel MOS transistor



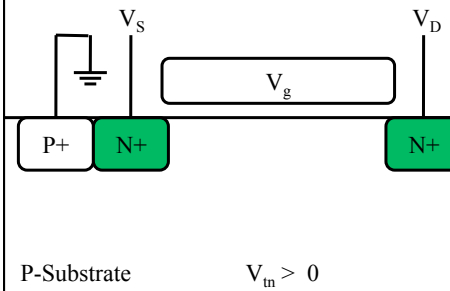
- P-channel MOS transistor



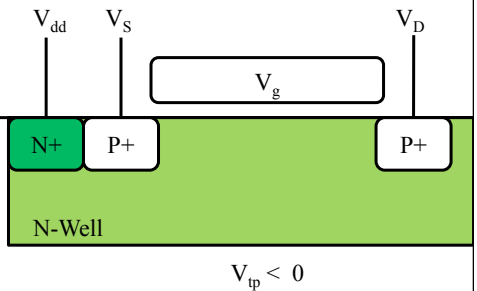
- Complementary MOS = CMOS
- Other symbols may exist
- Drain and Source are defined after biasing the transistor
- MOS transistor is a four terminal device

1.2. Microelectronic Technology: elementary devices in CMOS (2/2)

- MOST à canal N



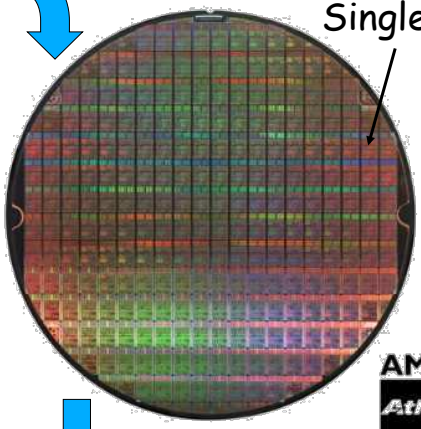
- MOST à canal P



- Other substrate may exist (N-Substrate, double-well, SOI)
- Source may be connected to substrate (well for PMOS)

1.2. Microelectronic Technology: from silicon to ICs…

FIGURE 1.2 Silicon ingot and silicon wafer. (*Courtesy of Dooson Company.*)

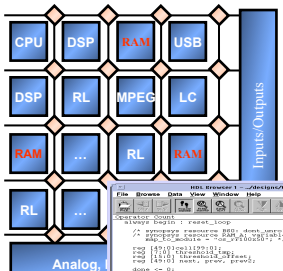


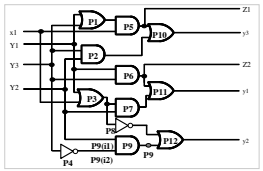
4" ⇒ 8" ⇒ 12"

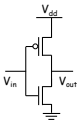
8" = 20 cm

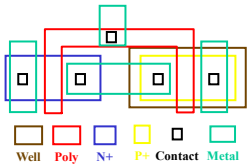
From http://www.amd.com

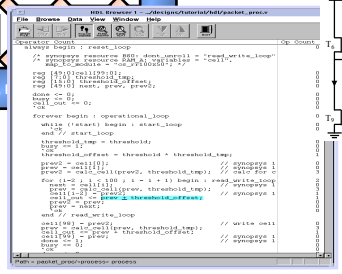
1.2. Microelectronic Technology: from design to manufacturing (1/2)…

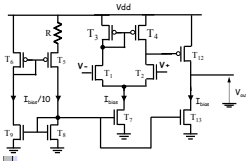


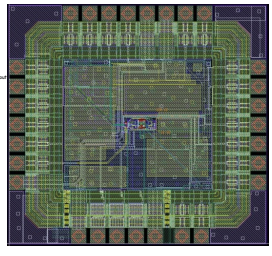










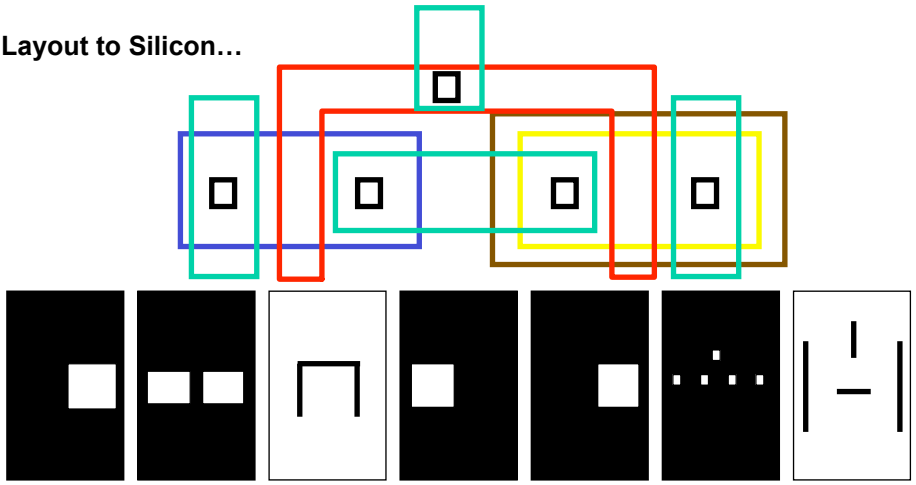


Architecture System Behavioral Circuit Layout …

Level

1.2. Microelectronic Technology: from design to manufacturing (2/2)…

Layout to Silicon…



Well Active Poly N+ P+ Contact Metal

Photolithography Masks

Outline

- History: five decades of innovations
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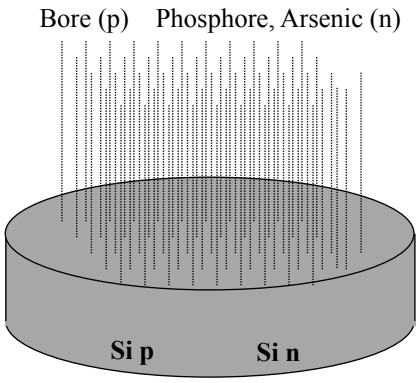
1.3. Elementary process steps

Full wafer ☑

Mask required ☒

Mask possible ☑

Ion Implantation



1.3. Elementary process steps

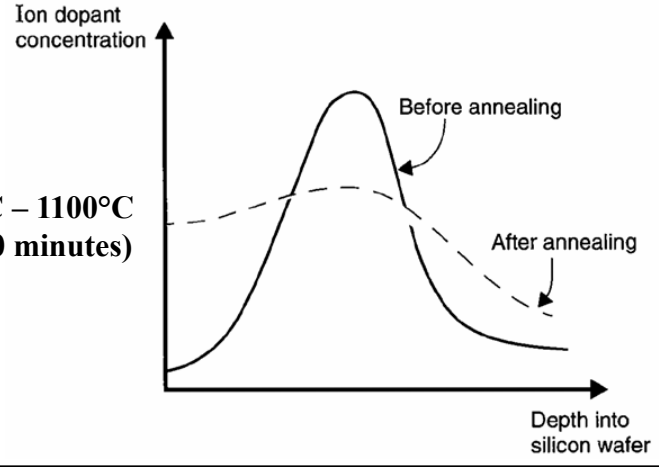
Full wafer ☑

Mask required ☒

Mask possible ☒

Annealing

900°C – 1100°C
(15-30 minutes)



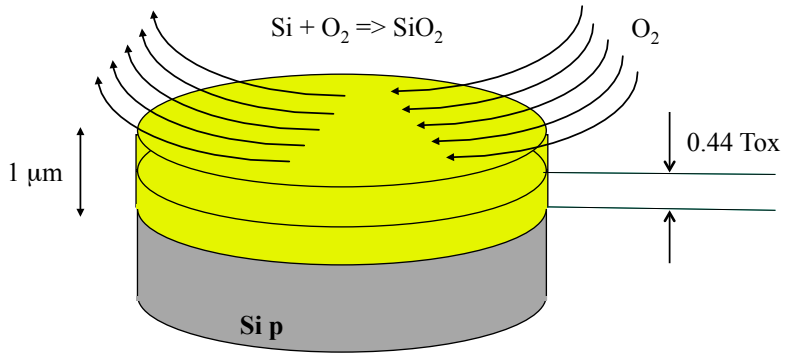
1.3. Elementary process steps

Full wafer ☑

Mask required ☒

Mask possible ☑

Oxydation



1.3. Elementary process steps

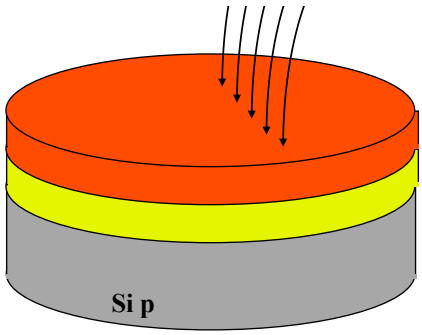
Full wafer ☑

Mask required ☒

Mask possible ☑

Deposition

Silicon nitride (Si3N4)
Silicon dioxide (SiO2)
Aluminum
Polysilicon, …



- Spin coating
- Chemical-vapor deposition (CVD)
- Low-pressure chemical-vapor deposition (LPCVD)
- Plasma-assisted chemical-vapor deposition (PECVD)
- Sputter deposition

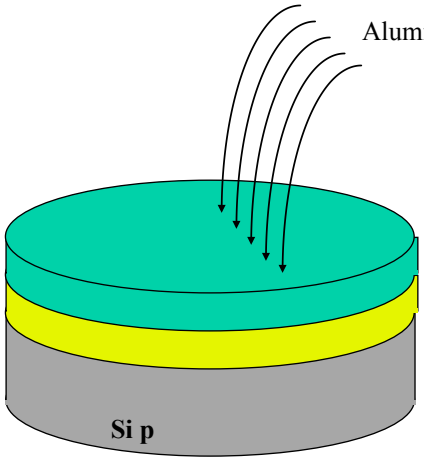
1.3. Elementary process steps

Full wafer ☑

Mask required ☑

Mask possible ☒

Evaporation

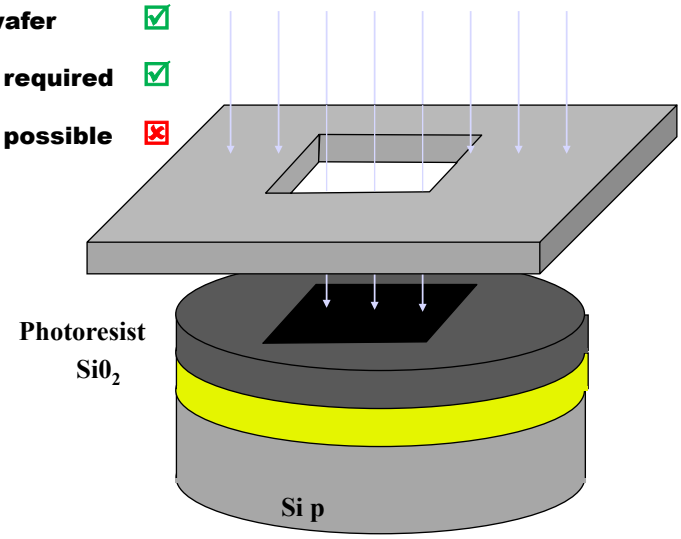


1.3. Elementary process steps

Full wafer ☑

Mask required ☑

Mask possible ☒



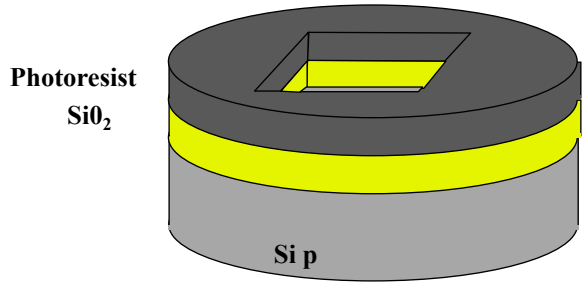
Photolithography

1.3. Elementary process steps

Full wafer ☑

Mask required ☒

Mask possible ☑



Etching

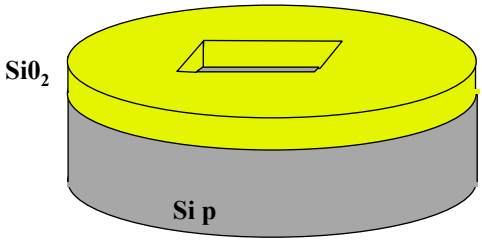
1.3. Elementary process steps

Full wafer ☑

Mask required ☑

Mask possible ☒

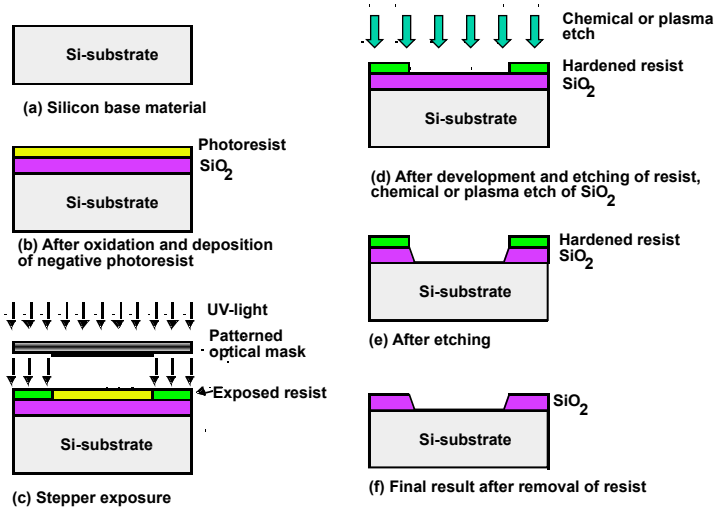
Diffusion



Gaz ($2PH_3$+$4O_2$) + 1000°C

Alternative: Ion Implantation + Annealing

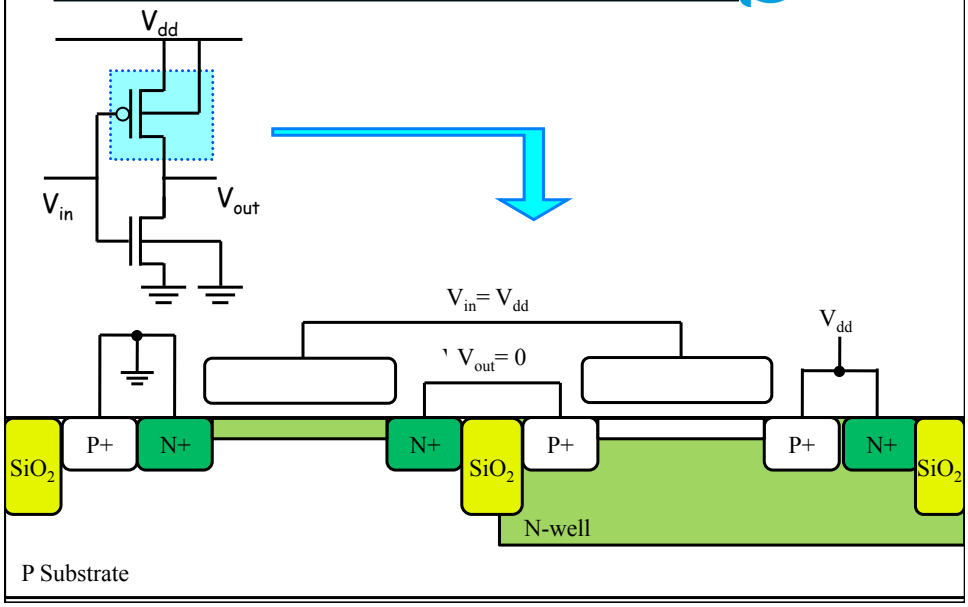
1.3. Elementary process steps: full process for SiO_2 patterning



Outline

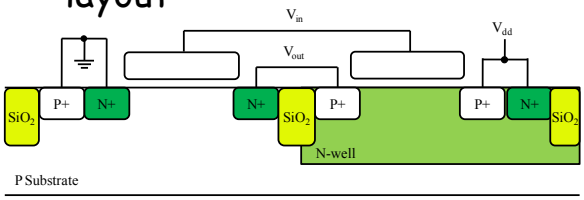
- History: five decades of innovations
- Overview of Microelectronics technology
- Elementary process steps
- CMOS process at a glance
- Layout basics and design rules
- Homework
- References

1.4. CMOS Process at a glance: application to a basic inverter



1.4. CMOS Process at a glance: application to a basic inverter

- A CMOS process is defined by the realization of elementary steps in a specific order.
- Each step is controlled by a mask inherited from the layout



Define active areas
Etch and fill trenches

Implant well regions

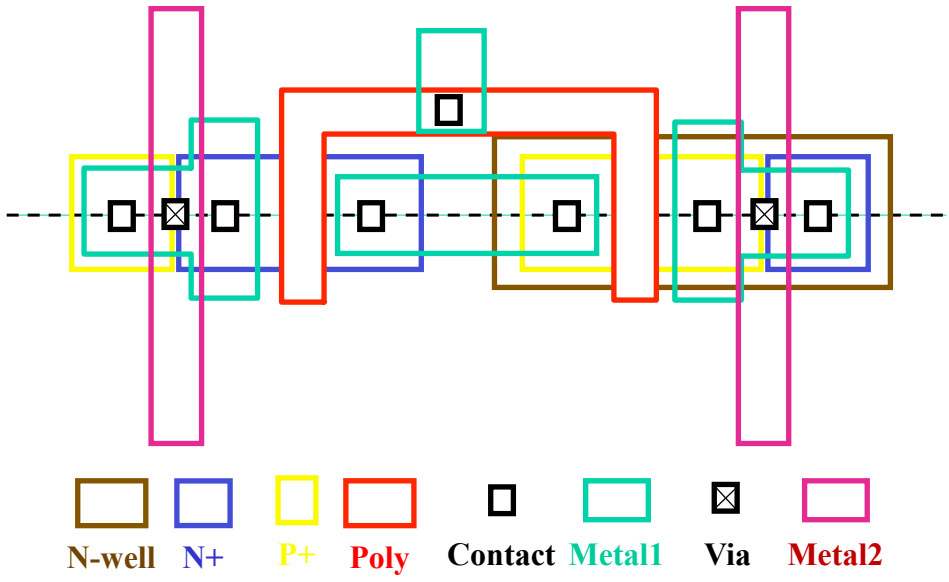
Deposit and pattern polysilicon layer

Implant source and drain regions and substrate contacts

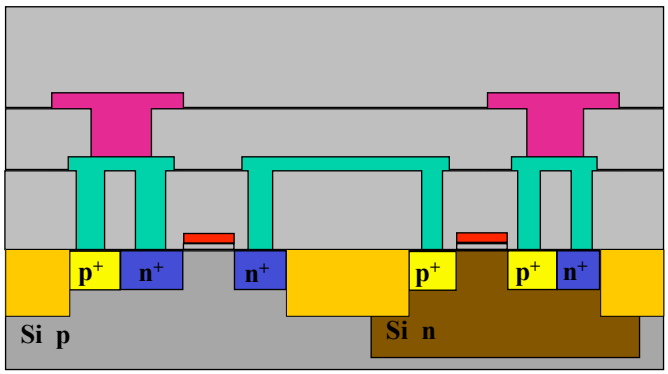
Create contact and via windows
Deposit and pattern metal layers

Interactive Java Application

1.4. CMOS Process at a glance: application to a basic inverter



1.4. CMOS Process at a Glance: application to a basic inverter

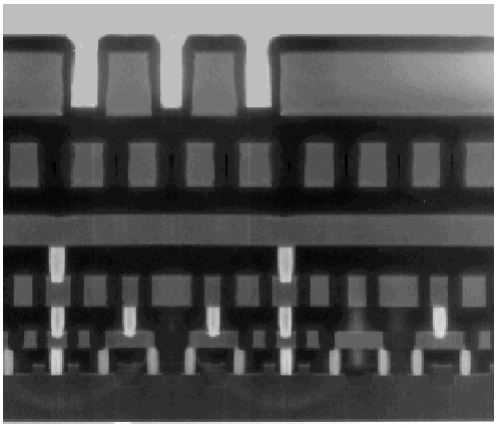


1.4. CMOS Process at a Glance: Intel 0.25 µm

5 metal layers
Ti/Al - Cu/Ti/TiN

LAYER	PITCH	THICK	A.R.
Isolation	0.67	0.40	-
Polysilicon	0.64	0.25	-
Metal 1	0.64	0.48	1.5
Metal 2	0.93	0.90	1.9
Metal 3	0.93	0.90	1.9
Metal 4	1.60	1.33	1.7
Metal 5	2.56	1.90	1.5
	µm	µm	

Layer pitch, thickness and aspect ratio



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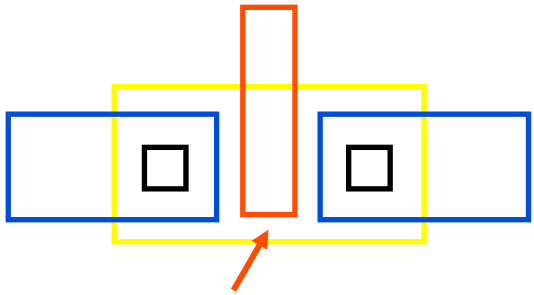
1.5. Layout basics and design rules

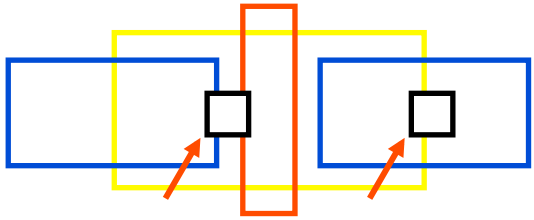
Impact of polysilicon mask misalignment ?



N-Well N+ P+ Poly Contact Metal1

1.5. Layout basics and design rules

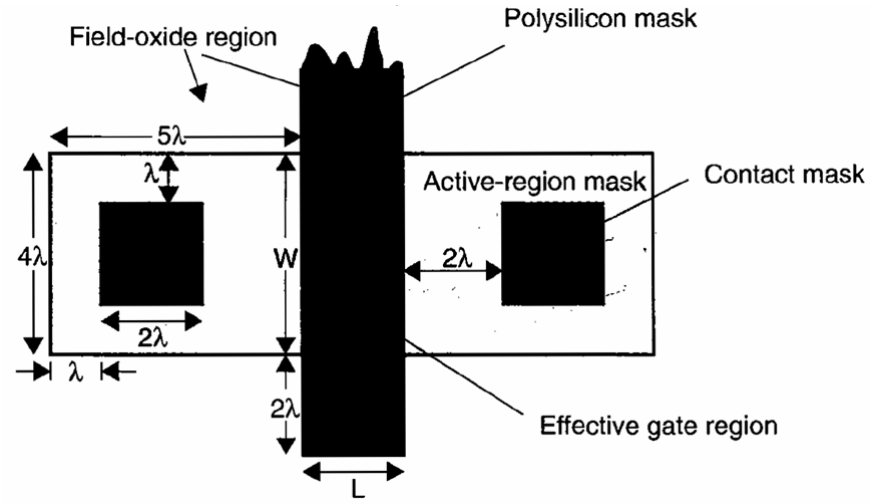
Impact of contact mask misalignment ?



N-Well N+ P+ Poly Contact Metal1

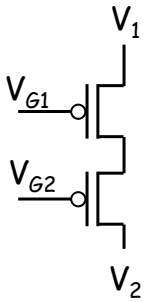
1.5. Layout basics and design rules

Design rules to prevent mask misalignment impact !



1.5. Layout basics and design rules

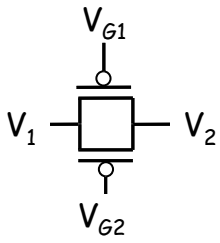
Serial connection of a pair of MOS transistors ?



N-Well N+ P+ Poly Contact Metal1

1.5. Layout basics and design rules

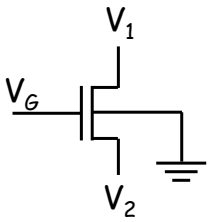
Parallel connection of a pair of MOS transistors ?

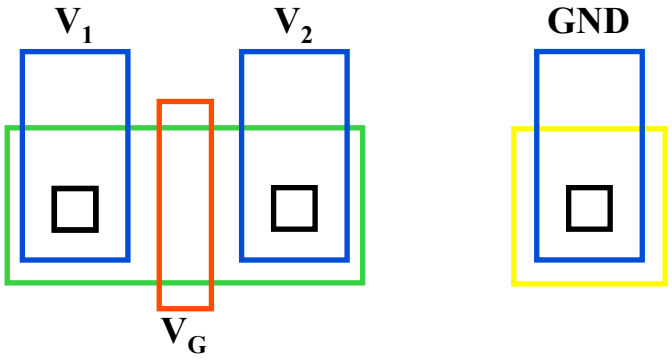


N-Well N+ P+ Poly Contact Metal1

1.5. Layout basics and design rules

P-substrate biasing

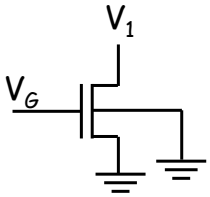


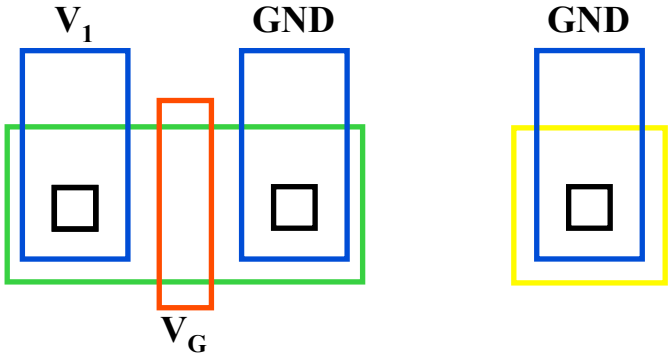


N-Well N+ P+ Poly Contact Metal1

1.5. Layout basics and design rules

P-substrate biasing: grounded source ?

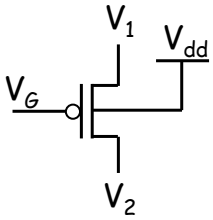


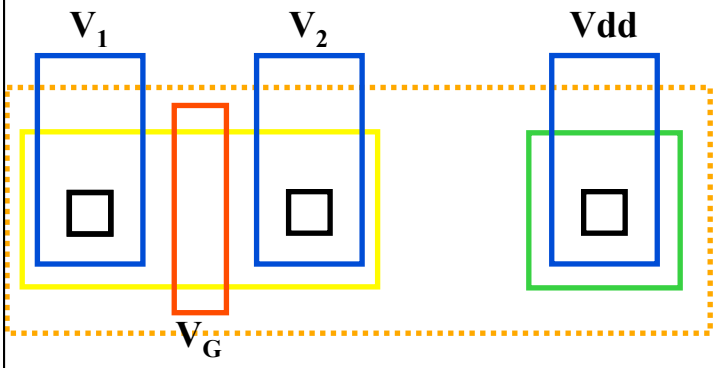


N-Well N+ P+ Poly Contact Metal1

1.5. Layout basics and design rules

N-well biasing

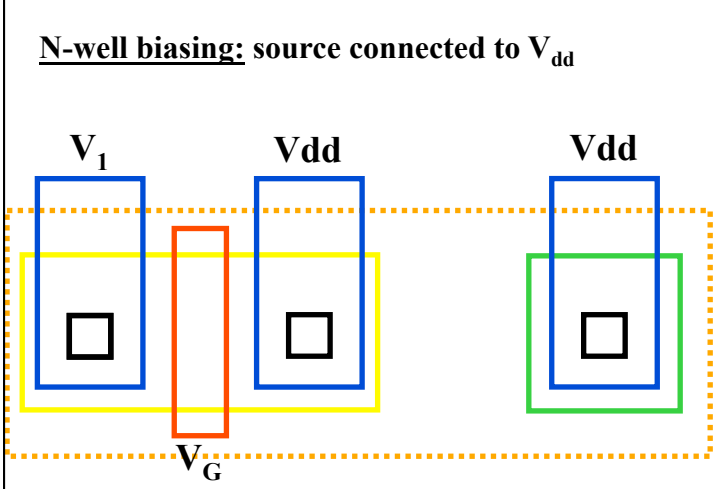


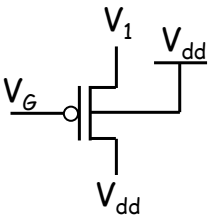


N-Well N+ P+ Poly Contact Metal1

1.5. Layout basics and design rules

N-well biasing: source connected to V_{dd}





N-Well N+ P+ Poly Contact Metal1

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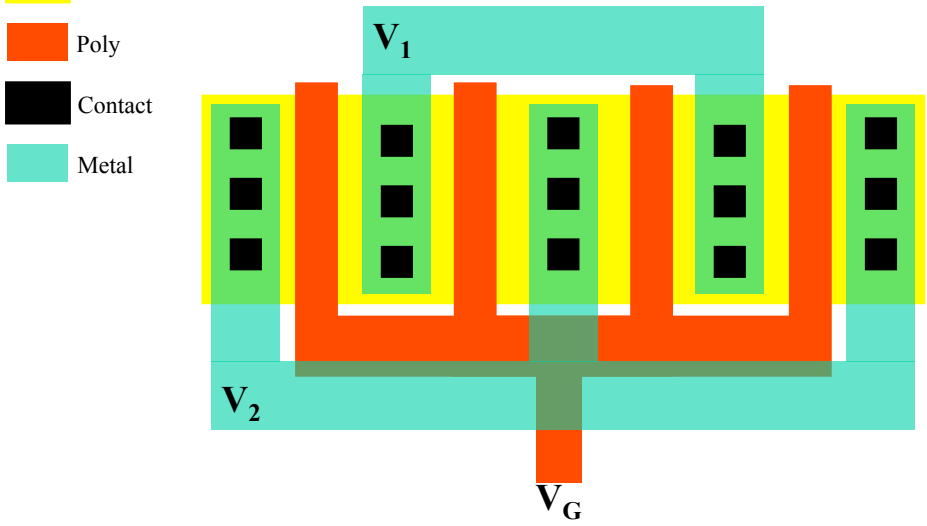
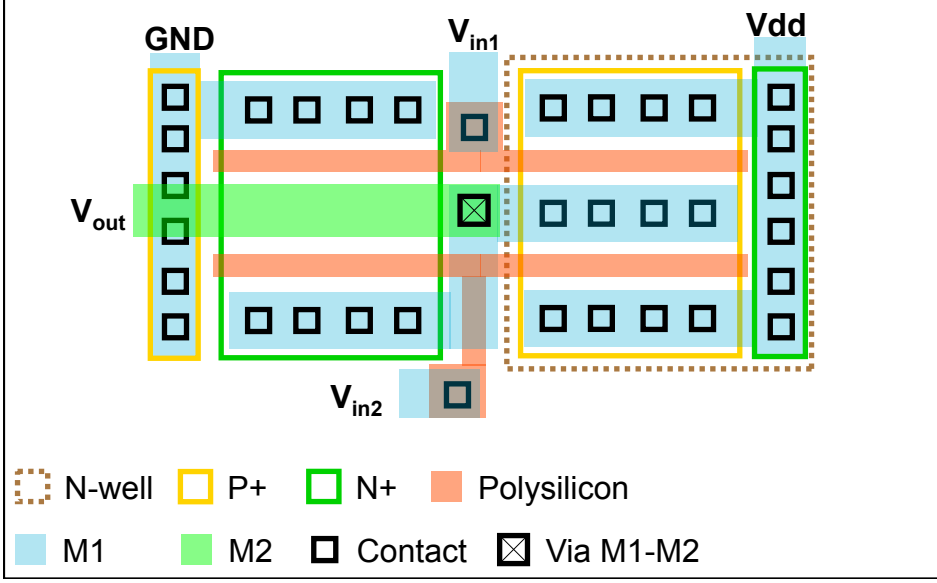
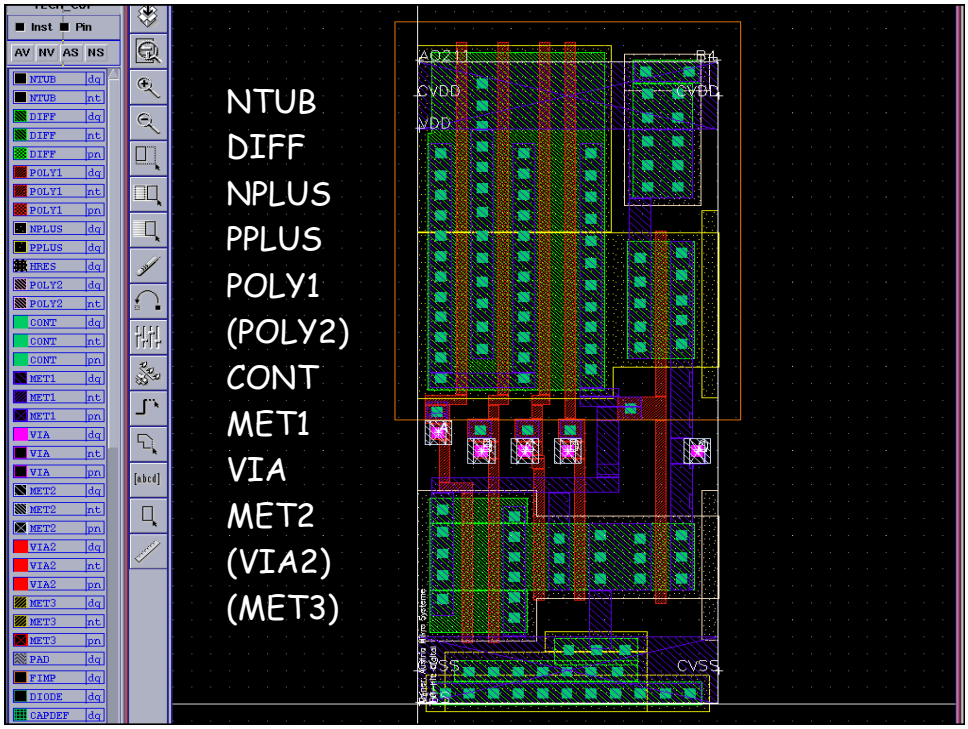
1.6.1. Homework: identification of a layout



1.6.2. Homework: identification of a layout – digital gate





1.7. References and further readings

- http://www.computerhistory.org/semiconductor/timeline.html
- www.inemi.org
- www.amd.com
- www.intel.com
- IC Insights, http://www.icinsights.com/
- www.youtube.com
- Applets Java pour la fabrication d'un inverseur
  http://jas.eng.buffalo.edu/education/fab/invFab/
- Remerciements : Michel Renovell
  « CAO des Circuits Intégrés » - Cours M1 EEA Université Montpellier II