Session 1: Introduction to Microelectronics
Labs & Homework

1. Start-up a Cadence Virtuoso Session

From Home (Polytech users): connect to the VPN @ Polytech first then open your VNC session…

From CAO1 (Polytech users): you can open your VNC session or a new session directly on MEARH14

Then, to setup a new install of Cadence (recommended), create a new directory, go into that directory and source the configuration file:

/soft_eii/2015/Configs/AMS_HK410_Analogique.csh

By sourcing this file, you're choosing to work with AMS 0.35 µm mixed-signal technology. Remember that this file must be sourced each time when you want to launch Cadence from your Cadence's install directory.

From this directory you can now launch Cadence Virtuoso: ams_cds –tech c35b4 –mode virt

The first time you're launching Cadence, you need to choose your process options. Choose one with Hi Resistivity Polysilicon (HiRes).

Anytime during this lab, beginner's tutorials may be used to help if needed.

2. Layout of a MOS transistor

Create a new library and a new cellview (for layout) and place in it an instance of both pmos4 and nmos4 transistor (these instance are available in the PRIMLIB directory).

2.1. Select an instance and open the properties' window (short-cut is q)

Explore parameters that affect the layout of the MOST by observing what happens when changing width and length, number of gates (integer), shape and bends (integer), top and bottom contacts, join parameters, guard bar parameters and substrate contact.

Evaluation: write a small document typically one page where you describe the effect of each parameter on the layout. Join this document to your Lab & HW report.

2.2. Play with the visibility to identify layers

By selecting a layer and clicking the NV (Non-Visible) button, all shapes except those using the selected layer will disappear. Then, just click layers to make them visible again. ***Tip: by clicking "Used" on the top left of the window, only layers used in the layout will be in the list.***

Evaluation: For each of this elementary element, list the name of the layers that must be superimposed in this technology (e.g., N+ contact requires DIFF, NPLUS, CONT, MET1)

p-type diffusion:

n-type diffusion:

polysilicon wire:

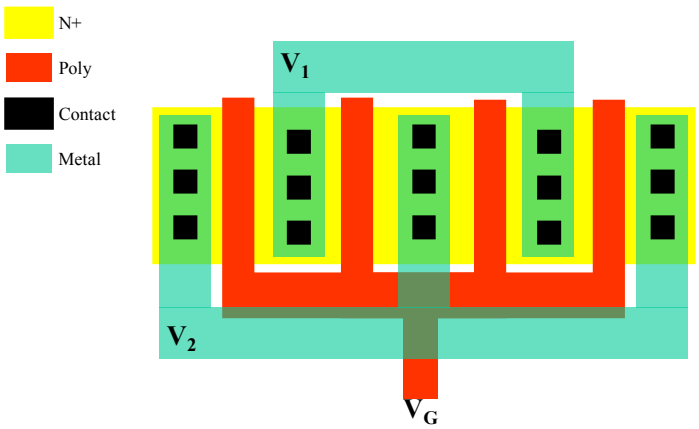
metal wire:

p+ contact in an N-well:

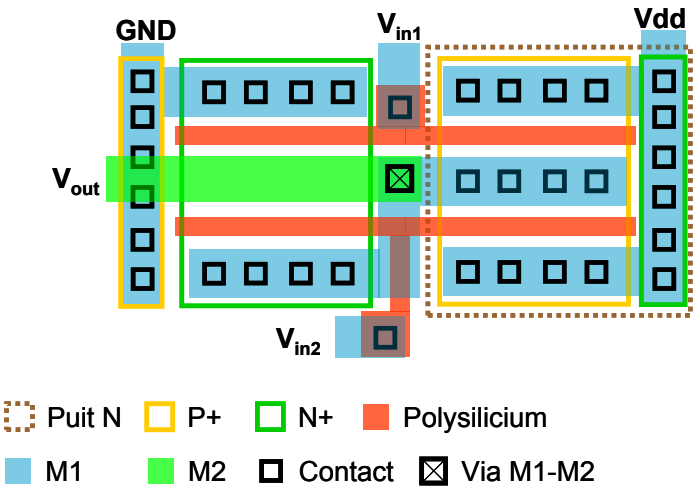
PMOS transistor:

3. Layout reading

1) After analyzing the layout below, draw beside of it the schematic with indications of W/L ratio for each transistors and label V_1, V_2 and V_G on the correct wire. Write few words to describe what is implemented in this layout.



2) After analyzing the layout below, give the schematic you obtain with indications of W/L ratio for each transistors and label GND, V_{dd}, V_{in1}, V_{in2} and V_{out} on the correct wire. Write beside the logical function implemented by this layout.



3) Open layout AOI310 in library corelib. After analyzing it, answer the following questions:

- Silicon area of the cell :
- Number of transistors: ……. with ……. NMOS and ……. PMOS
- Number of I/Os: ……. with ……. Inputs and ……. outputs
- Equation of the so-obtained logical function:
- Give below a well-organized transistor-level schematic of the cell with name of I/O and dimensions.

Tips: identify first the layer used to give the name to inputs and outputs of the cell. By pressing k on the keyboard, you will obtain the ruler function.