Polytech'Montpellier – MEA4
M2 EEA – Systèmes Microélectroniques

Analog IC Design

Building a DC Small-Signal Model of a CMOS Analog Circuit: a comprehensive guide

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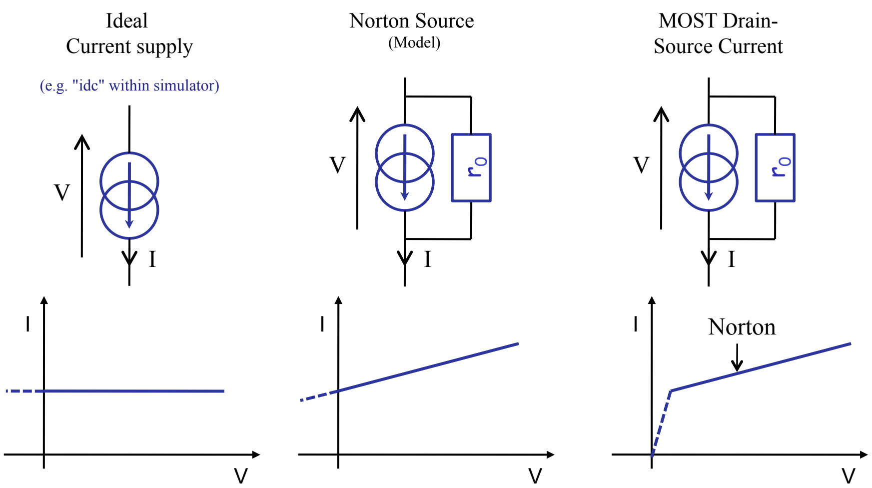
http://www.lirmm.fr/~nouet/homepage/lecture_ressources.html

Objective / Content

- Demystify the building of a low-frequency (dc) small-signal model for your CMOS analog circuit
- A step by step straightforward approach
- Pre-requisites
  - Good practice of solving electrical circuits (Node and Mesh laws)
  - Large- and small-signal models for MOST in strong-inversion
- Content
  - A comprehensive guide
  - A set of exercises
  - Good practice of solving small-signal circuits

From Norton (Current) Source to MOS transistor

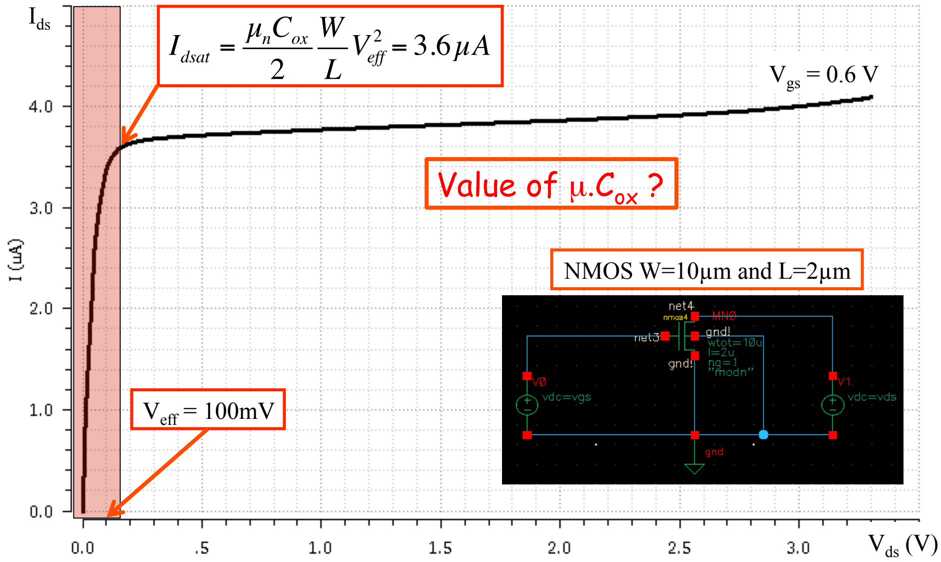
Practical Current Source ≠ Current supply



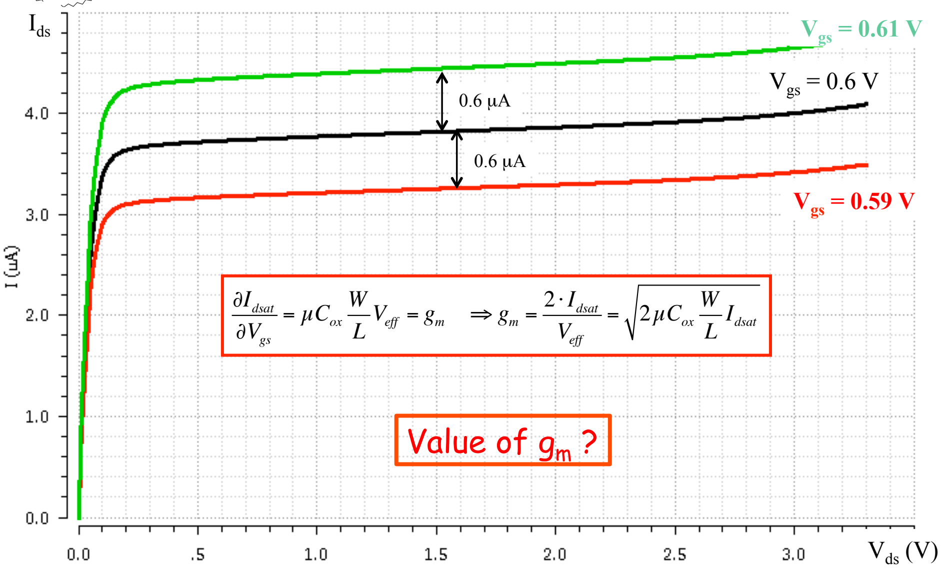
Outline

- Large- and small-signal models for MOST in strong-inversion
  - Overview of theoretical background
  - Experiments
- DC Small-Signal Model of a CMOS Analog Circuit
  - Step-by-step method
  - Practical example
- Exercises
  - A basic Voltage source : determine V_{dd} dependency
  - A basic Current source : output resistance and V_{dd} dependency
  - A basic amplifier : voltage gain

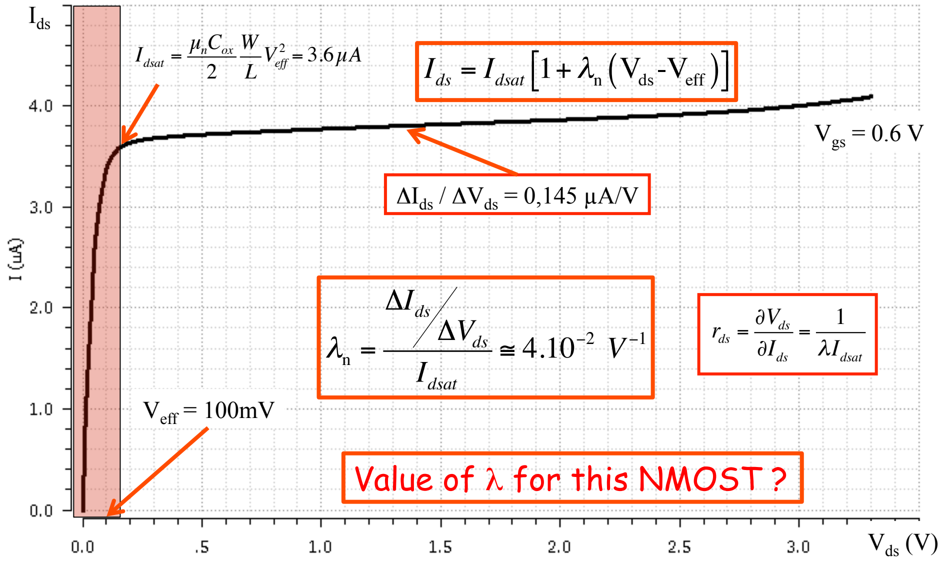
Large-signal model of the MOS transistor: saturation current, I_{dsat}



Small-signal model of the MOS transistor: transconductance, g_m

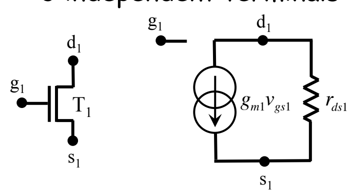


Small-signal model of the MOS transistor: output resistance, r_{ds}

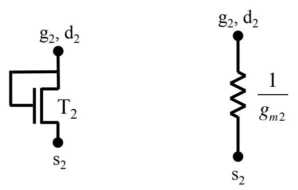


Pre-requisite summary

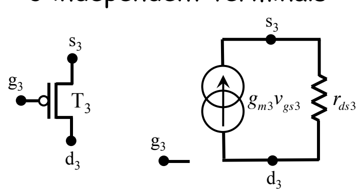
- N-type MOS transistor SSM in strong inversion
  - 3 independent terminals



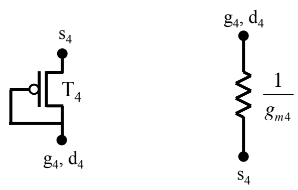
  - 2-terminal (diode-like)



- P-type MOS transistor SSM in strong inversion
  - 3 independent terminals



  - 2-terminal (diode-like)



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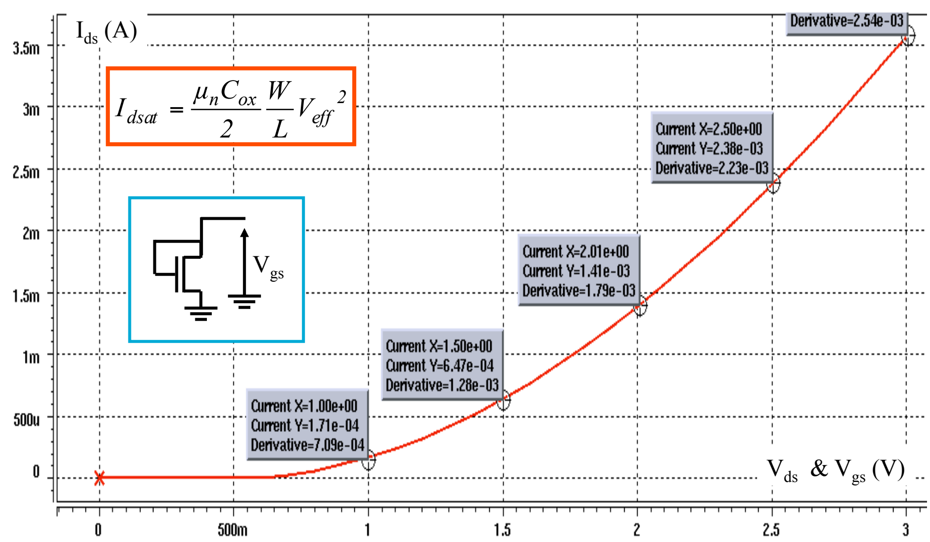
Characterization of a diode-connected NMOS Transistor



Characterization of a diode-connected NMOS Transistor

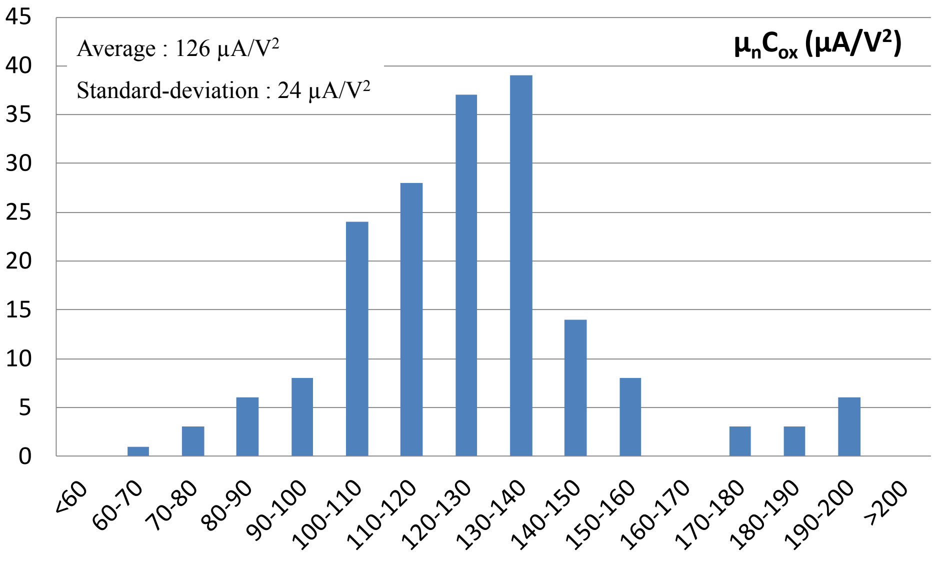
V_{eff} (V)	0.5	1	2
I_{dsat} (μA)	171	647	2380
$\delta I_{ds}/\delta V_{gs}$ (mA/V)	0.709	1.28	2.23
$\mu_n C_{ox}$ (A/V²)	1.42e-4	1.28e-4	1.12e-4
$\mu_n C_{ox}$ (A/V²)	1.37e-4	1.29e-4	1.19e-4

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \mu_n C_{ox} \frac{W}{L} V_{eff} \Rightarrow \mu_n C_{ox} = \frac{g_m}{\frac{W}{L} V_{eff}}$$

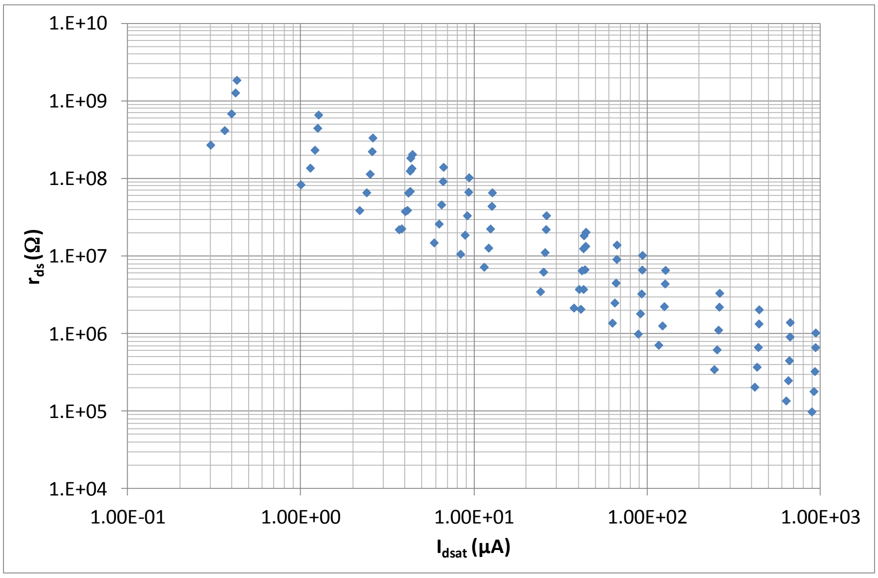
$$\mu_n C_{ox} = 2 I_{dsat} \Big/ \left(\frac{W}{L} V_{eff}^2 \right)$$

μ_n.Cox = 112 to 142 μA/V²

Characterization of a diode-connected NMOS Transistor



Characterization of r_{ds} (PMOS)



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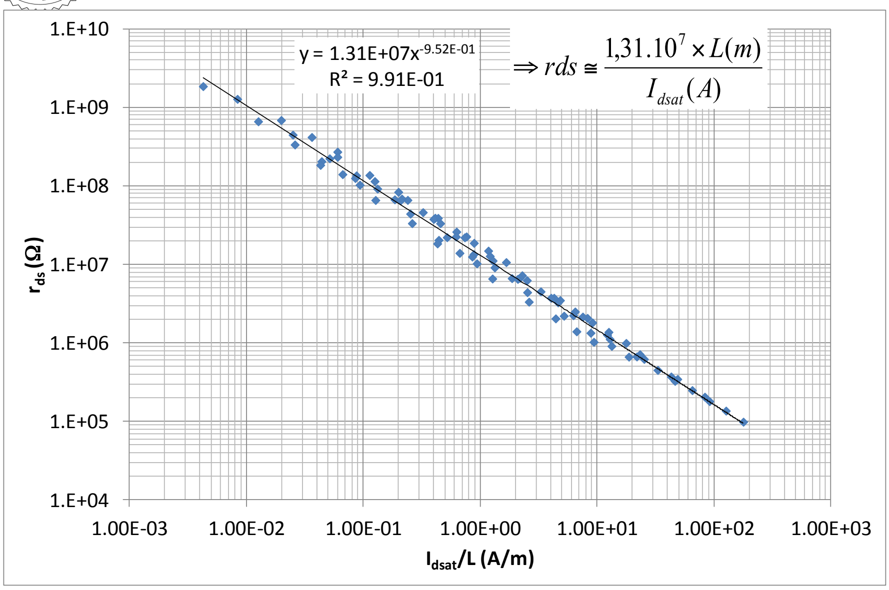


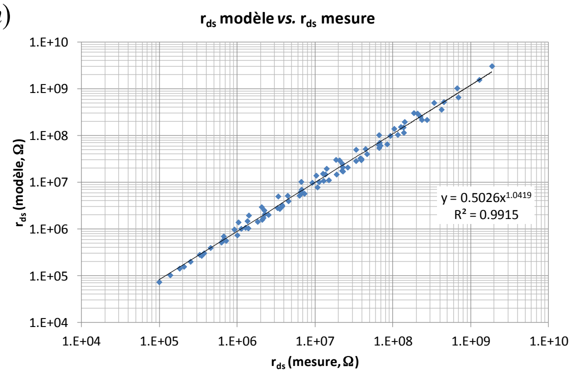
Characterization of λ_p

$$I_{ds} = I_{dsat}\left[1+\lambda\left(V_{ds}-V_{eff}\right)\right] \text{ avec } \lambda = \frac{k_{ds}}{2L_{eff}\sqrt{V_{ds}-V_{eff}+\Phi_0}} \qquad k_{ds} = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{qN_a}}$$

$$r_{ds} \cong \frac{13{,}1\times L(\mu m)}{I_{dsat}(A)} \Rightarrow \lambda_p = \frac{76mV^{-1}}{L(\mu m)}$$

- Standard deviation $\pm 25\%$
- Fixed length design (e.g. L=10µm)

➔ $\lambda_p = 7{,}65.10^{-3}V^{-1}$



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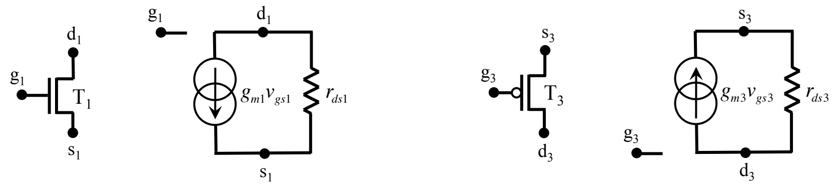
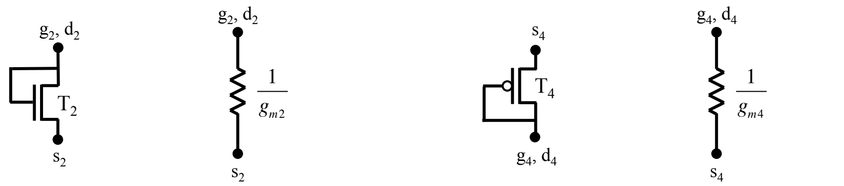
  - 3 independent terminals
- P-type MOS transistor SSM in strong inversion
  - 3 independent terminals



- N-type: 2-terminal (diode-like)
- P-type: 2-terminal (diode-like)



The step-by-step method

- ***All the steps below will be easier and you will reduce the risk of error if you keep the initial circuit topography for your small-signal model…***
- Step 1: identify your input i.e. the magnitude that will vary during your small-signal analysis and keep-it unaltered anytime
- Step 2: replace I and V sources by their small-signal model
- Step 3: replace each transistors by their small-signal model including labels for g, d, s
- Step 4: add electrical connections as in your initial circuit
- Step 5: identify all required v_{gs} and eliminate related voltage-controlled current sources when v_{gs}=0
- Step 6: identify your output variable, eventually rearrange your circuit and solve the obtained circuit

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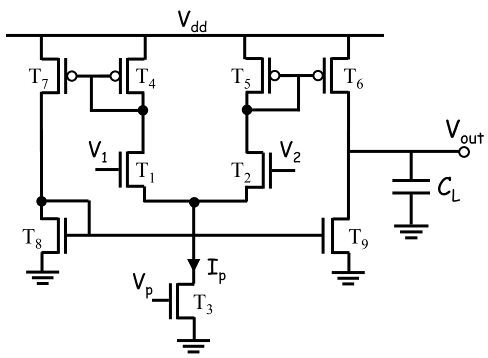
Building a small-signal model

- Let's determine the small-signal output resistance of this Operational Transconductance Amplifier



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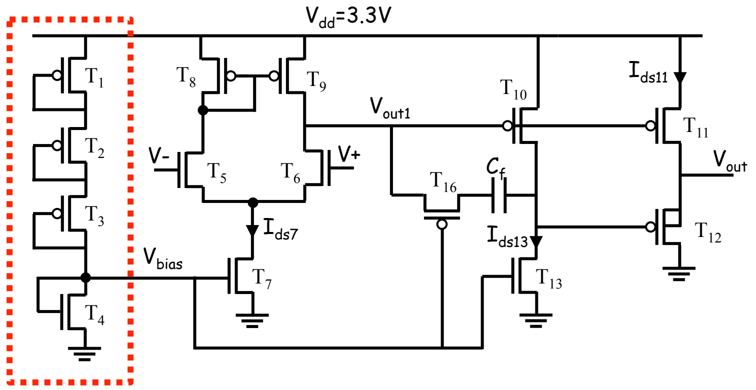
Your first Analog Design



Voltage Reference

Homework & Lab

- Homework
  - Choose size of T_1 to T_4 for V_{bias}=0.6V and I_{T1}=10μA
  - Derive a small-signal model of the circuit to determine sensitivity to V_{dd} of both V_{bias} and I_{T1}
  - Compute these sensitivities
- Lab
  - Verify the biasing point using an 'Operating Point' simulation (both V_{bias} and I_{T1})
  - Verify the sensitivity to V_{dd} of the biasing point using a 'DC' simulation (both V_{bias} and I_{T1})

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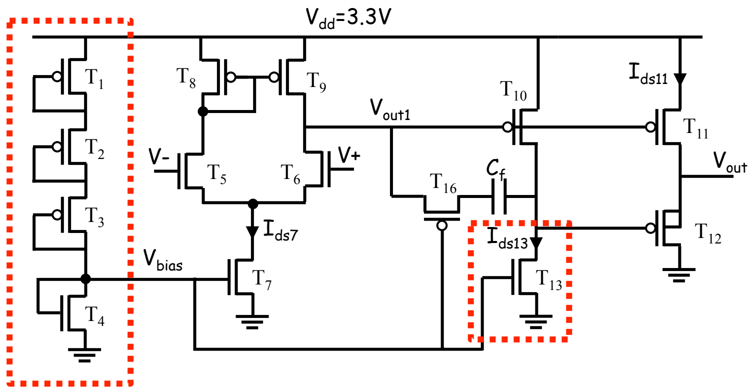

Voltage Reference

Current Source

Homework & Lab

- Homework
  - Design T_{13} for I_{T13}=50μA
  - Derive a small-signal model of the circuit to determine r_{out}
  - Compute r_{out}
- Lab
  - Verify the biasing point using an 'Operating Point' simulation (I_{T13})
  - Verify the output resistance using a 'DC' simulation

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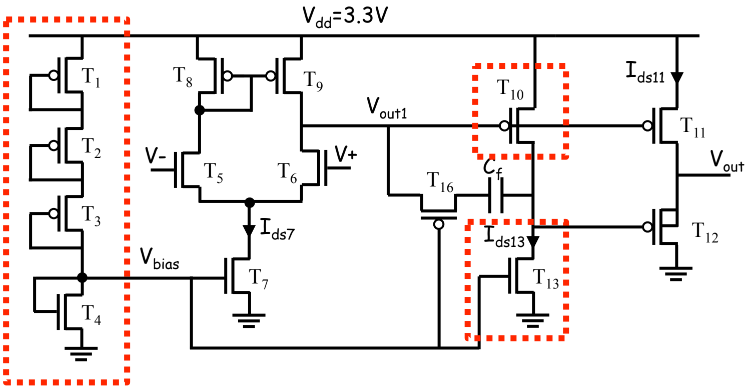

Voltage Reference

Current Source

Common source voltage amplifier

Homework & Lab

- Homework
  - Derive a small-signal model of the circuit to determine the voltage gain
  - Compute the voltage gain
  - Design T_{10} for a voltage gain of 500
- Lab
  - Verify the voltage gain using a 'DC' simulation
  - Verify the voltage gain using a 'AC' simulation

Références

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