Polytech'Montpellier – MEA4
M2 EEA – Systèmes Microélectroniques

Analog IC Design

From transistor biasing to current sources

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http://www.lirmm.fr/~nouet/homepage/lecture_ressources.html


Introduction / Background

- Small-signal parameters of the MOS transistor in the active region (g_m and r_{ds}) are both dependent to the saturation current → MOST biasing is based on a current source
- MOS Transistor is a good current source in the active region
- Basic analog stage (e.g. a common source amplifier) is based on a pair of MOS transistor
  - one used as a voltage to current converter
  - one used as a current source

Pre-requisites / Content

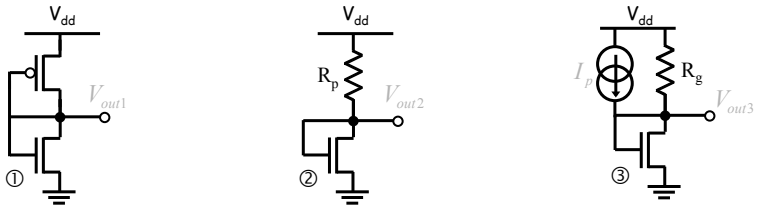
- Pre-requisites
  - Good practice of solving electrical circuits (Node and Mesh laws)
  - Large- and small-signal models for MOST in strong-inversion
- Content
  - How to set-up a constant gate-source voltage for an MOS Transistor? → basic to advanced voltage references
  - Basic current source
  - Increasing output resistance
  - Advanced current sources for V_{dd} stability and large voltage swing

Outline

- Voltage references
  - Elementary self-biasing schemes
  - Some other elementary self-biasing schemes
  - Sensitivity to V_{dd} and T°C variations
  - Advanced voltage references
- Current mirror
  - Elementary current mirror
  - Elementary stages for increased output resistance
  - Other elementary current mirrors
- Elementary current sources
- Overview of advanced current sources
- PMOS current sources

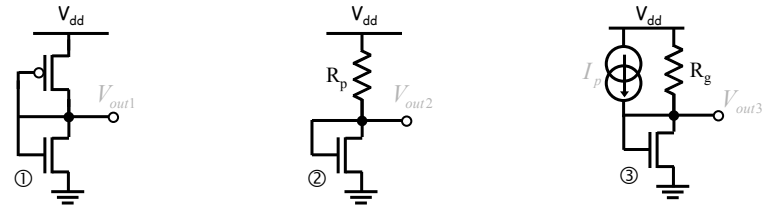
Initial sizing of elementary self-biasing schemes

- Basic statement: a diode-connected MOST is always biased in the active region (if not in the OFF-state)
- 3 basic scheme may allow to control the biasing point of the MOST:
  - one pull-up diode-connected PMOS transistor
  - one pull-up resistor
  - one quasi-ideal current-source



Initial sizing of elementary self-biasing schemes

- Let's design the following circuits to deliver 0.7V under 10μA with V_{dd}=3.3V… The internal resistance of the current source will be R_g=1MΩ.



$$I_{dsn} = I_{dsp} = I_{dsat} = 10\mu A$$

$$V_{effp} = 1.9V; V_{effn} = 0.2V$$

$$\left.\frac{W}{L}\right|_n = \frac{2I_{dsat}}{\mu_n C_{ox}} \frac{1}{V_{effn}^2} = 3.57$$

$$\left.\frac{W}{L}\right|_p = \frac{2I_{dsat}}{\mu_p C_{ox}} \frac{1}{V_{effp}^2} = 0.11$$

$$R_p = \frac{2.6V}{10\mu A} = 260k\Omega$$

$$\left.\frac{W}{L}\right|_n = \frac{2I_{dsat}}{\mu_n C_{ox}} \frac{1}{V_{effn}^2} = 3.57$$

$$I(R_g) = \frac{2.6V}{1M\Omega} = 2.6\mu A$$

$$I_p = 7.4\mu A$$

$$\left.\frac{W}{L}\right|_n = \frac{2I_{dsat}}{\mu_n C_{ox}} \frac{1}{V_{effn}^2} = 3.57$$

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Alternative self-biasing schemes

- Two outputs circuits
- Dual PMOS for output w.r.t V_{dd}
- Silicon surface considerations

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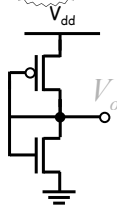
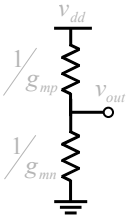
Impact of V_{dd} variations



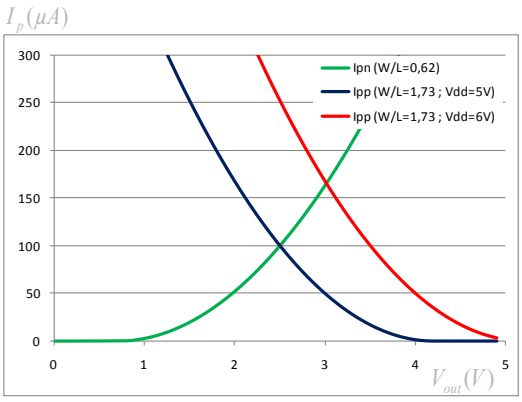
$$I_{pp} = \frac{\mu_p C_{ox}}{2}\frac{W}{L}\left(V_{dd} - V_{out} - |V_{tp}|\right)^2 \qquad I_{pn} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_{out} - V_{tn}\right)^2$$

$$\frac{\partial I_p}{\partial V_{dd}} = ?$$

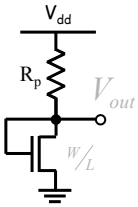


$$\frac{\partial I_p}{\partial V_{dd}} =$$

$$\frac{\partial V_{out}}{\partial V_{dd}} =$$



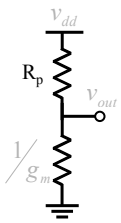
Impact of V_{dd} variations



$$V_{dd} - V_{out} = R_p . I_p \qquad V_{out}; I_p \Rightarrow R_p; V_{eff}; \frac{W}{L}$$

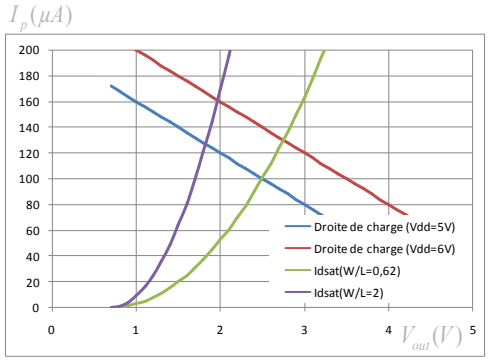
$$I_p = \frac{\mu_n C_{ox}}{2} \frac{W}{L} V_{eff}^2 \qquad I_p = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \left(V_{dd} - R_p I_p - V_t\right)^2$$

$$\frac{\partial I_p}{\partial V_{dd}} = ?$$

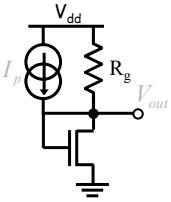


$$\frac{\partial I_p}{\partial V_{dd}} =$$

$$\frac{\partial V_{out}}{\partial V_{dd}} =$$

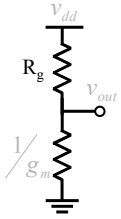


Impact of V_{dd} variations



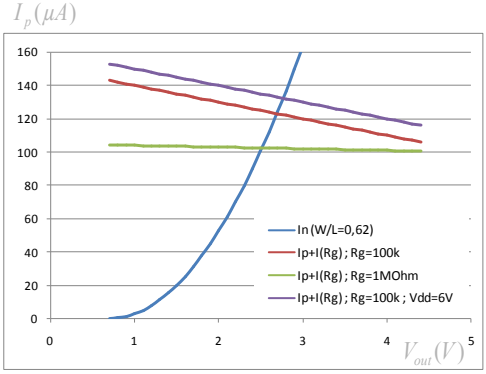
$$I_{ds} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \left(V_{out} - V_t\right)^2 \qquad V_{out}; I_{ds} \Rightarrow \frac{W}{L} \qquad \frac{\partial I_{ds}}{\partial V_{dd}} = ?$$

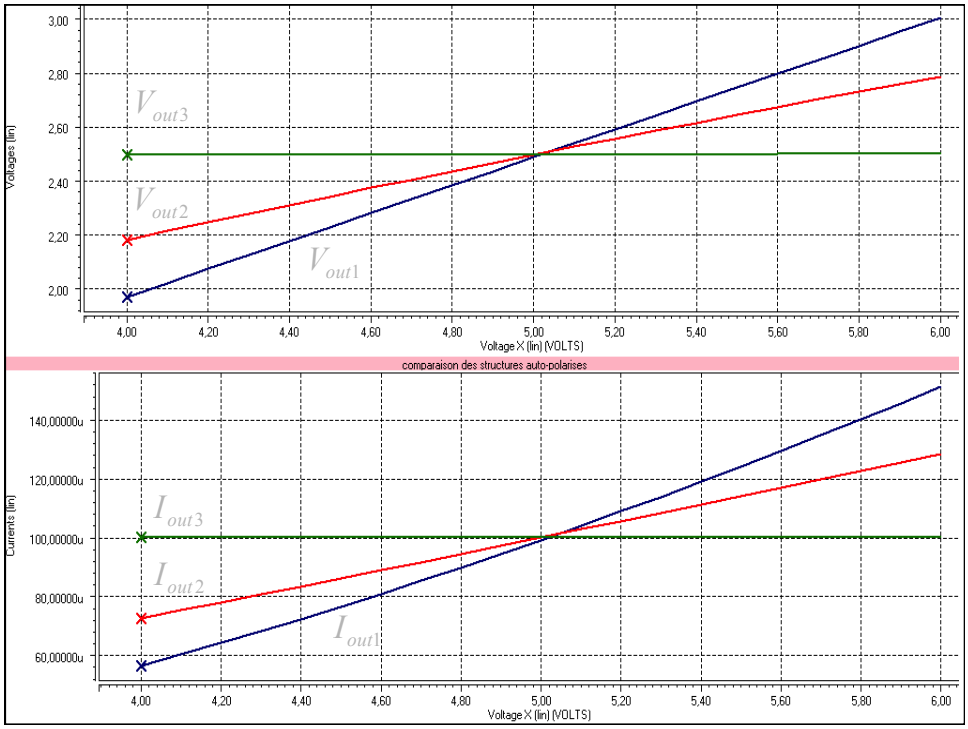
$$I_{ds} = I_p + \frac{V_{dd} - V_{out}}{R_g}$$



$$\frac{\partial I_{ds}}{\partial V_{dd}} =$$

$$\frac{\partial V_{out}}{\partial V_{dd}} =$$





Lab #1: Design of a voltage reference

- Specification: let's design a basic self-biased MOS circuit to deliver two voltages equal respectively to V_{dd}-0.8V and V_{dd}-1.6V. Try to optimize stability for V_{dd} varying +/- 10% around the nominal value (3.3V), power consumption and silicon area…
- Let's calculate the theoretical sensitivity of both output's voltage to V_{dd}…
- Let's verify the previous value by simulation
- Let's simulate the sensitivity to temperature (-25°C up to 85°C)

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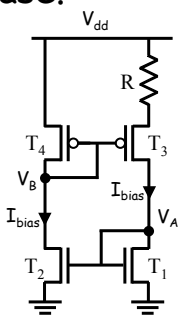
V_{dd}-independent reference voltage

- Principle: a resistor is used to implement a local feedback, when I_{ds} tends to increase under the effect of a V_{dd} increase, the voltage drop in R reduces V_{gs3} and limit the current increase.
- Sizing for a given value of V_A:
  → choice of I_{bias}
  → sizing of T_1 and T_2
  → choice of α
  → sizing of T_3 and T_4 for V_B=V_A
  → calculate R from kirchoff's law:

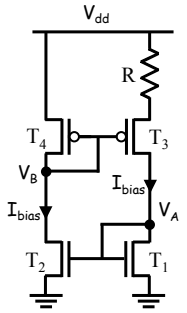
$$V_{gs4} = V_{gs3} + R.I_{bias}$$



$$\frac{W_3}{L_3} = \alpha \cdot \frac{W_4}{L_4}$$

V_{dd}-independent reference voltage

- How it works?
  - I_{bias} is independant of V_{dd}
    → V_A depends only of T_1 size and I_{bias}
- Assumption: $I_{ds1}=I_{ds2}$
  →I_{ds3} and I_{ds4} are then identical
  →$V_{eff4}^2=\alpha.V_{eff3}^2$
- calculate I_{bias} from kirchoff's law:



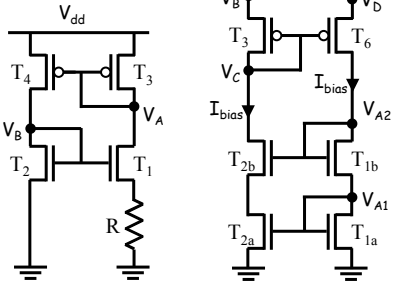
$$\frac{W_3}{L_3}=\alpha\cdot\frac{W_4}{L_4}$$

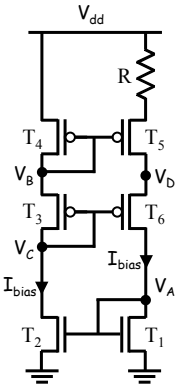
$$V_{eff\,4}-V_{eff\,3}=V_{eff\,4}\left(\frac{\sqrt{\alpha}-1}{\sqrt{\alpha}}\right)=R.I_{bias}$$

$$V_{eff\,4}=\sqrt{\frac{2I_{bias}}{\mu_p C_{ox}}\frac{L_4}{W_4}}\Rightarrow I_{bias}=\frac{2}{\mu_p C_{ox}R^2}\cdot\frac{L_4}{W_4}\cdot\left(\frac{\alpha-1}{\alpha+\sqrt{\alpha}}\right)^2$$

Alternative configurations

- Stability to V_{dd} can be increased by reducing V_{ds}
- Delivering two independant voltages
- Delivering a voltage w.r.t. V_{dd}





$$\frac{W_1}{L_1}=\alpha\cdot\frac{W_2}{L_2}$$

$$\frac{W_5}{L_5}=\alpha\cdot\frac{W_4}{L_4}$$

Lab #2: Design of a voltage reference

- Specification: let's design a V_{dd}-independent reference voltage to deliver the same outputs as in Lab#1 with the same constraints.
- Let's calculate the theoretical sensitivity of both output's voltage to V_{dd}…
- Let's verify the previous values by simulation
- Let's simulate the sensitivity to temperature (-25°C up to 85°C)

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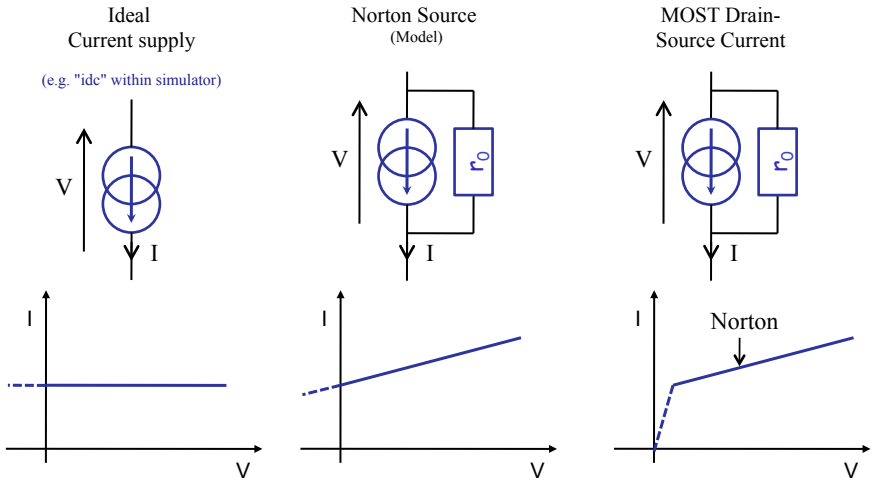
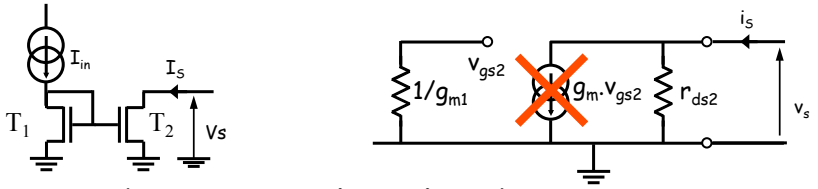
From Norton (Current) Source to MOS transistor

Practical Current Source ≠ Norton source



Current mirroring principle

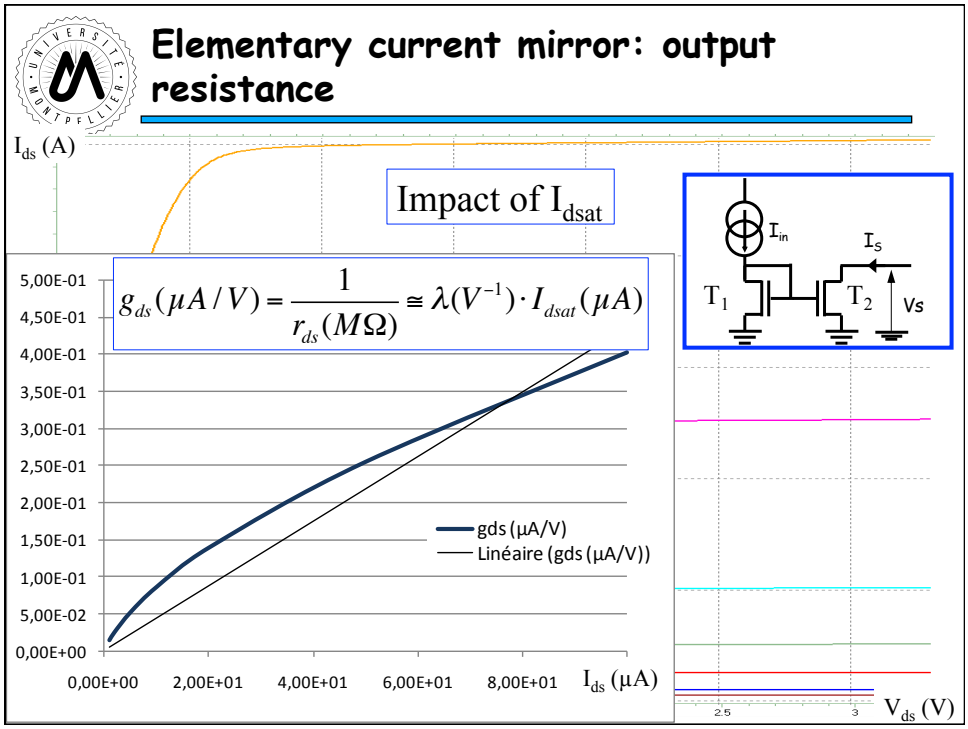


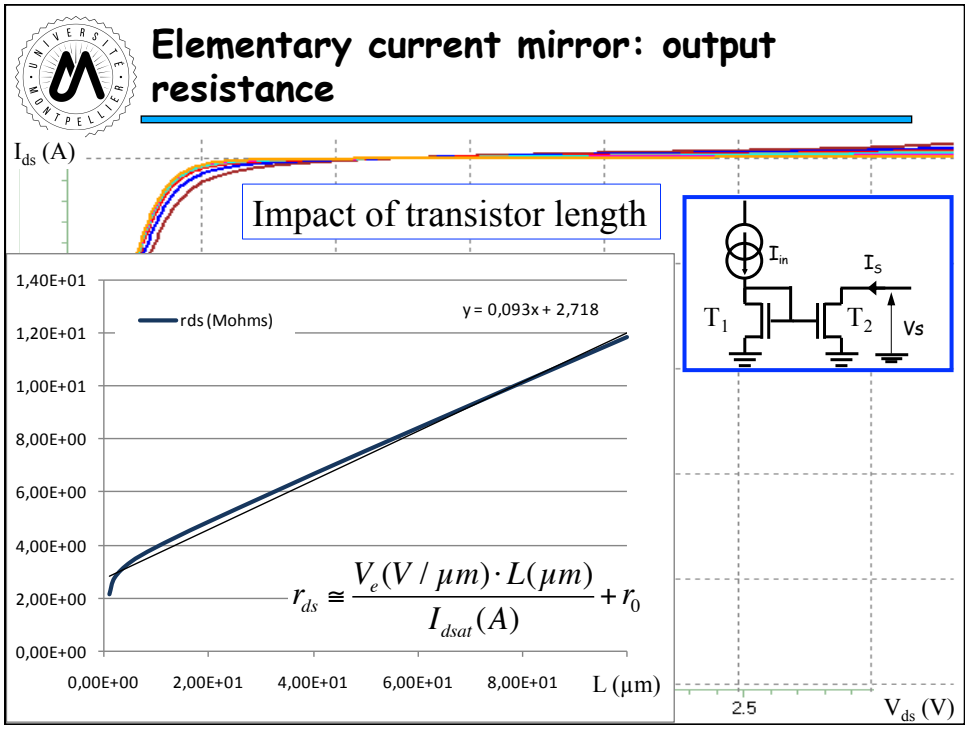
- Biasing (Large Signal Analysis):
  - T_1 is saturated ➔ $I_{in} = I_{ds1} = f(V_{gs1}) = f(V_{eff1})$
  - T_2 must be saturated to deliver a constant current
    - $V_{eff2}=V_{eff1}$ → Output dynamic: $\mathbf{V_{ds} \geq V_{eff}}$

$$I_s = I_{dsat} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}V_{eff}^2 = I_{in}$$

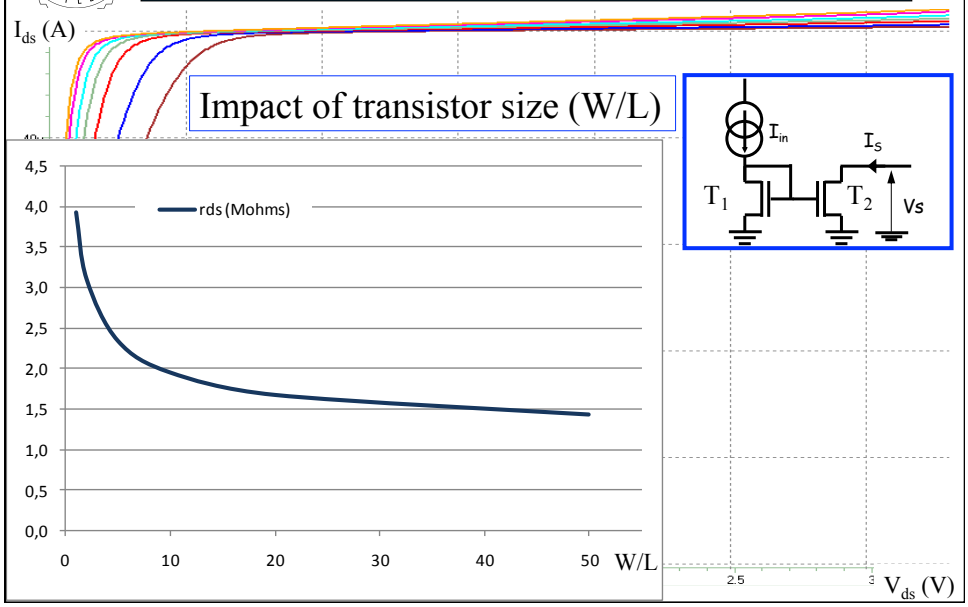
- Small-Signal Analysis
  → Output resistance

$$\frac{v_s}{i_s} = r_{ds2} = \frac{1}{\lambda I_{dsat}}$$


Elementary current mirror: output resistance
Ids (A)
Impact of Idsat
$g_{ds}(\mu A/V) = \frac{1}{r_{ds}(M\Omega)} \cong \lambda(V^{-1}) \cdot I_{dsat}(\mu A)$
5,00E-01
4,50E-01
4,00E-01
3,50E-01
3,00E-01
2,50E-01
2,00E-01
1,50E-01
1,00E-01
5,00E-02
0,00E+00
0,00E+00 2,00E+01 4,00E+01 6,00E+01 8,00E+01 Ids (µA)
gds (µA/V)
Linéaire (gds (µA/V))
Iin
Is
T1
T2
Vs
2.5
3
Vds (V)

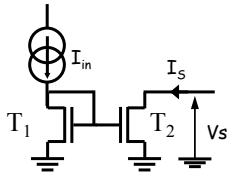

Elementary current mirror: output resistance
Ids (A)
Impact of transistor length
1,40E+01
1,20E+01
1,00E+01
8,00E+00
6,00E+00
4,00E+00
2,00E+00
0,00E+00
rds (Mohms)
y = 0,093x + 2,718
$r_{ds} \cong \frac{V_e(V/\mu m) \cdot L(\mu m)}{I_{dsat}(A)} + r_0$
0,00E+00 2,00E+01 4,00E+01 6,00E+01 8,00E+01 L (µm)
Iin
Is
T1
T2
Vs
2.5
Vds (V)

Elementary current mirror: output resistance



Elementary current mirror: summary

- Impact of I_{dsat}
  - Output resistance is divided by two when current is multiplied by two



- Impact of transistor size
  - Output resistance doubled when transistor length is multiplied by two (constant W/L)
- Useful equations
  - Working with both V_{eff} and length constant

$$\frac{i_s}{v_s} = \frac{1}{r_{ds}} = \frac{\partial I_{ds}}{\partial V_{ds}} \cong \lambda(V^{-1}) \cdot I_{dsat}(A)$$

  - General case → $r_{ds} \propto L$

$$r_{ds} \cong \frac{V_e(V/\mu m) \cdot L(\mu m)}{I_{dsat}(A)} + r_0$$

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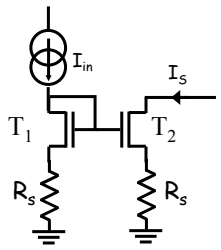
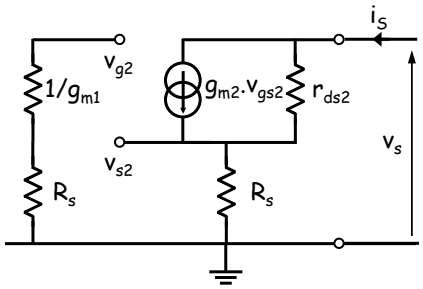
Degenerated source current mirror

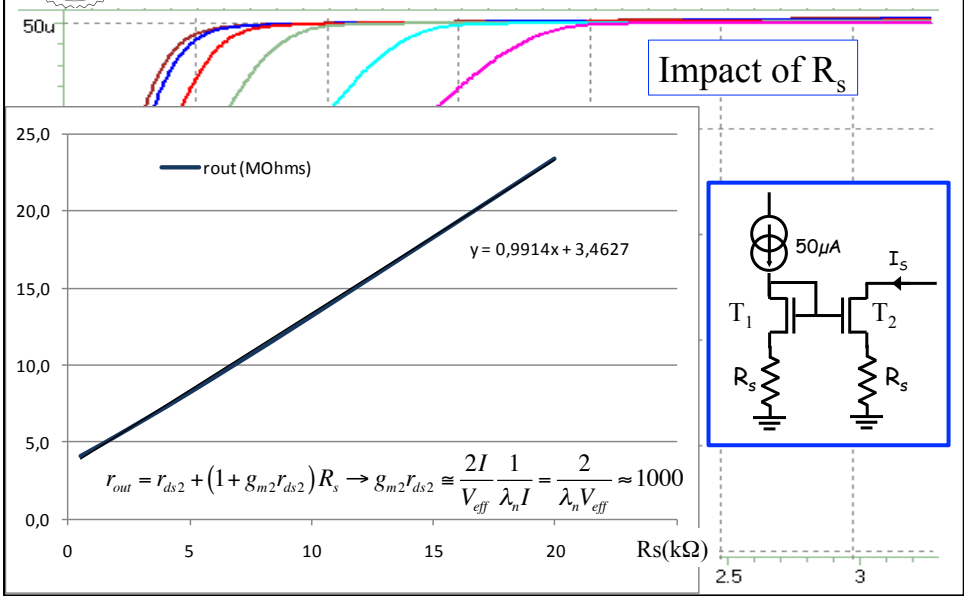




- Large-Signal Analysis
  - T1 always saturated
  - Output dynamic → saturation of T_2
- Small-Signal Analysis
  - Output resistance

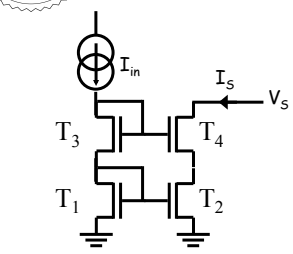
$$I_s = I_{dsat} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}V_{eff}^2 = I_{in}$$

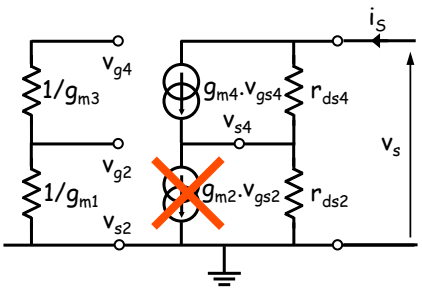
Degenerated source current mirror



$$r_{out} = r_{ds2} + (1 + g_{m2} r_{ds2}) R_s \rightarrow g_{m2} r_{ds2} \cong \frac{2I}{V_{eff}} \frac{1}{\lambda_n I} = \frac{2}{\lambda_n V_{eff}} \approx 1000$$

Cascode current mirror



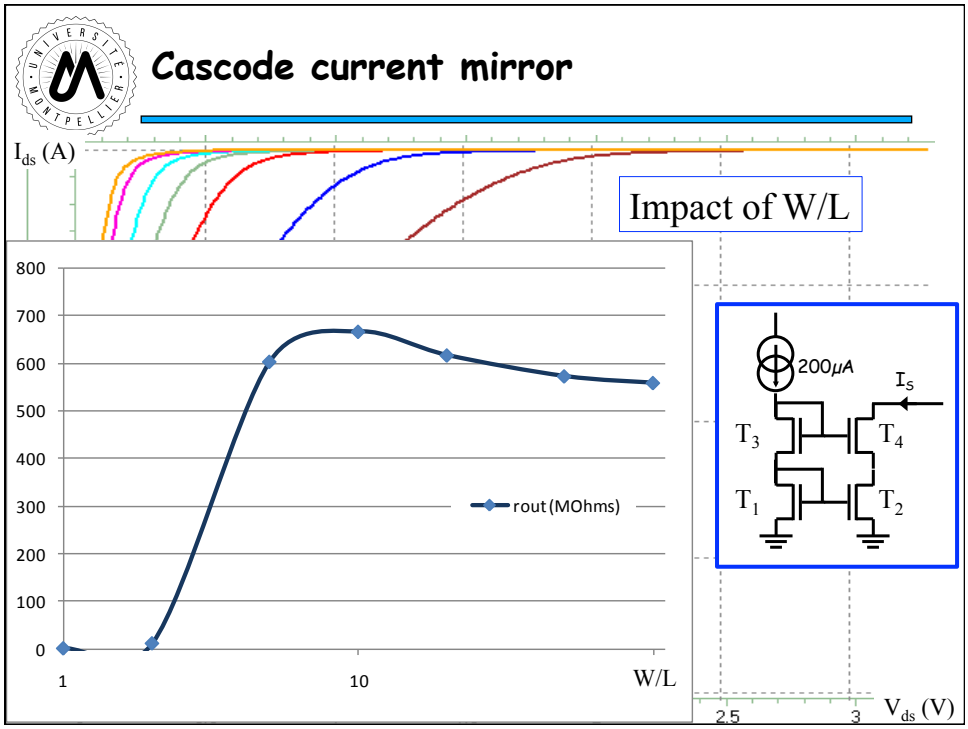


$$I_{d1} = I_{d2} = I_{d3} = I_{d4} = I_{in}$$

- Large-Signal Analysis
  - T1 and T_3 are saturated, T2 also
  - Output dynamic → saturation of T_4
- Small-Signal Analysis
  - Output resistance

$$I_s = I_{dsat} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} V_{eff}^2 = I_{in}$$

Cascode current mirror



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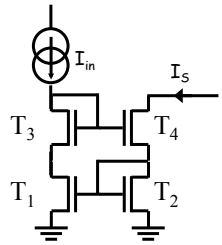
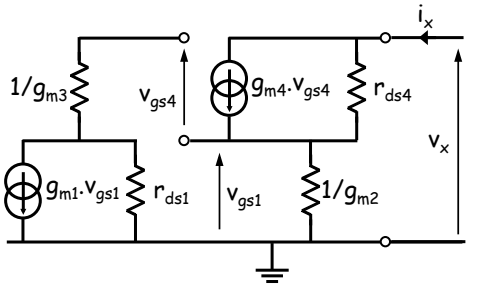
Wilson current mirror





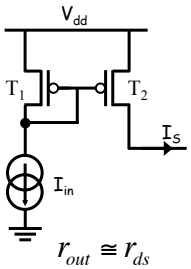
$$I_{d1} = I_{d2} = I_{d3} = I_{d4} = I_{in}$$

- Similar performance to cascode mirror

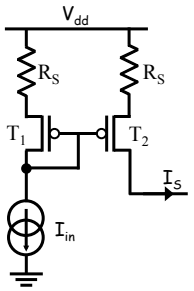
$$I_s = I_{dsat} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}V_{eff}^2 = I_{in} \qquad V_S > V_{tn} + 2\cdot V_{eff} \qquad \frac{v_S}{i_s} \cong g_{m4} r_{ds1} r_{ds4}$$

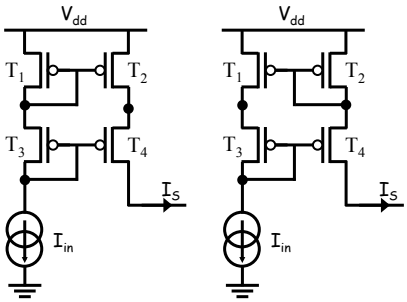
PMOS Current Mirrors

- Every NMOS current mirror has a PMOS dual
- Caracteristics are identical and easy to transpose: $V_{smin} \rightarrow V_{smax}$, r_{out}



$$r_{out} \cong r_{ds}$$

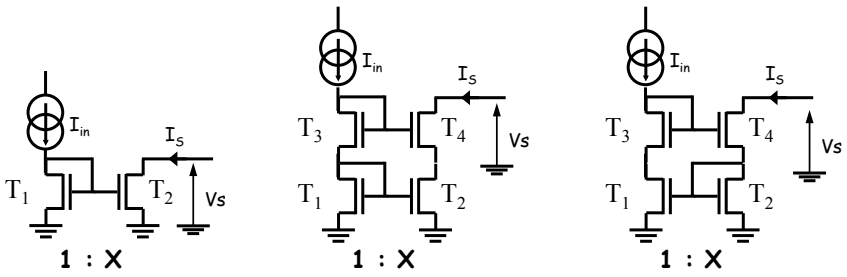




$$r_{out} \cong g_m r_{ds} r_{ds}$$

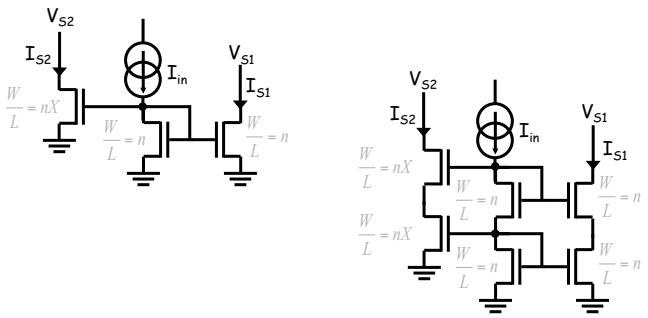
Non-symetrical mirrors

- Different ratio W/L may be used in the output branch (generally X>1 → output current higher than reference current)
- Same V_{eff} for all transistors means current proportionnal to W/L:

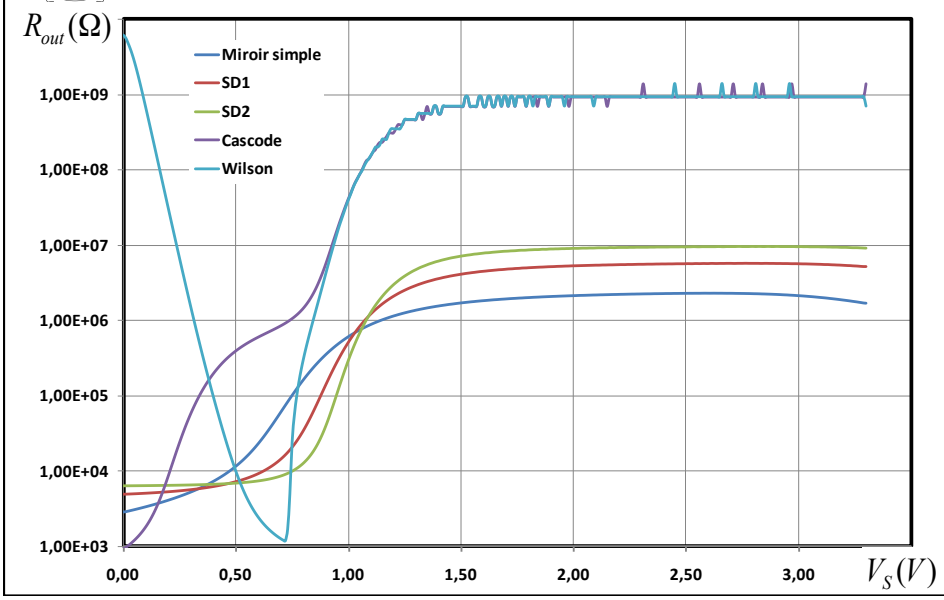


Multiple outputs current mirrors

- One reference branch may be connected to as many output branches as recessary for the application
- Each output may deliver a different ratio of current
- Each output may have a different output resistance



Overview of output resistance of elementary current mirors



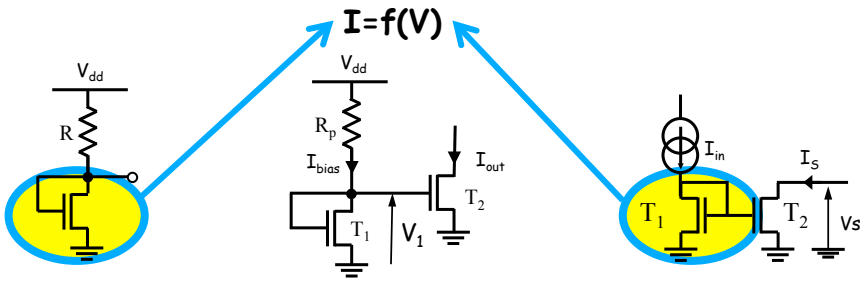
Outline

- Voltage references
  - Elementary self-biasing schemes
  - Some other elementary self-biasing schemes
  - Sensitivity to V_{dd} and T°C variations
  - Advanced voltage references
- Current mirror
  - Elementary current mirror
  - Elementary stages for increased output resistance
  - Other elementary current mirrors
- Elementary current sources
- Overview of advanced current sources
- PMOS current sources

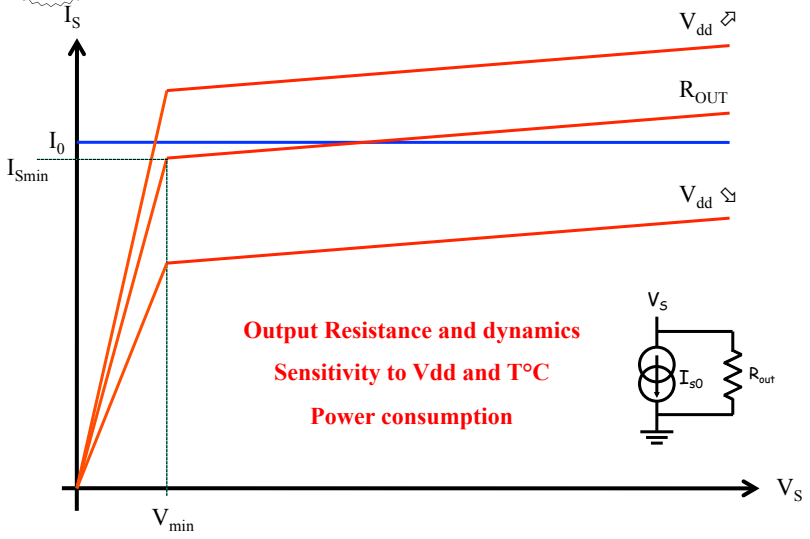
From current mirrors towards current sources

- Analog Integrated Circuits are based on elementary stages
  - Voltage references
  - Current mirrors
  - **Current sources**
  - Amplifier stages

Current flowing through ground or from V_{dd}

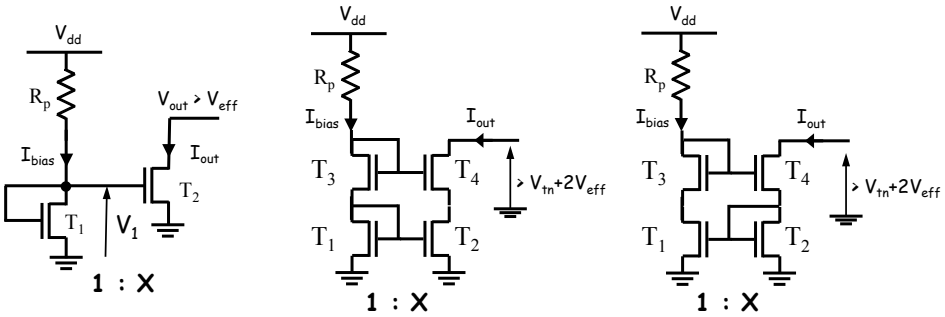


Ideal versus actual current sources



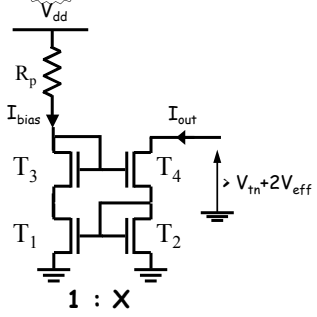
Resistance biasing

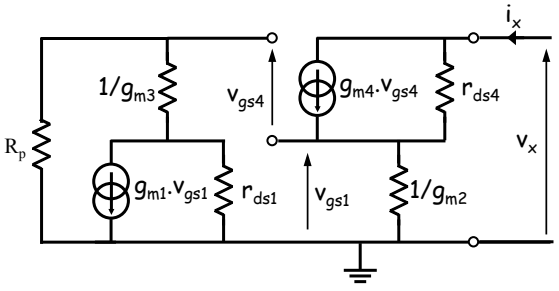
- NMOS current sources



- Sizing
  - Output dynamics → V_{eff}
  - Output current (I_{out}) → W/L of T_2 (T_4)
  - X → Reference current (I_{in}) → W/L of T_1 (T_3), R_p

Output resistance calculation
(e.g. Wilson Current Source)





$$i(R_p) = \frac{r_{ds1}}{R_p + r_{ds1} + \frac{1}{g_{m3}}} g_{m1} v_{gs1}$$

$$v_{g4} = -R_p \cdot i(R_p) = \frac{-g_{m1} r_{ds1} R_p}{R_p + r_{ds1} + \frac{1}{g_{m3}}} v_{gs1} = -A v_{gs1}$$

$$v_{gs4} = -(1+A) v_{gs1} = -(1+A)\frac{i_x}{g_{m2}} \cong -(1 + g_{m1} R_p)\frac{i_x}{g_{m2}}$$

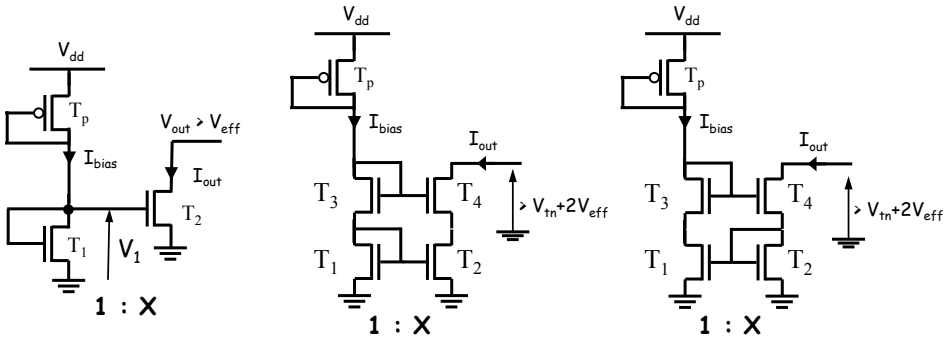
$$v_x = \frac{i_x}{g_{m2}} + r_{ds4}\left(i_x - g_{m4} v_{gs4}\right)$$

$$v_x = \left(\frac{1}{g_{m2}} + r_{ds4} + (1+A)\frac{g_{m4}}{g_{m2}} r_{ds4}\right) i_x$$

$$r_{out} = \frac{1}{g_{m2}} + (2+A) \cdot r_{ds} \cong (2 + g_{m1} R_p) \cdot r_{ds}$$

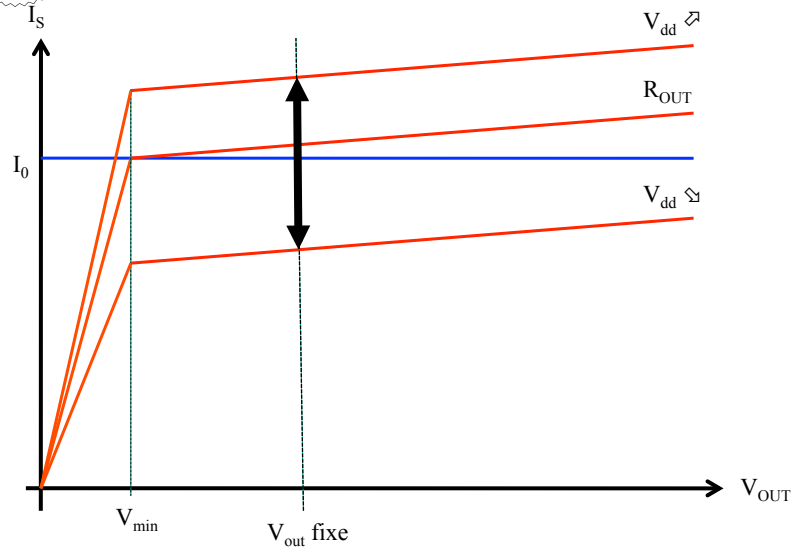
Transistor biasing

- NMOS Current Sources

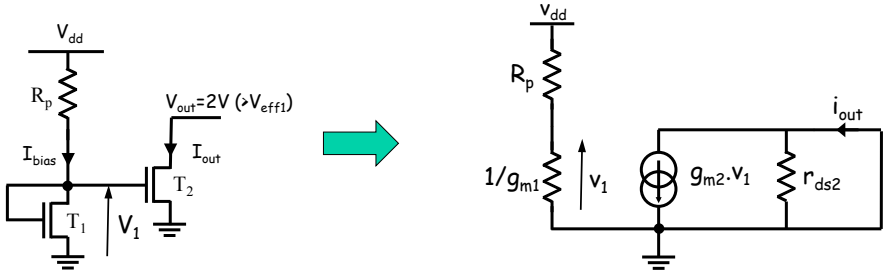


- Output dynamics → V_{eff}
- Output current (I_{out}) → W/L of T_2 (T_4)
- X → Reference current (I_{in}) → W/L of T_1 (T_3), T_p

Impact of V_{dd}



Resistance biasing



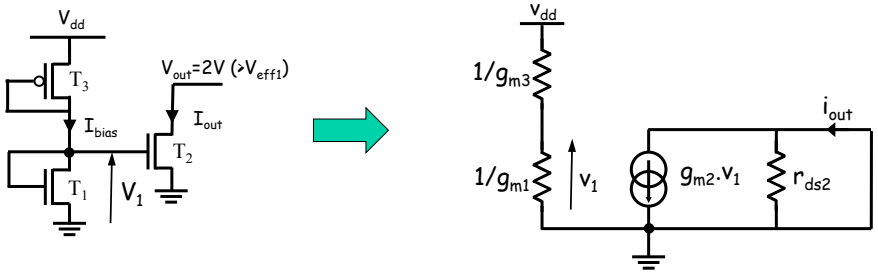
$$V_1 = V_{eff1} + V_{tn}$$

$$I_{bias} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} \cdot V_{eff1}^2$$

$$R_p = \frac{V_{dd} - V_1}{I_{bias}}$$

$$I_{bias} = I_{out}(T_1 = T_2)$$

Transistor biasing

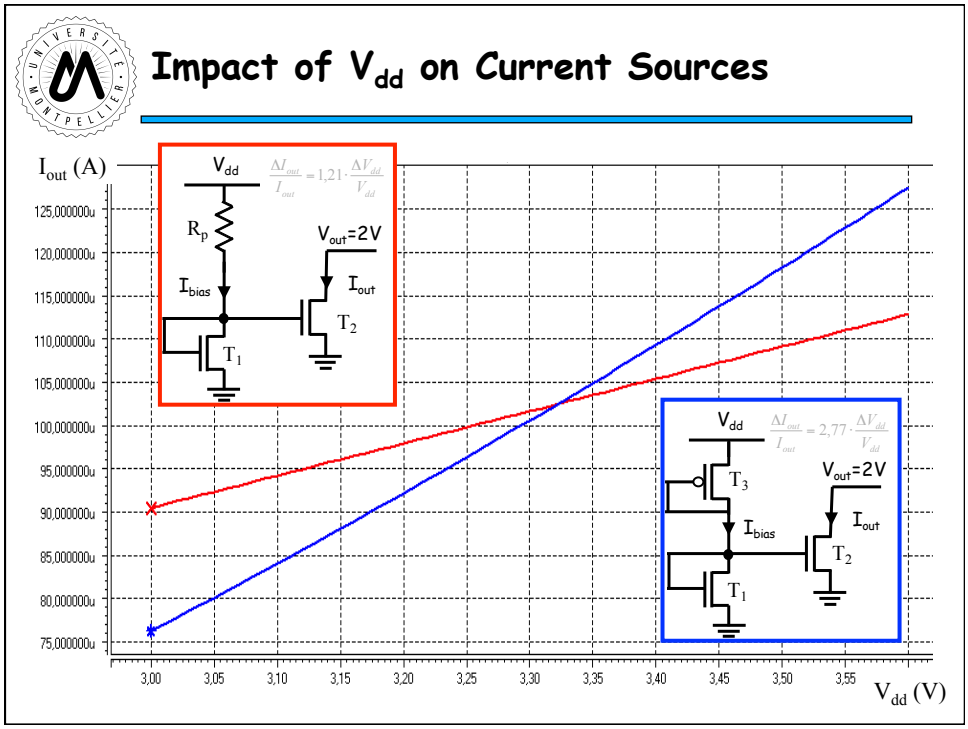


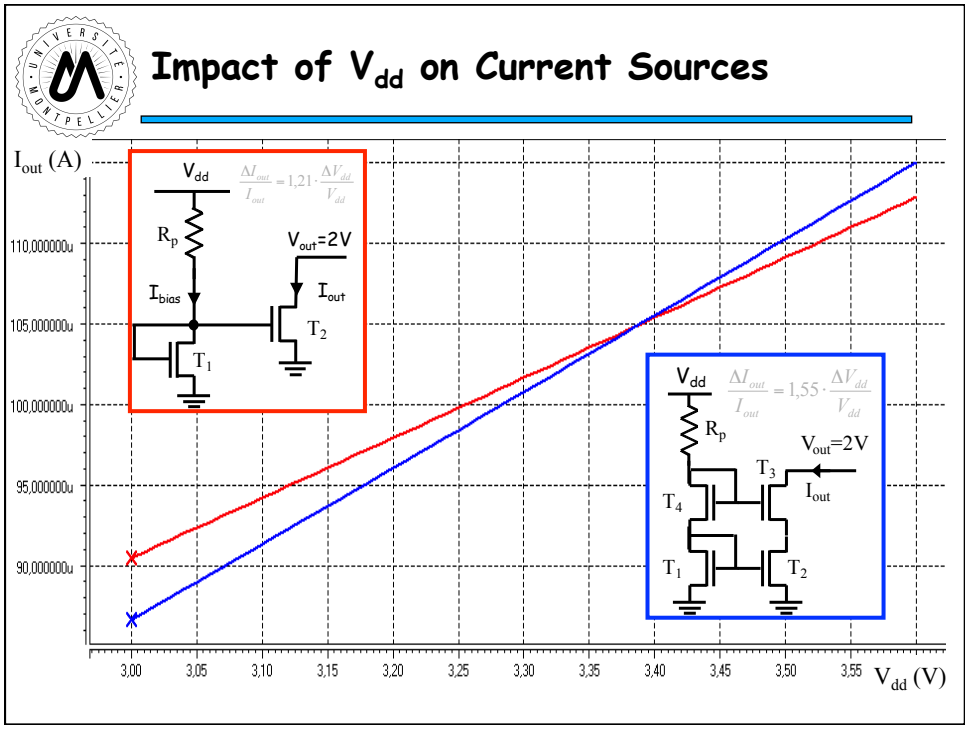
$$V_1 = V_{eff1} + V_{tn}$$

$$I_{bias} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W_1}{L_1} \cdot V_{eff1}^2$$

$$I_{bias} = \frac{\mu_p C_{ox}}{2} \cdot \frac{W_3}{L_3} \cdot \left(V_{dd} - V_1 - |V_{tp}|\right)^2$$

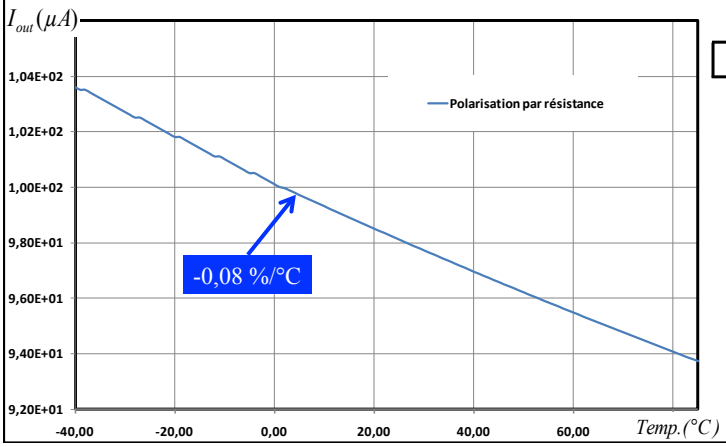
$$I_{bias} = I_{out}(T_1 = T_2)$$

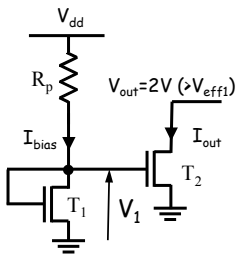

Impact of V_{dd} on Current Sources
I_{out} (A)
125,000000u
120,000000u
115,000000u
110,000000u
105,000000u
100,000000u
95,000000u
90,000000u
85,000000u
80,000000u
75,000000u
3,00
3,05
3,10
3,15
3,20
3,25
3,30
3,35
3,40
3,45
3,50
3,55
V_{dd} (V)
V_{dd}
$\frac{\Delta I_{out}}{I_{out}} = 1,21 \cdot \frac{\Delta V_{dd}}{V_{dd}}$
R_p
V_{out}=2V
I_{bias}
I_{out}
T_1
T_2
$\frac{\Delta I_{out}}{I_{out}} = 2,77 \cdot \frac{\Delta V_{dd}}{V_{dd}}$
T_3


Impact of V_{dd} on Current Sources
I_{out} (A)
110,000000u
105,000000u
100,000000u
95,000000u
90,000000u
3,00
3,05
3,10
3,15
3,20
3,25
3,30
3,35
3,40
3,45
3,50
3,55
V_{dd} (V)
V_{dd}
$\frac{\Delta I_{out}}{I_{out}} = 1,21 \cdot \frac{\Delta V_{dd}}{V_{dd}}$
R_p
V_{out}=2V
I_{bias}
I_{out}
T_1
T_2
$\frac{\Delta I_{out}}{I_{out}} = 1,55 \cdot \frac{\Delta V_{dd}}{V_{dd}}$
T_3
T_4

Resistance biasing and temperature

- An increase in temperature reduces the saturation current of a transistor

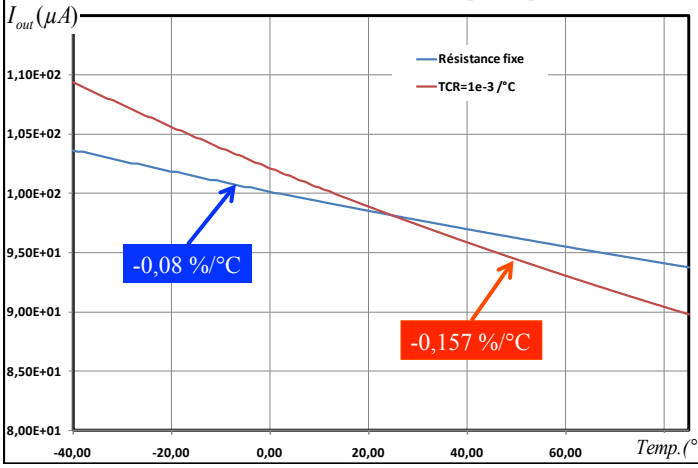


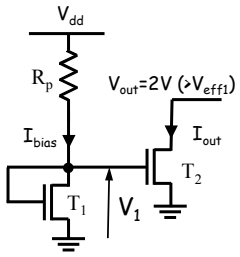


Resistance biasing and temperature

- Resistance may also change with temperature

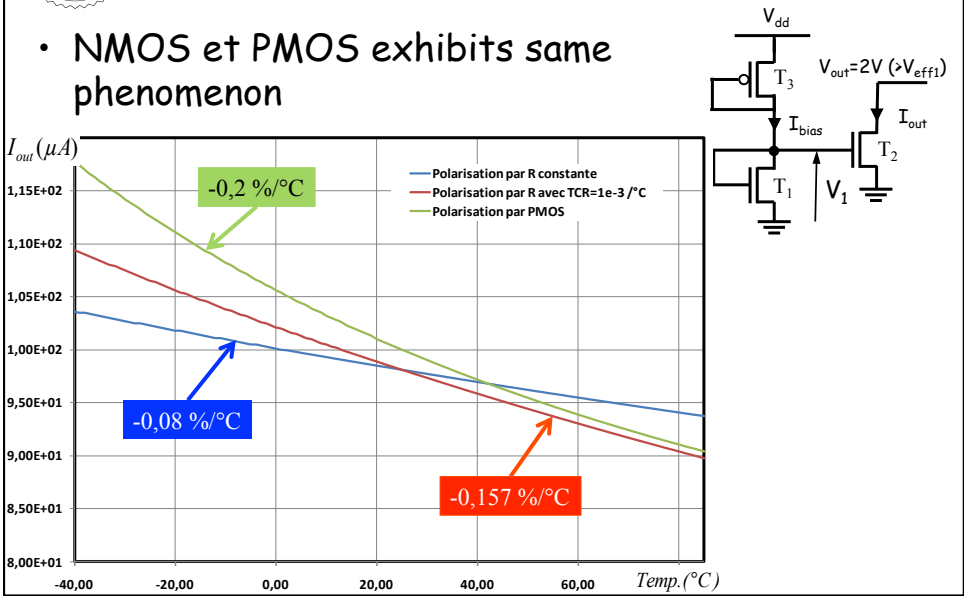
$$R_p = R_{p0}(1 + TCR.T)$$





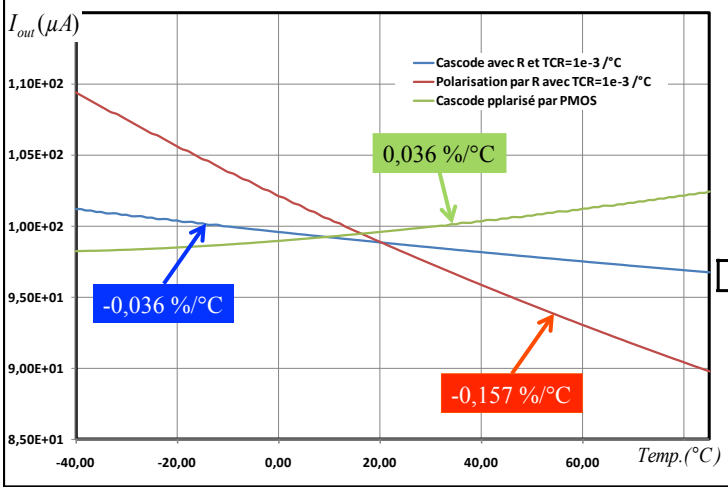
Transistor biasing and temperature

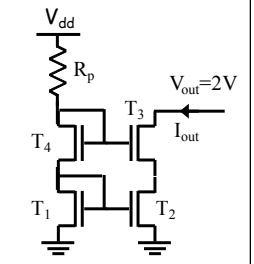
- NMOS et PMOS exhibits same phenomenon

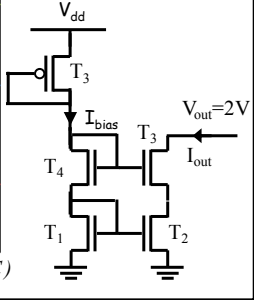


Cascode Source and temperature

- Feedback may improve results







Outline

- Voltage references
  - Elementary self-biasing schemes
  - Some other elementary self-biasing schemes
  - Sensitivity to V_{dd} and T°C variations
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  - Elementary current mirror
  - Elementary stages for increased output resistance
  - Other elementary current mirrors
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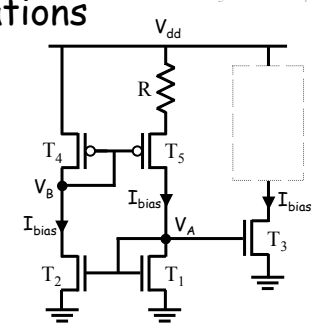
V_{dd}-independent current sources

- Principle: a resistor implement a feedback that tends to reduce current variations
- Sizing methods
  - Choice of I_{bias} and α (generally, 4, 9 or 16)

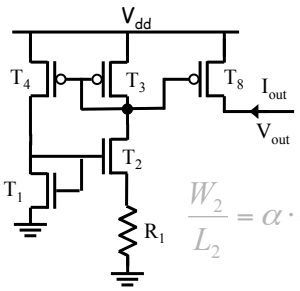
$$\frac{W_5}{L_5} = \alpha \cdot \frac{W_4}{L_4}$$

- I_{bias} is not sensitive to V_{dd} variations
  - Assuming identical currents in T_1 and T_2 leads to an expression of I_{bias} depending of T_4, T_5 et R



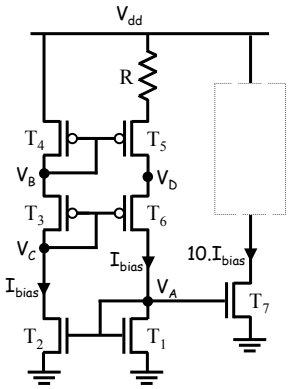
V_{dd}-independent current sources

- Other configurations
  - Dual circuit in PMOS (current from V_{dd})
  - Increased stability by reduction of V_{ds2} and V_{ds5}
  - Power consumption
    → asymmetrical current mirror



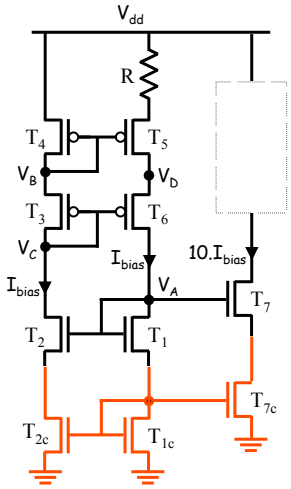
$$\frac{W_2}{L_2} = \alpha \cdot \frac{W_1}{L_1}$$

$$\frac{W_5}{L_5} = \alpha \cdot \frac{W_4}{L_4}$$



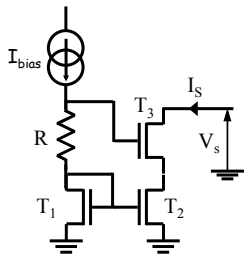
V_{dd}- independent and increased output resistance

- V_{dd}-independent
  → R, T_4 and T_5 to set value of I_{bias} independently of V_{dd}
- Reduced power consumption
  → asymmetrical current mirror
- High-voltage operation
  → T_3 and T_6 are optional
- Increased R_{out}
  → Cascode output
  → Problem → output range of operation



Increasing output dynamic range

- Principle

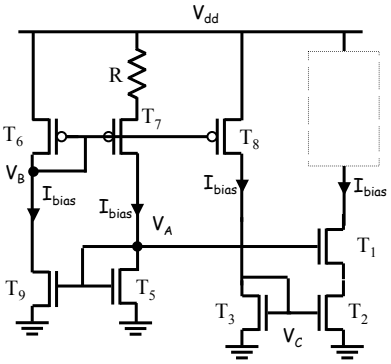


$$V_{eff} = V_{gs} - V_{tn}$$
$$V_{ds1} = V_{gs1} = V_{eff} + V_{tn}$$
$$V_{gs3} = V_{ds1} + R.I_{bias} - V_{s3} = V_{eff} + V_{tn}$$
$$\Rightarrow V_{ds2} = V_{s3} = R.I_{bias} \geq V_{eff}$$
$$\Rightarrow V_{d3} \geq 2.V_{eff}$$

Trade-off between output range of operation and output resistance…

Increasing output dynamic range

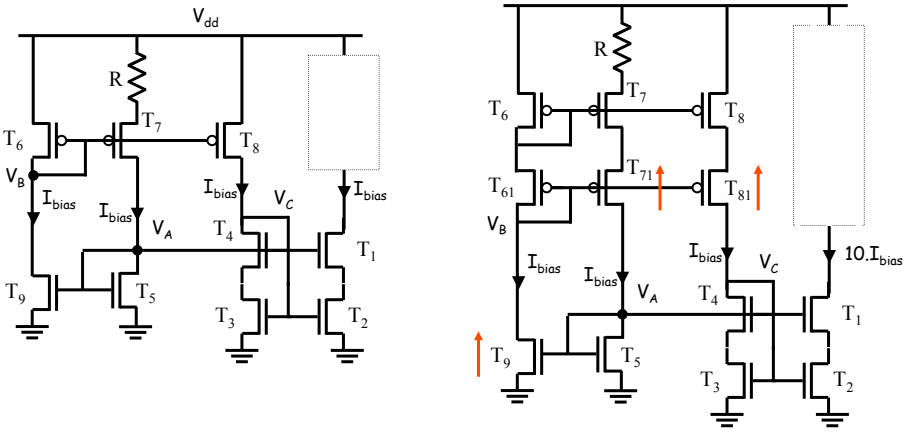
- Implementation: large-swing cascode current source with V_{dd}-independent reference current



$$\frac{W_7}{L_7} = \alpha \cdot \frac{W_6}{L_6} (\alpha > 1)$$
$$V_{eff\,6} = V_{eff\,7} + V_R \text{ avec } V_R = R \cdot I_{bias}$$
$$V_{eff\,6} = \sqrt{\alpha} \cdot V_{eff\,7}$$

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W_3}{L_3} = 4 \cdot \frac{W_5}{L_5} = 4 \cdot \frac{W_9}{L_9}$$

Increasing output dynamic range: alternative configurations



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Current sources

- Overview of main characteristics

	Impact of V_{dd}	Output resistance	Output range of operation
Basic current source	±25%	625kΩ	> 0,8V
V_{dd}-independent current source	±2,3%	500kΩ	> 0,9V
V_{dd}-independent current source with cascoded output	±0,02%	80MΩ	> 1V
Large-swing V_{dd}-independent cascoded current source	±9% ±2,25%	3,54MΩ 4,88MΩ	> 0,3V > 0,3V

Références

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- P. Allen and D. Holberg, "CMOS Analog Circuit Design", 2nd Edition, 2002,Oxford University Press, ISBN 0-19-511644-5
- B. Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2001, ISBN 0-07-238032-2
- P. Gray, P. Hurst, S. Lewis,and R.G. Meyer, "Analysis and Design of Analog Integrated Circuits", 4th Edition, John Wiley and Sons, 2001, ISBN 0-471-32168-0