Polytech'Montpellier – MEA4
M2 EEA – Systèmes Microélectroniques

Analog IC Design

One- and two-transistors Amplifiers

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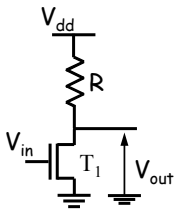
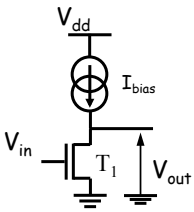
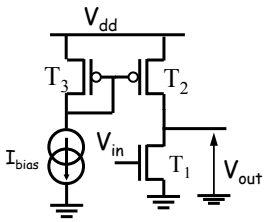
http://www.lirmm.fr/~nouet/homepage/lecture_ressources.html

Introduction

- Analog Integrated Circuits are based on elementary stages
  - Voltage references
  - Current mirrors
  - Current sources
  - **Amplifier stages**





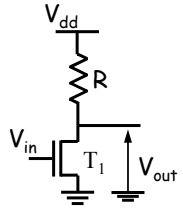


Outline

- Elementary amplifiers
  - Common source amplifier
    - Biasing with a resistor
    - Biasing with an ideal current source
    - Biasing with a current miror
  - Common gate amplifier
  - Common drain or source follower
  - Overview of Basic CMOS Amplifiers
- Common mode issues
  - Differential pair and differential amplifier
  - Differential output amplifier
- Homework & Labs

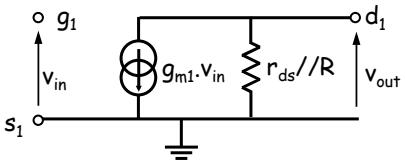
Common Source amplifier

- Resistance biasing: dimensionnement & plage de fonctionnement
  - $V_{out} > V_{eff}$
  - $V_{in}(dc) \rightarrow V_{eff1} \rightarrow W/L\ (I_{bias})$
  - $R \rightarrow V_{out} \# V_{dd}/2$

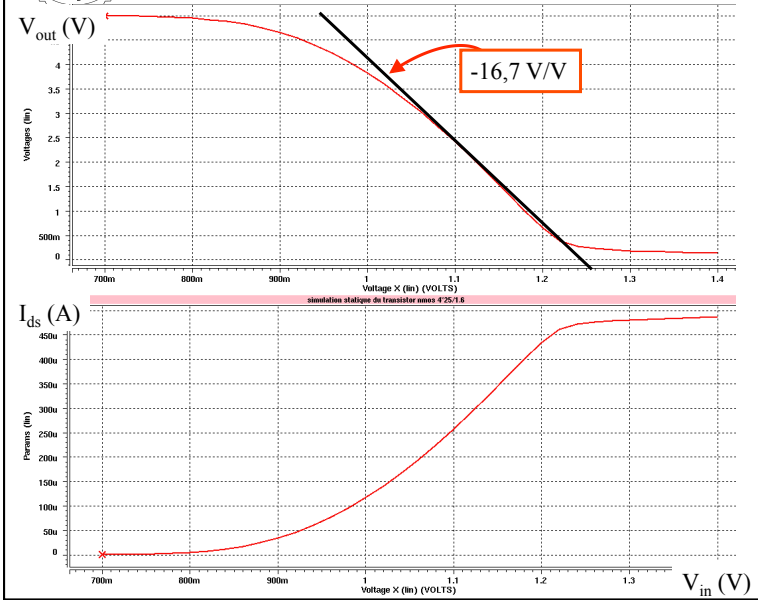


$$V_{in} = V_{dc} + v_{in} \cong V_{eff} + V_{tn}$$

- Small-Signal Model
  - Voltage Gain, input and output resistance

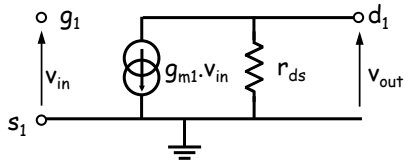


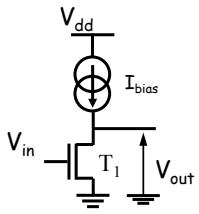
R-biased Common Source amplifier



Common Source amplifier

- Biasing with an ideal current source

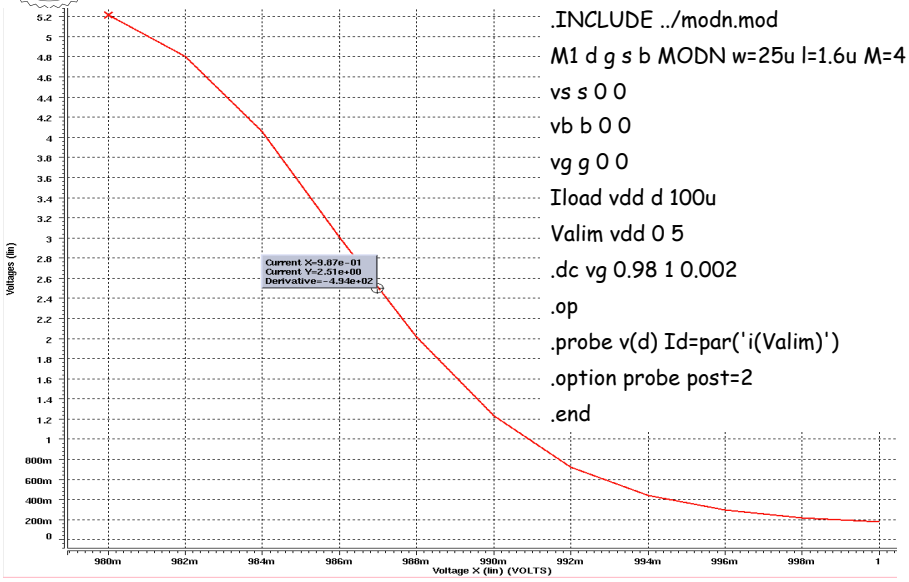




- Biasing point
  - $V_{in} > V_{tn}$; $V_{in}-V_{tn} = V_{eff} < V_{out}$; $V_{out} \# V_{dd}/2$
  - → W/L
- Small-Signal Model
  - Voltage Gain, input and output resistance

Impact of a resistive load ?

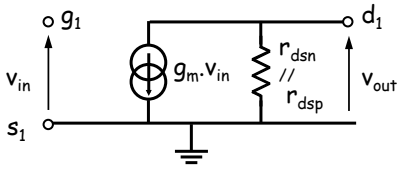
I-biased Common Source amplifier

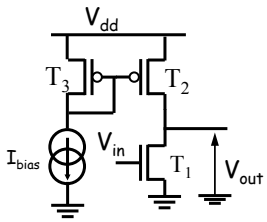



```
.INCLUDE ../modn.mod
M1 d g s b MODN w=25u l=1.6u M=4
vs s 0 0
vb b 0 0
vg g 0 0
Iload vdd d 100u
Valim vdd 0 5
.dc vg 0.98 1 0.002
.op
.probe v(d) Id=par('i(Valim)')
.option probe post=2
.end
```

Common Source amplifier

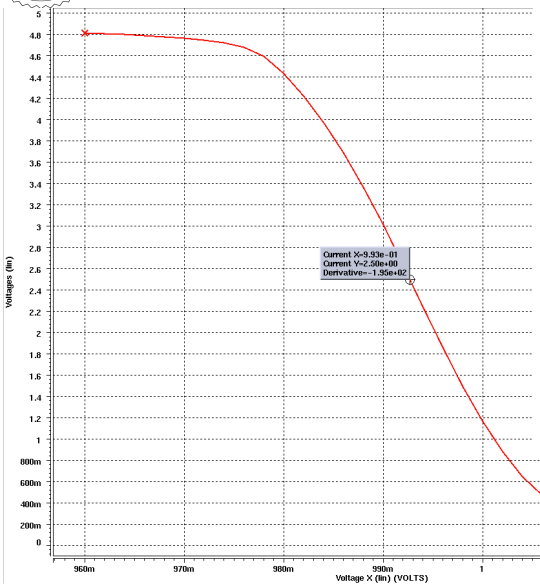
- Biasing by current mirror





- Biasing point
  - $V_{in} > V_{tn}$; $V_{in}-V_{tn} = V_{eff} < V_{out}$; $V_{out} \# V_{dd}/2$
  - → W/L
- Small-Signal Model
  - Voltage Gain, input and output resistance

T-biased Common Source amplifier




```
.INCLUDE ../modn.mod
.Include ../modp.mod
M1 d g s b MODN w=25u l=1.6u M=4
M2 d g1 vdd vdd MODP w=25u l=1.6u M=4
M3 g1 g1 vdd vdd MODP w=25u l=1.6u M=4
vs s 0 0
vb b 0 0
vg g 0 0
Ibias g1 0 100u
Valim vdd 0 5
.dc vg 0.96 1.02 0.002
.probe v(d) Id=par('i(Valim)')
.option probe post=2
.end
```

Impact of a capacitive load ?

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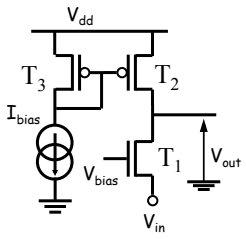
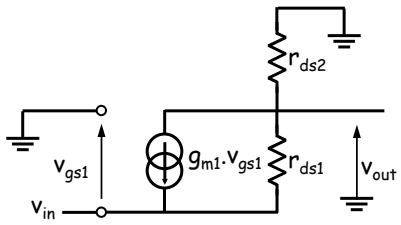
Common gate amplifier



All transistors are saturated



$$v_{gs1} = -v_{in}$$

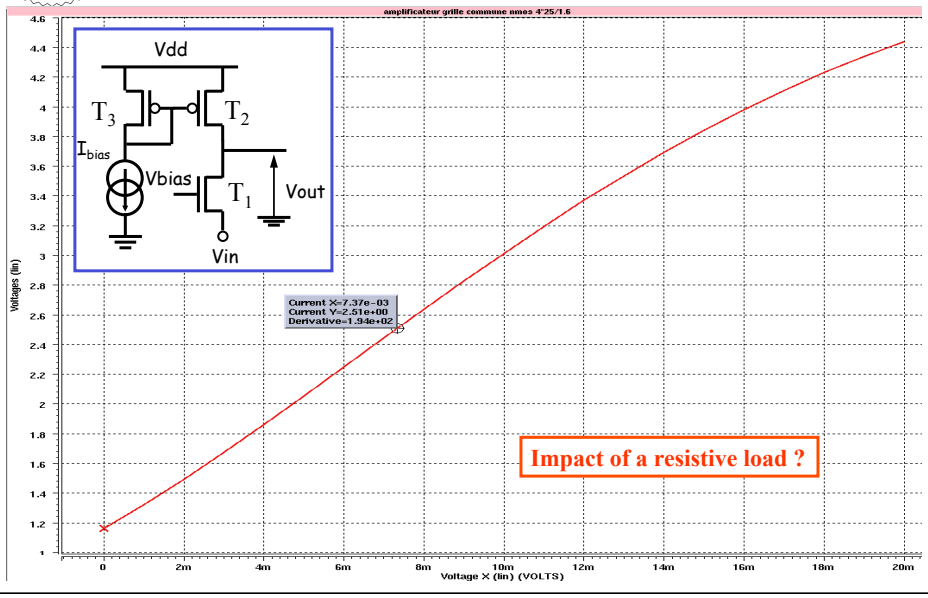
$$g_{ds2} \cdot v_{out} + g_{ds1} \cdot (v_{out} - v_{in}) - g_{m1} \cdot v_{in} = 0$$

$$(g_{ds1} + g_{ds2}) \cdot v_{out} = (g_{ds1} + g_{m1}) \cdot v_{in} \qquad A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m1} + g_{ds1}}{g_{ds1} + g_{ds2}}$$

Input resistance ?

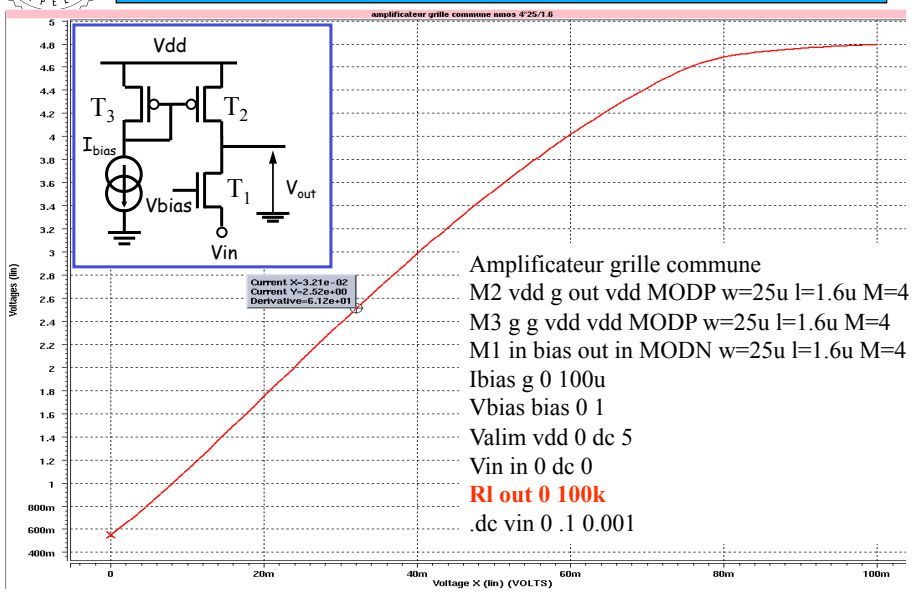
$$r_{in} = \frac{r_{ds2}}{A_v} \cong \frac{2}{g_{m1}}$$

Common gate amplifier



Impact of a resistive load ?

Common gate amplifier




```
Amplificateur grille commune
M2 vdd g out vdd MODP w=25u l=1.6u M=4
M3 g g vdd vdd MODP w=25u l=1.6u M=4
M1 in bias out in MODN w=25u l=1.6u M=4
Ibias g 0 100u
Vbias bias 0 1
Valim vdd 0 dc 5
Vin in 0 dc 0
Rl out 0 100k
.dc vin 0 .1 0.001
```

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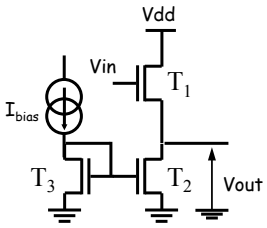
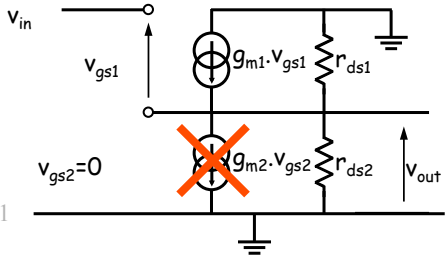
Source follower (Common drain)



All transistors are saturated



$$v_{gs1} = v_{in} - v_{out}$$

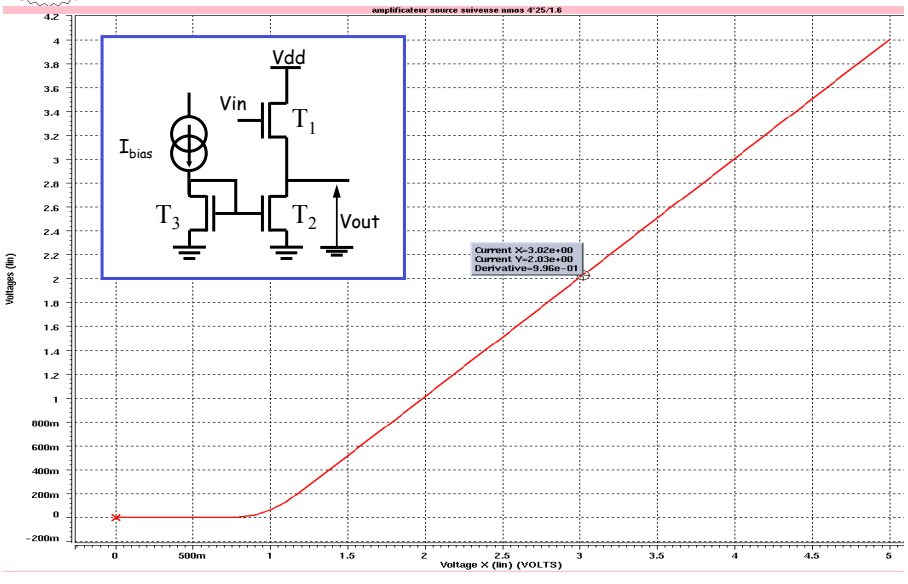
$$v_{out} = \left(r_{ds1} // r_{ds2}\right) \times g_{m1} \cdot v_{gs1}$$

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{ds1} + g_{ds2} + g_{m1}} \cong 1$$

$$r_{out} = \frac{1}{g_{ds1} + g_{ds2} + g_{m1}} \cong \frac{1}{g_{m1}}$$

Output resistance?

Source follower (Common drain)



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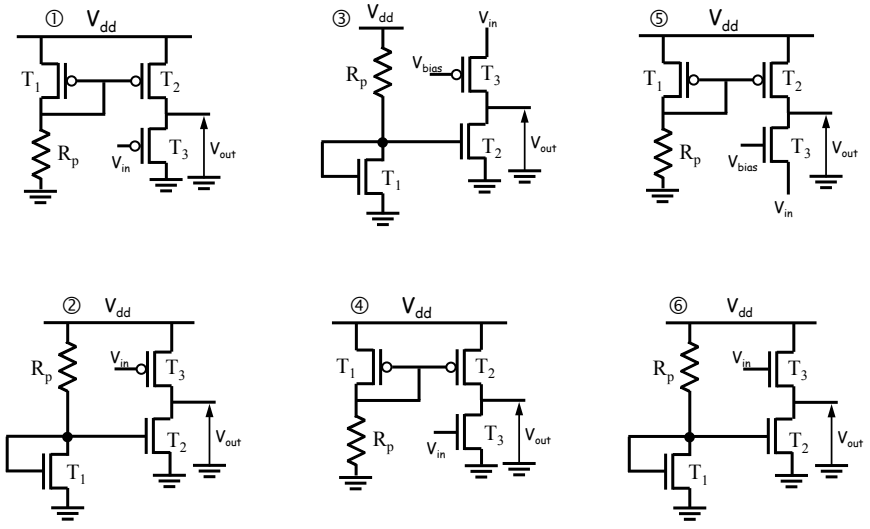
Overview of Basic CMOS Amplifiers



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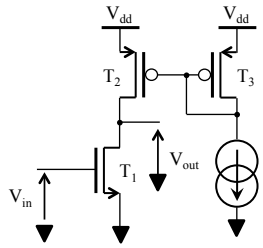
Common Source Amplifier Limitations

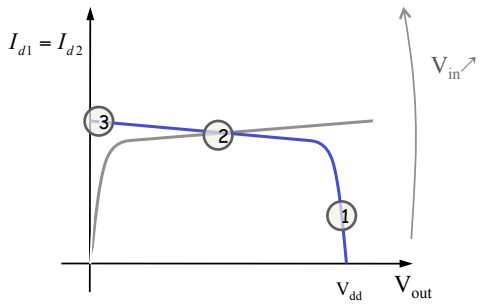
Current Mirror Biasing



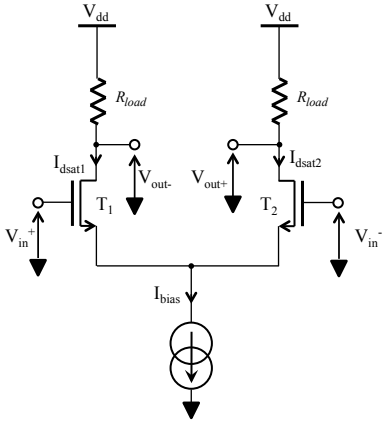
$$A_V = -g_{m1}\left(r_{ds1} // r_{ds2}\right) = \frac{-g_{m1}}{\left(g_{ds1} + g_{ds2}\right)}$$

$r_{in} = \infty$ $r_{out} = r_{ds1} // r_{ds2}$

- Biasing
  - $V_{in}=V_{eff}+V_{tn}$



Differential Input Stage: Principle

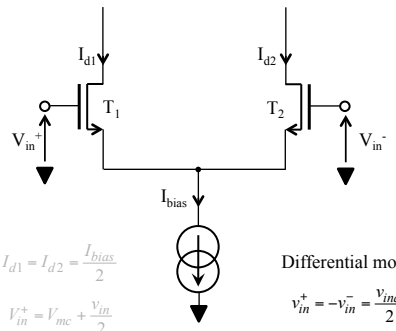


$$A_{vd} = \frac{v_{out}}{v_{ind}} = \frac{V_{out+} - V_{out-}}{v_{ind}} = g_m R_{load}$$

$$A_{vmc} = \frac{v_{out}}{v_{mc}} = \frac{V_{out+} - V_{out-}}{v_{mc}} = 0$$

- Sizing: symmetrical
- Biasing
  - $I_{dsat}=I_{bias}/2$
  - $V_{in+}=V_{in-}=V_{mc}$
  - $V_{s1}=V_{s2} > V_{min}(I_{bias})$
  - $V_{gs1}=V_{gs2}=V_{eff}+V_{tn}$
  - $V_{out}=V_{dd}-R_{load}.I_{bias}/2$
- Small-signal
  - $v_{ind}=V_{in+}-V_{in-}$
  - $v_{out}=V_{out+}-V_{out-}$
  - $v_{mc}=(v_{in+}+v_{in-})/2$

Differential Input Stage: Principle



$$I_{d1} = I_{d2} = \frac{I_{bias}}{2}$$

$$V_{in}^{+} = V_{mc} + \frac{v_{in}}{2}$$

$$V_{in}^{-} = V_{mc} - \frac{v_{in}}{2}$$

$$V_{eff1} = V_{eff2}$$

$$g_{m1} = g_{m2} = g_m$$

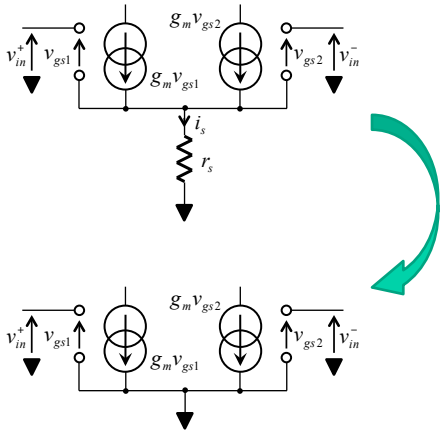
Differential mode

$$v_{in}^{+} = -v_{in}^{-} = \frac{v_{ind}}{2}$$

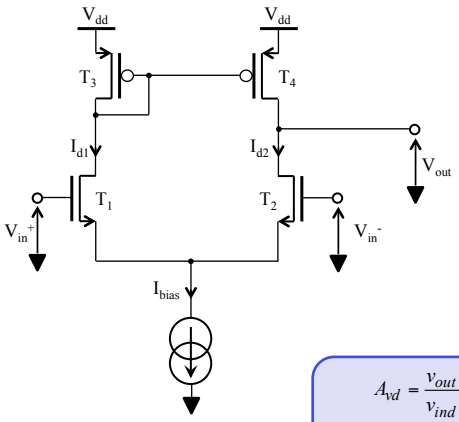
$$v_{gs1} = -v_{gs2}$$

$$g_m v_{gs1} = -g_m v_{gs2}$$

$$i_s = 0$$



Differential Input Stage: high gain implementation

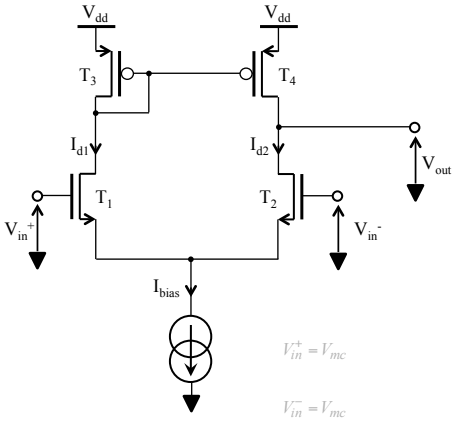


- Active load with a current mirror
  - Higher output resistance
  - Referenced output voltage
- Biasing
  - $V_{out}=V_{dd}-V_{gs3}$

$$A_{vd} = \frac{v_{out}}{v_{ind}} = g_m r_{out}$$

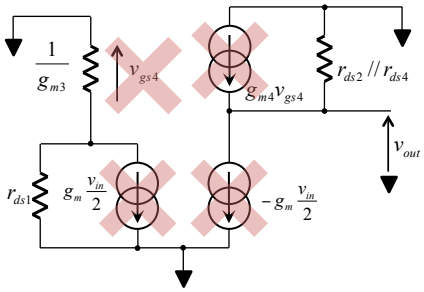
$$A_{vmc} = \frac{v_{out}}{v_{mc}} = 0$$

Differential Input Stage: small-signal output resistance



$V_{in}^{+} = V_{mc}$

$V_{in}^{-} = V_{mc}$



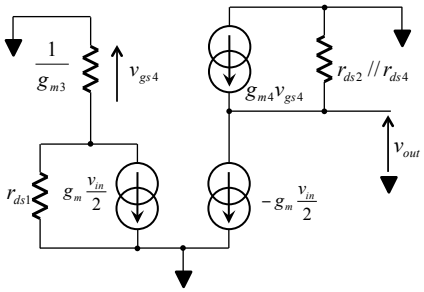
$v_{in} = 0$

$v_{gs4} = 0$

$g_{m4} v_{gs4} = 0$

$$r_{out} = r_{ds2} // r_{ds4}$$

Differential Input Stage: small-signal output voltage



$$v_{out} = \left(g_{m4} v_{gs4} + g_m \frac{v_{in}}{2} \right) \times \left(r_{ds2} // r_{ds4} \right)$$

$$v_{gs4} \approx g_m \frac{v_{in}}{2} \times \frac{1}{g_{m3}}$$

$$v_{out} = \left(\frac{g_{m4}}{g_{m3}} g_m \frac{v_{in}}{2} + g_m \frac{v_{in}}{2} \right) \times \left(r_{ds2} // r_{ds4} \right)$$

$$g_{m3} = g_{m4}$$

$$\frac{v_{out}}{v_{in}} = g_m \times \left(r_{ds2} // r_{ds4} \right)$$

$$V_{in}^{+} = V_{mc} + \frac{v_{in}}{2}$$

$$V_{in}^{-} = V_{mc} - \frac{v_{in}}{2}$$

Differential Input Stage: small-signal gain analysis

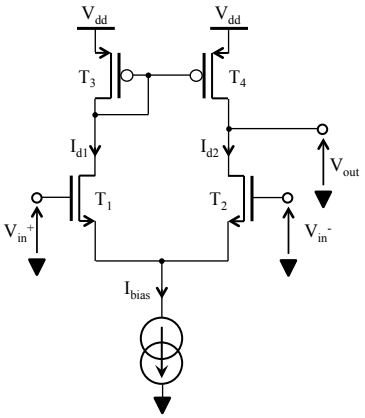
$$\frac{v_{out}}{v_{in}} = g_{m1,2} \times \left(r_{ds2} // r_{ds4} \right) = \frac{g_{m1,2}}{g_{ds2} + g_{ds4}}$$

$$A_v = \frac{g_{m1,2}}{\lambda_n \frac{I_{bias}}{2} + \lambda_p \frac{I_{bias}}{2}}$$

$$g_{m1,2} = \frac{2\left(\frac{I_{bias}}{2} \right)}{V_{eff1,2}} = \frac{I_{bias}}{V_{eff1,2}}$$

$$A_v = \frac{2}{\left(\lambda_n + \lambda_p \right) V_{eff1,2}}$$

Low V_{eff} and large length for large gain



$$V_{eff1,2} = \sqrt{\frac{2 I_{d1,2}}{\mu_n C_{ox}} \frac{L}{W}\Big|_{1,2}}$$

$$A_v = \frac{\sqrt{2 \mu_n C_{ox}}}{(\lambda_n + \lambda_p) \cdot \sqrt{I_{d1,2}}} \sqrt{\frac{W}{L}\Big|_{1,2}}$$

Differential Input Stage: common-mode input range (CMIR)

All transistors must operate in saturation:

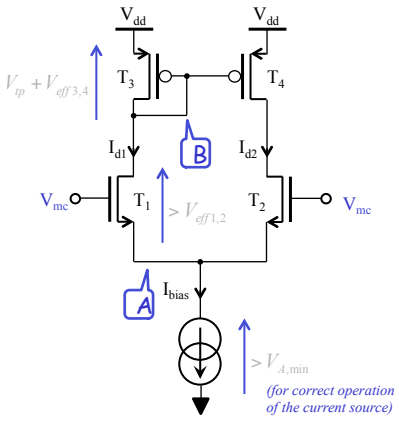
Low V_{eff} for large CMIR

$$V_B = V_{dd} - |V_{eff\,3,4}| - |V_{tp}|$$
$$V_B - V_A > V_{eff\,1,2}$$
$$V_A > V_{A,\min}$$

$$V_A = V_{mc} - (V_{tn} + V_{eff\,1,2}) > V_{A,\min}$$

$$\Rightarrow \boxed{V_{mc} > V_{A,\min} + V_{tn} + V_{eff\,1,2}}$$

$$V_B - V_A > V_{eff\,1,2} \rightarrow V_B > V_{eff\,1,2} + V_A$$
$$V_B > (V_{mc} - V_A - V_{tn}) + V_A$$
$$V_B > V_{mc} - V_{tn}$$
$$V_{mc} < V_B + V_{tn} \Rightarrow \boxed{V_{mc} < V_{dd} - |V_{eff\,3,4}| - |V_{tp}| + V_{tn}}$$



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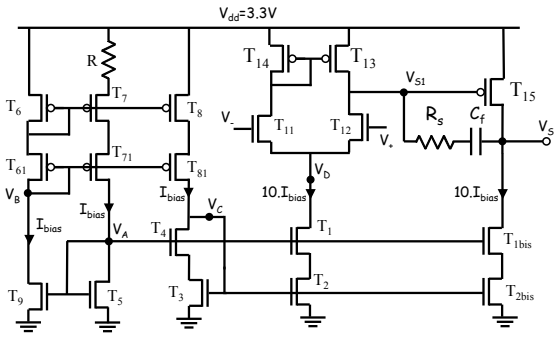
Homework & Lab



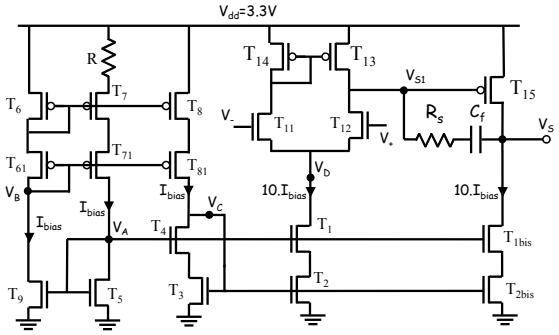
Dimensionnement de l'étage différentiel

1°) Calculez le W/L de T_{13} et T_{14} de façon à ce que la tension de sortie soit égale à 2,5V lorsque V_1=V_2=1,6V. Estimez ensuite la résistance de sortie de cet étage.

2°) Calculez le W/L de T_{11} et T_{12} de façon à ce que le gain différentiel soit de 500.

3°) Quelle serait la fréquence de coupure de cet étage si on connecte une capacité de 5 pF à la sortie à la place du 2ème étage de gain ?

Homework & Lab



Dimensionnement du 2ème étage de gain

1°) Calculez la résistance de sortie de l'étage puis le W/L du transistor T_{15} ainsi que le gain petit-signal de l'étage A_v.

2°) On connecte une résistance de 100kΩ en sortie de l'amplificateur. Calculez le nouveau gain de l'étage A'_v ?

Homework & Lab

Performances statiques de l'OTA Miller

Déterminez les valeurs théoriques du gain statique (petit-signal) de l'amplificateur (en l'absence de charge), de la plage de mode commun d'entrée admissible et de la dynamique de sortie.

Caractérisation statique de l'OTA Miller

Tracez la caractéristique statique $V_S=f(V_+-V_-)$ sans charge de sortie pour un mode commun égal à $V_{dd}/2$. Relevez le point de pente maximum $(V_+-V_-)_{max}$ de cette caractéristique et déduisez-en le gain expérimental.

Caractérisation dynamique de l'OTA Miller

Tracez le diagramme de Bode du montage et concluez sur la stabilité de ce montage utilisé en suiveur de tension.

Montez l'amplificateur en suiveur de tension puis appliquez un échelon de tension entre 1V et 2V sur l'entrée et observez la sortie. Conclure et expliquez les résultats obtenus.